Written Test

Course code: TSTE08, Exam code: TENA

Analog and Discrete-time Integrated Circuits (ISY)

Date:	June 12, 2009
Time:	14-18
Place:	TER2
Number of exercises:	5 (5 points max. for each exercise)
Grades:	10p for 3 (ECTS: C), 15p for 4 (ECTS: B), and 20p for 5 (ECTS:A).
Allowed material:	All types of calcuclators except laptops. All types of official tables and handbooks. Textbooks: Johns & Martin: Analog Integrated Circuit Design. Razavi: Design of Analog CMOS Integrated Circuits. Sedra&Smith: Microelectronic Circuits. Dictionaries.
Examiner and responsible teacher:	Sune Söderkvist
Course administrator:	Sune Söderkvist. Tel.: 281355, mail: sune@isy.liu.se
Visiting today:	Around 15.30 and 17.00.
Corrrect (?) solutions:	Solutions and results will be on the webb home page for the couse.

Graded exams are returned on examinator's office times, tuesdays and fridays at 11.00-13.00, during week no. 34 and 35.

Students instructions

- The CMOS transistor operation regions, small-signal parameters, and noise characteristics are found on the last page of this exam.
- Generally, do not just answer yes or no to a short question. You always have to answer with figures, formulas etc., otherwise no or fewer points will be given.
- You may write down your answers in Swedish or English.

Good Luck!

Exercise 1.

a) Draw a small signal equivalent and determine transfer function $H(s) = V_{out}/V_{in}$, DC-gain and gain-bandwidth (3 dB bandwidth) product for the gainstage in **Figure 1**. (3p)

b) State three ways to increase the value of DC-gain for the gainstage in **Figure 1**.

Both changes to the topology and to the design parameters are allowed.

(The length L of the transistors can not be changed.)

If changing design parameters show why DC-gain is increasing. If changing topology you just need to show *how* it is done; not why DC-gain is increasing. (2p)

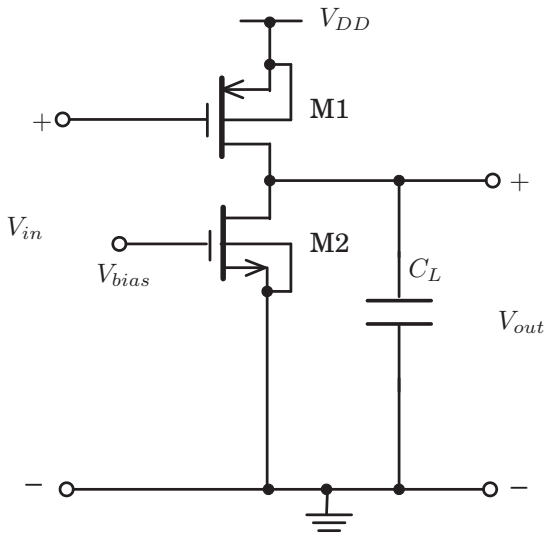

Figure 1: Gain stage.

Exercise 2.

Derive the common-mode range, CMR, and the output range, OR, of the circuit in **Figure 2**. You don't know anything about the relationship between sizes of different transistors. Threshold voltages may be different for all transistors. Anyhow all transistors are saturated. The voltages should be expressed in currents I_{Di}, constants α_i, threshold voltages V_{tni} and V_{tpi}.

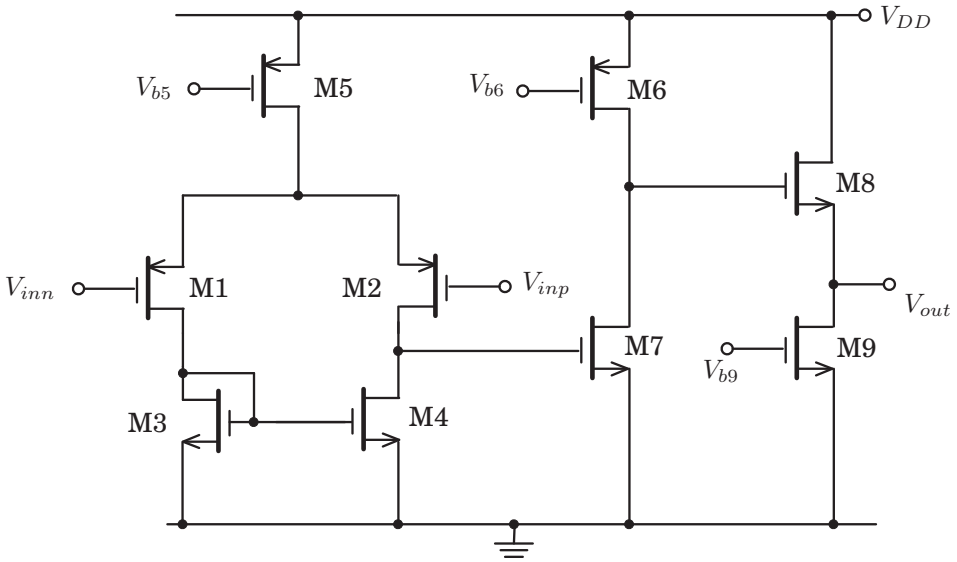

Figure 2: Transistor circuit.

Exercise 3.

The circuit in **Figure 3** is used to establish an appropriate bias voltage V_{bias} to an operational amplifier. The transistors have following parameter values:

	N-channel	P-channel
V_{t0} [V]	0.47	0.62
$\mu_0 C_{ox}$ [muA/V^2]	180	58.5
λ [V^{-1}]	0.03	0.05
γ [V$^{1/2}$]	0.62	0.41
ϕ_F [V]	0.43	0.41

a) Show that all transistors are saturated in this circuit. (1.5p)

b) Determine $\frac{W}{L}\big|_i$, $i = 1, 2, 3$, for transistors Mi , $i = 1, 2, 3$, if $V_{DD} = 3.3$ V, $V_{bias} = 0.6$ V and $I_D = 5$ μ A.

If the potential V_x, on gate of transistor **M1**, is just above 2.05 V it shows that $\frac{W}{L}\big|_2 = \frac{W}{L}\big|_1$. Choose $V_x = 2.05$ V here.

Do not neglect the bulk effekt neither the channel-length modulation. (3.5p)

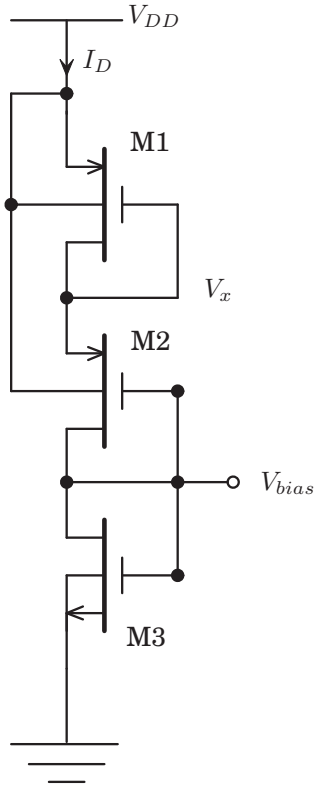

Figure 3: A bias circuit.

Exercise 4.

a) Determine $V_{out}(z)$ as a function of $V_1(z)$ and $V_2(z)$ for the SC-circuit in **Figure 4**. The figure shows the SC-circuit in clock phase I, i.e. at t, $t + 2\tau$, $t + 4\tau$ etc. The OP-amp. is ideal. $v_1(t)$ and $v_2(t)$ are delivered by ideal voltage sources. (4p)

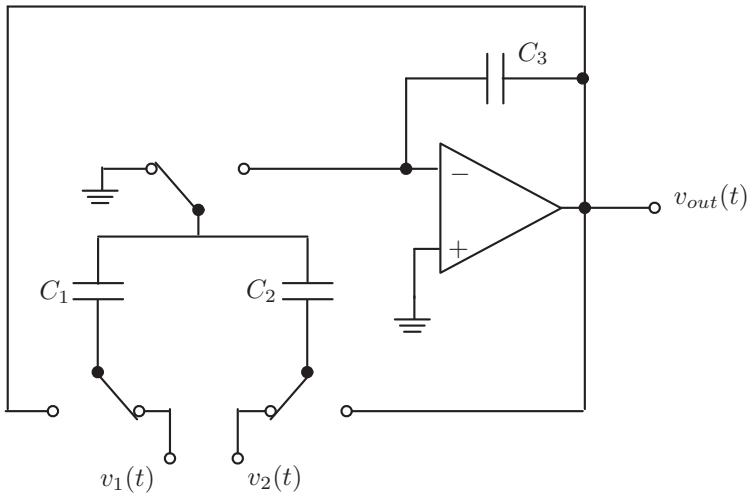

Figure 4: SC-circuit.

b) Is the circuit insensitive or not for capacitive parasitics? Motivate your answer carefully. (1p)

Exercise 5.

The inverting amplifier in **Figure 5a** is used in an application where low noise is of major importance. Hence, a low noise design of the amplifier is required. In this exercise, only the thermal noise in the op.amp. is considered. The gain of the op.amp. $A = g_{m1}/g_{out} = g_{m1}/(g_{ds2} + g_{ds4})$. Further, the ratio between R_2 and R_1 is $R_2/R_1 = a$.

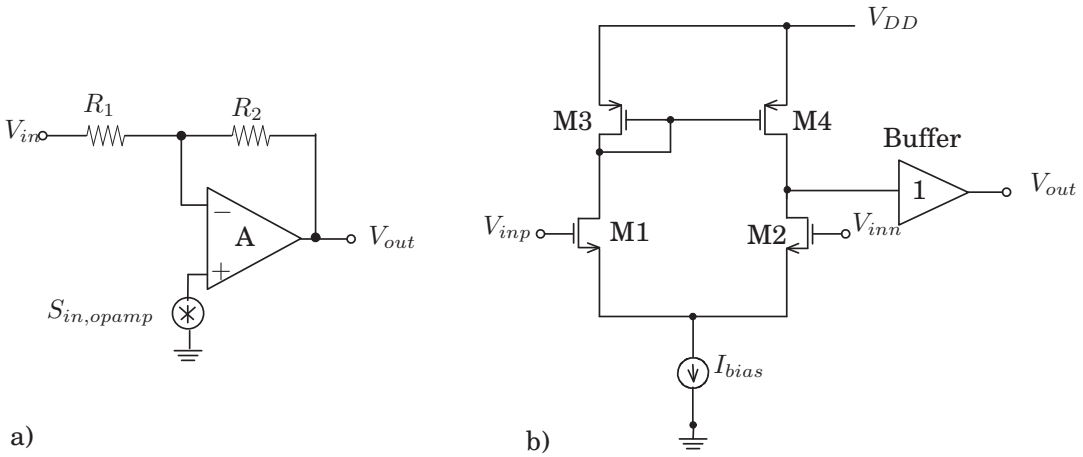

Figure 5: a) A noisy inverting op.amp. b) The principal schematic of the op.amp.

a) Assume that the resistors do not generate any thermal noise while the op.amp. has an equivalent voltage input noise spectral density of

$$S_{in,opamp} = \frac{16kT}{3}\frac{1}{g_{m1}}[1 + \frac{g_{m4}}{g_{m1}}]$$

where the number in the index refers to the op.amp. implementation in **Figure 5b**. Compute the equivalent output noise spectral density for the circuit in **Figure 5a** caused by the noisy amplifier. (4p)

b) State one approach to decrease the equivalent output noise spectral density of the circuit in **Figure 5a** caused by the operational amplifier. How does this impact the DC gain of the open loop amplifier? (1p)

Transistor formulas and noise

1 CMOS transistors

Current and threshold voltage formulas and operating regions for an NMOS transistor

Cut-off:	$V_{GS} < V_t$	$I_D \approx 0$
Linear:	$V_{GS} - V_t > V_{DS} > 0$	$I_D = \alpha(2(V_{GS} - V_t) - V_{DS})V_{DS}$
Saturation:	$0 < V_{GS} - V_t < V_{DS}$	$I_D = \alpha(V_{GS} - V_t)^2(1 + \lambda(V_{DS} - V_{eff}))$
	$V_{DSsat} = V_{eff} = V_{GS} - V_t$	
All regions:	$V_t = V_{t,0} + \gamma(\sqrt{2\phi_F - V_{BS}} - \sqrt{2\phi_F})$	

Small-signal parameters

Linear:	$g_m \approx 2\alpha V_{DS}$	$g_{ds} \approx 2\alpha(V_{GS} - V_t - V_{DS})$
Saturation:	$g_m \approx 2\sqrt{\alpha I_D}$	$g_{ds} \approx \lambda I_D$

Constants: $\alpha = \frac{1}{2}\mu_{0n}C_{ox}\frac{W}{L}$ $\lambda = \sqrt{\frac{K_s\epsilon_0}{2qN_A\phi_0}} \cdot \frac{1}{L}$ $\gamma = \frac{\sqrt{2qN_AK_s\epsilon_0}}{C_{ox}}$

2 Circuit noise

Thermal noise in CMOS transistors
The thermal noise spectral density at the gate of a CMOS transistor is

$$V^2(f) = \frac{8kT}{3} \cdot \frac{1}{g_m}$$

Thermal noise in resistors
The thermal noise spectral density of a resistor is modeled as a parallel noise current source

$$I^2(f) = \frac{4kT}{R}$$

Flicker noise in CMOS transistors
The flicker noise spectral density at the gate of a CMOS transistor is

$$V^2(f) = \frac{K}{WLC_{ox}f}$$