TSTE08, Analog and Discrete-time Integrated Circuits, 2011-08-24
Written exam, TENA

Date and time	2011-08-24, 8.00 - 12.00
Location(s)	TER2
Responsible teacher	J Jacob Wikner, jacwi50, +46-70-5915938
Aid	Any written and printed material, including books and old exams. Note! No pocket calculators, no laptops, no iPods, no telephones, no internet connection.
Instructions	A maximum of 25 points can be obtained from the written exam. Three points can be obtained from quizzes. In total: 10 points are required to pass, 15 for a grade four, and 20 for a grade five. ˣ *Hint!* ***Be strategic*** *when you pick exercises to solve. You have five exercises in four hours and you could therefore spend some 45 minutes on each exercise. That leaves you 15 minutes to relax...* Note that a **good motivation to your answer** must be included in your solutions in order to obtain maximum number of points! With "motivation" mathematical derivations are understood (and not only text). Also note that the questions in this exam are divided into logical sections. You may use **Swedish, English or German** in your answers. Notice that some questions are **"hidden" in the text** and therefore: read the instructions carefully! ˣ *Notice also that eventhough you do not fully know the answer, please add some elaborations on your reasoning around the question. Any (good...) conclusions might add up points in the end.*
Results	Available within two weeks from exam date (hopefully...)

Outline

1. NOISE (5 P)

✗ *We'll take a simple one this time too ...*

Consider the circuit in Figure 1.1. It is a you-know-what. The circuit is balanced symmetrically such that the input and output DC points are equal.

1) Derive a compact expression of the **total output noise power** for the circuit**!**

2) Derive the **input-referred noise spectral density!**

3) How should you minimize the total noise when **maintaining the bandwidth**?

Make valid assumptions and motivate them well!

✗ ***Finding a compact expressions implies in this context: "Minimize the number of parameters in your expression."***

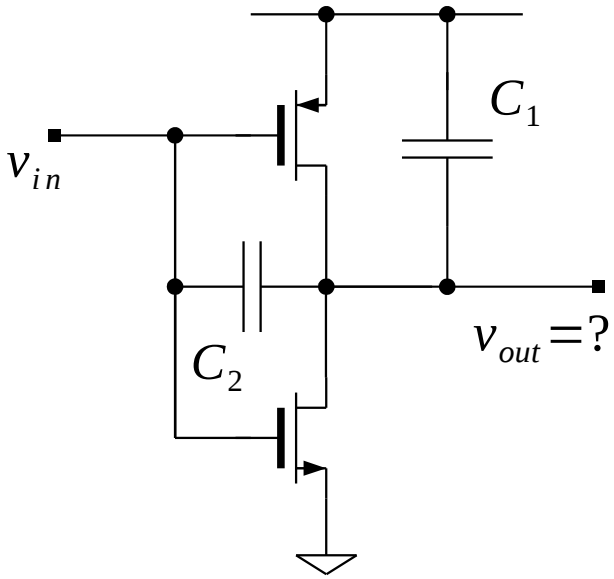

Figure 1.1: Phew! Three transistors...

✗ *Tip! Use symmetries to speed up your conclusions.*

✗ *Don't forget that you have to consider the **total noise power** at the output. Hint: use the noise brickwall bandwidth:* $p_1/4$ *(see for exampleJohns Martin).*

2. OP/OTA, STABILITY (5 P)

✗ *OK, so we saw this one last exam... but the number of answers was low... show me that you can plug in the numbers and understand the exercise.*

Consider the configuration in Figure 2.1, which consists of a current mirror and two other transistors. One can see that this is a simplified version of a current-mirror OTA. You can safely assume that all transistors operate in their saturation regions. Obviously it is a kind of two-stage amplifier (?) and you would have a parasitic capacitance, C_p, as indicated in the figure.

Assume the following: (1) $C_{gs} \approx C_{ox} W L/2$ is the dominating capacitor of a single NMOS transistor and for simplicity (2) $g_{mp} = g_{mn}$.

For which values of C_L does the circuit have a 63-degree phase margin (and more)? Especially, express how this relates to the mirror ratio, K.

Make valid assumptions and motivate them well!

✗ *Minimize the number of parameters in your expressions.*

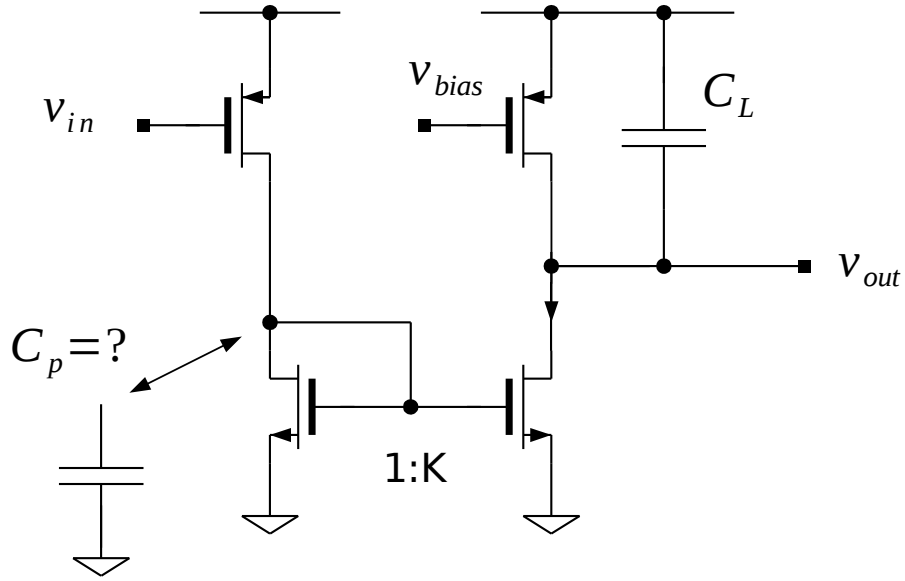

Figure 2.1: Transistors in a gain configuration.

✗ *Once again! Any (reasonable) try to answer the question can give you credits!*

✗ *And once again! Do not forget to present your results properly!*

✗ $\tan^{-1}(\text{large number}) \approx 90$ *degrees,* $\tan^{-1}(2) \approx 63$ *degrees.*

3. SWITCHED CAPACITOR CIRCUITS, ETC. (5 P)

Consider the circuit in Figure 3.1. It has an ideal operational amplifier, one capacitor and some three switches that operate in nonoverlapping phases, ϕ_1 and ϕ_2.

1) Find the transfer function of this circuit by doing a proper charge redistribution analysis.

2) Given your results explain what kind of transfer function it describes is!

3) Help yourself (and me...) by sketching the output voltage in the time domain (provide some example input signal).

4) Assume that the input, $v_1(t)$ is a ramp, that the switching frequency is a very high frequency. Derive the output signal as a function of the on-resistance of the switches. Assume the on-resistance to be a constant value, R_{on} (ie. independent of the voltage levels).

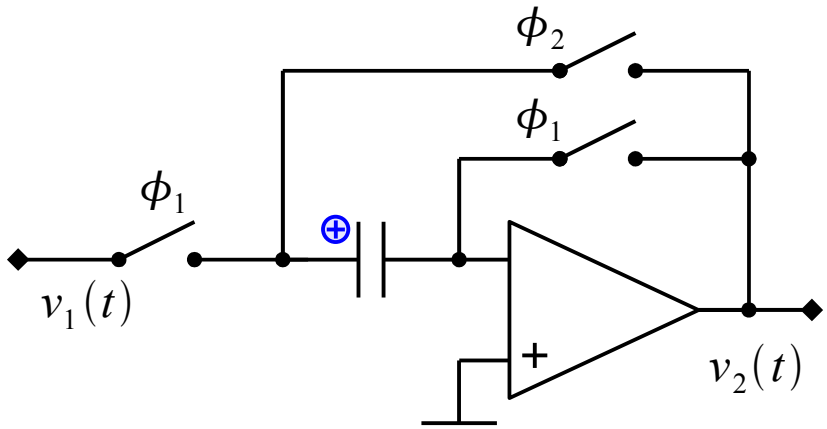

Figure 3.1: Some kind of SC-stuff

✗ *Do not forget to present your calculations properly!*

4. DATA CONVERTERS (ADCS) (5 P)

There is normally a relationship between speed and accuracy of a comparator. Assume that the comparator is an amplifier in open-loop configuration. The (linearized) transfer function in the frequency domain can be described by:

$$A(s)=\frac{A_0}{1+s/p_1} \tag{4.1}$$

where A_0 is the DC gain and p_1 is the dominant pole of the comparator. A typical scenario could be the step response in Figure 4.1 where $V_H=V_{DD}-V_L$ and V_L are the digital detection levels, respectively.

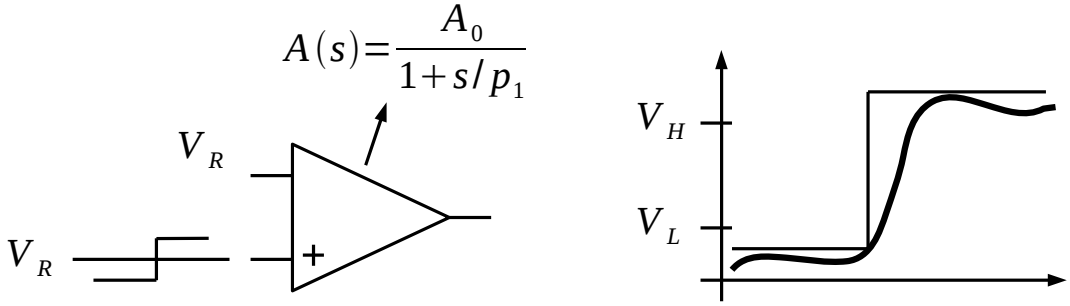

Figure 4.1: Comparator with its step response. Thick curve is the kind of non-ideal one.

1) Find the minimum decision time for the comparator given an input step of ΔV across the reference voltage. Assume that the comparator gain is constant over the input/output voltage ranges.

2) What is the maximum operating frequency, f_{max}, of a data converter using this comparator, as a function of the number of bits N, i.e.,

$$\Delta V=\frac{2V_R}{2^N}. \tag{4.2}$$

3) Sketch the relationship between the number of bits and the ratio between maximum sample frequency and dominant pole of the comparator, f_{max}/p_1.

5. FILTERS, ETC. (5 P)

Consider the “filter” in Figure 5.1. It consists of an operational amplifier, an impedance connected to the input, v_{in}, and a feedback impedance connected to the output, v_{out}.

Assume that the Z_i is a resistance, $Z_i = R_i$, and that the feedback impedance is a resistor in parallel with a capacitor, i.e., $Z_f = R_f / (1 + s R_f C_f)$.

Now assume that the amplifier has two limitations: the DC gain is only 20x and it can only drive an output current of I_{max}.

1) What's the slew rate of this device? I.e., what's the maximum output slope it can drive?

2) What's the maximum voltage swing you can apply at the input without saturating the device?

3) In general -- what is the impact due to the limited DC gain? Can you compensate for this “error” in some clever way using Z_i and Z_f?

There is no additional load on the amplifier and the input is an ideal voltage source.

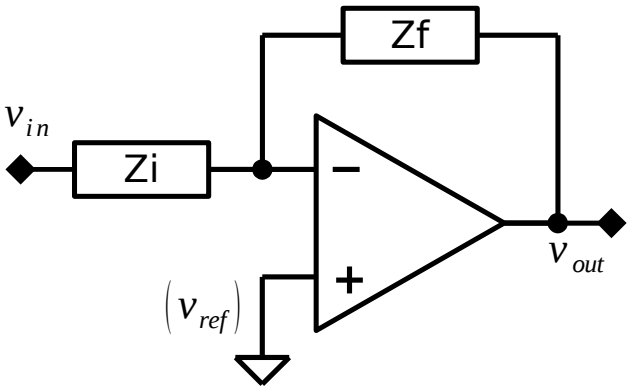

Figure 5.1: Some impedance link of some kind