TSTE08, Analog and Discrete-time Integrated Circuits, 2011-03-16
Written exam, TENA

Date and time	2011-03-16, 14.00 - 18.00
Location(s)	TER3 (32 copies printed)
Responsible teacher	J Jacob Wikner, jacwi50, +46-70-5915938
Aid	Any written and printed material, including books and old exams. Note! No pocket calculators, no laptops, no iPods, no telephones, no internet connection.
Instructions	A maximum of 25 points can be obtained from the written exam. Three points can be obtained from quizzes. In total: 10 points are required to pass, 15 for a grade four, and 20 for a grade five. ✗ *Hint!* ***Be strategic*** *when you pick exercises to solve. You have five exercises in four hours and you could therefore spend some 45 minutes on each exercise. That leaves you 15 minutes to relax...* Note that a **good motivation to your answer** must be included in your solutions in order to obtain maximum number of points! With "motivation" mathematical derivations are understood (and not only text). Also note that the questions in this exam are divided into logical sections. You may use **Swedish, English or German** in your answers. Notice that some questions are **"hidden" in the text** and therefore: read the instructions carefully! ✗ *Notice also that eventhough you do not fully know the answer, please add some elaborations on your reasoning around the question. Any (good...) conclusions might add up points in the end.*
Results	Available by 2011-03-31 (hopefully...)

Outline

1. NOISE (5 P)

✗ *We'll take a simple one this year ...*

Consider the circuit in Figure 1.1. The input voltage, v_{in}, is connected to the PMOS and the current mirror sets the bias current through the active device. Only consider the thermal noise of the transistors.

1) Derive a compact expression of the **total output noise power** for the circuit**!**

2) Derive the **input-referred noise spectral density!**

3) Express and sketch **how the total output noise power depends on the bias current,** I_0! Should the current be **minimized or maximized** for minimum noise?

4) How should you **set the mirror ratio** for maintained gain but lower noise?

Make valid assumptions and motivate them well!

✗ ***Finding a compact expressions implies in this context: "Minimize the number of parameters in your expression."***

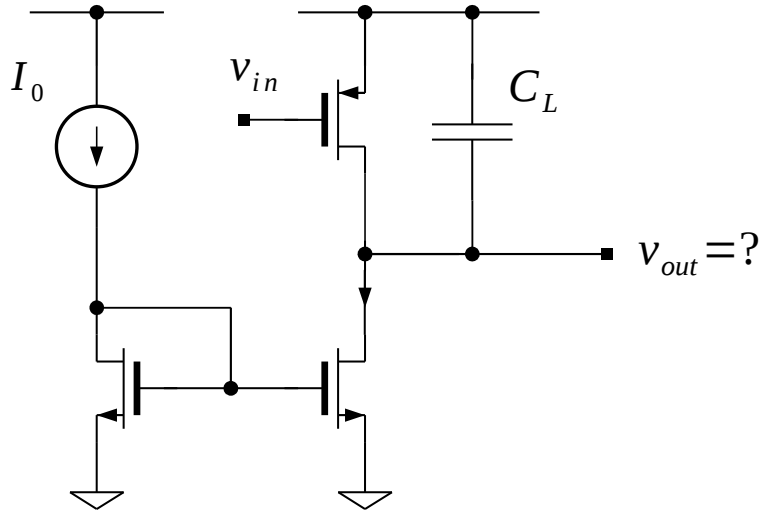

Figure 1.1: Phew! Three transistors...

✗ *Tip! Use symmetries to speed up your conclusions.*

✗ *Don't forget that you have to consider the* ***total noise power*** *at the output.*

Hint: use the noise brickwall bandwidth: $p_1/4$ *(see for exampleJohns Martin).*

2. OP/OTA, STABILITY (5 P)

OK, so a question on stability in amplifiers, etc. Consider the configuration in Figure 2.1, which consists of a current mirror and two other transistors. One can see that this is a simplified version of a current-mirror OTA. You can safely assume that all transistors operate in their saturation regions. Obviously it is a kind of two-stage amplifier (?) and you would have a parasitic capacitance, C_p, as indicated in the figure.

Assume the following: (1) $C_{gs} \approx C_{ox} W L/2$ is the dominating capacitor of a single NMOS transistor and for simplicity (2) $g_{mp} = 4 \cdot g_{mn}$.

Express the total DC gain as a function of the mirror ratio, K.

For which values of C_L does the circuit have a 45-degree phase margin (and more)? Sketch and express how this relates to the mirror ratio, K.

Make valid assumptions and motivate them well!

- *Minimize the number of parameters in your expressions.*

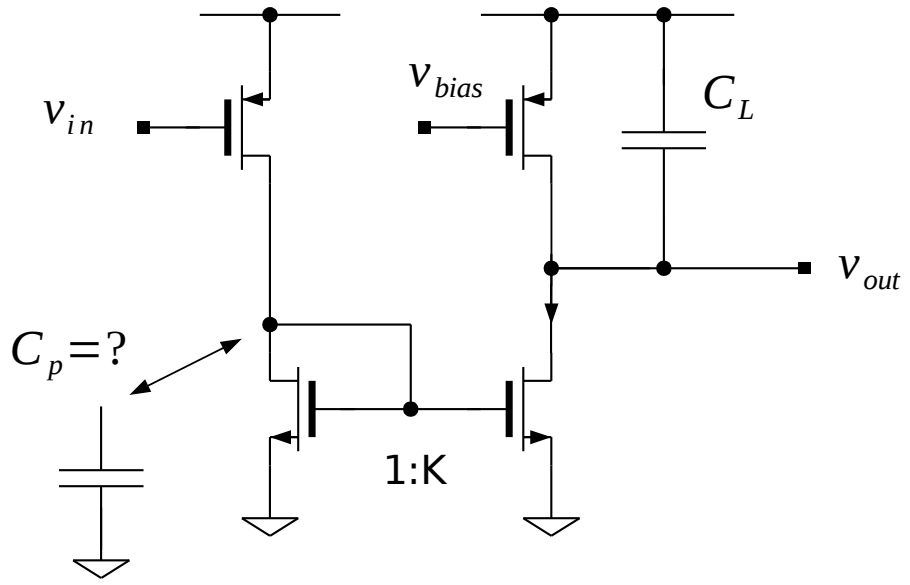

Figure 2.1: Transistors in a gain configuration.

- *Once again! Any (reasonable) try to answer the question can give you credits!*
- *And once again! Do not forget to present your results properly!*

✗ $\tan^{-1}(\text{large number}) \approx 90$ *degrees,* $\tan^{-1}(1) = 45$ *degrees.*

3. SWITCHED CAPACITOR CIRCUITS, ETC. (5 P)

Consider the circuit in Figure 3.1. It has an ideal operational amplifier, two capacitors and some four switches that operate in nonoverlapping phases, ϕ_1 and ϕ_2.

1) Find the transfer function of this circuit by doing a proper charge redistribution analysis.

2) Given your results explain what kind of transfer function it describes is! This is a special circuit and therefore state the important parameters that are so typically associated with this one.

3) Is it parasitic insensitive? **Motivate well and show steps!**

4) Help yourself (and me...) by sketching the output voltage in the time domain (provide some example input signal).

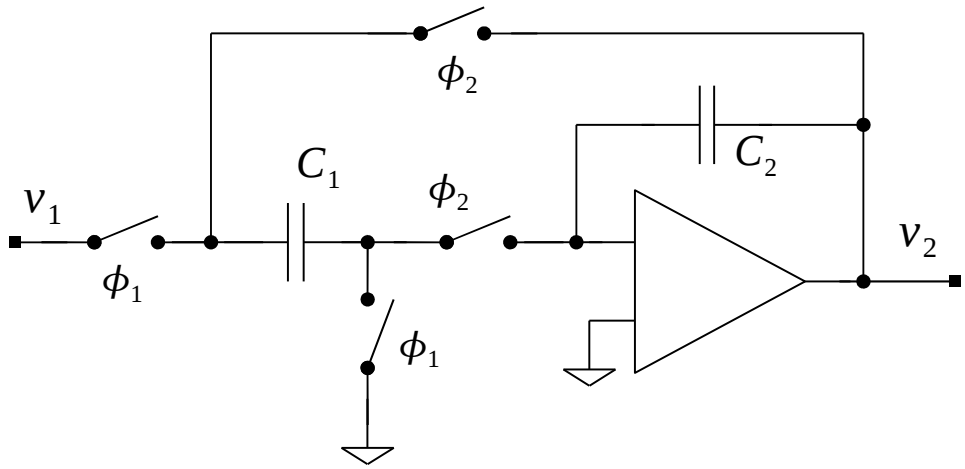

Figure 3.1: Some kind of SC-stuff

✗ *Do not forget to present your calculations properly!*

4. DATA CONVERTERS (ADCS)

The noise analysis in question one was so simple this time ... let us extend to cover also data converters.

You want to design an uniformly sampling and uniformly quantizating N-bit flash ADC. The conversion range is 1 V. The reference levels for the comparators are given by a resistor string containing a total resistance of

$$R_{tot}=2^N\cdot\Delta R \tag{4.1}$$

where ΔR is a unit resistance. Assume that all resistors in the resistive divider are noisy. The thermal noise voltage spectral density for any resistance, R, is given by

$$v_{nR}^2(f)=4kTR \tag{4.2}$$

and can be assumed to be white, i.e., a Gaussian distribution.

Assume that, magically, the bandwidth of the resistive divider equals the sample frequency of the converter, f_s, for all reference nodes.

1) What is the (theoretical) **quantization noise power** of the converter provided the sample frequency is f_s, the input signal bandwidth is $f_{BW}=4\cdot f_s$, and the decimation filters receiving the ADC output have an ideal bandwidth of $f_s/2$.

2) In the text above we have put two requirements on the ADC to be able to do the type of calculations we do in 1). What is missing?

3) How large can ΔR be **without having any impact on performance** (assume a 6-sigma limit on the thermal noise)? Express this in terms of number of bits, N, and sample frequency, f_s.

- *Notice that you need to work with some probability theory - the noise has a Gaussian distribution, hence the comment on 6 sigma above.*
- *Are you really comparing right things with eachother? Apples and pears - as we say in Swedish.*

5. FILTERS, OPAMPS, ETC.

Implement the following transfer function

$$H(s)=\frac{V_2(s)}{V_1(s)}=\frac{K\cdot\omega_0^2}{s^2+\frac{\omega_0}{Q}s+\omega_0^2} \tag{5.1}$$

using the leapfrog approach (see Figure 5.1 for an outline and suggested starting point for your work). All the three parameters K, ω_0, and Q, are positive numbers. We can set the DC gain of the filter to unity and the cut-off frequency to be 10 MHz. We can set the quality factor to $1/\sqrt{2}$.

1) Realize the filter using active RC components! Use a minimum number of single-ended operational amplifiers. Use Figure 5.1 as a guidance.

2) Suggest different R and C values, i.e., find the R and C that give you the K, ω_0, and Q values.

3) Assume the filter is implemented using OTAs rather than OPs. How should you in that case select the values on R and C?

4) In general - in a modern, 45-nm CMOS process and a filter of this type, how large would you set the components?

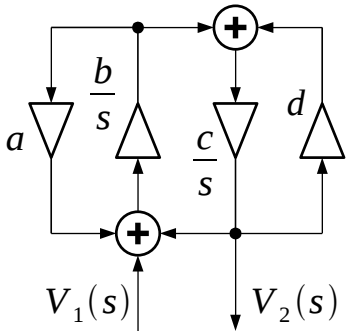

Figure 5.1: Second-order leapfrog approach...

- *Hint! We have been looking at odd-order structures (mainly third-order) in our leapfrog filters. Strip the existing Leapfrog diagram and see what happens if you only save two integrators.*
- *Do not forget the option to invert nodes if needed ...*
- *Subquestions 2, 3, and 4 are more or less the same question...*