TSTE08, Analog and Discrete-time Integrated Circuits, 20100611
Written exam, TENA

Date and time	20100611, 14.00 - 18.00
Locations	KÅRA
Responsible teacher	J Jacob Wikner, jacwi50, +46705915938
Aid	**Any written and printed material, including books and old exams.** **Note! No pocket calculators, no laptops, no ipods, no telephones, no internet connection.**
Instructions	A maximum of 25 points can be obtained, 10 points are required to pass, 15 for a grade four, and 20 for a grade five. *Hint! **Be strategic** when you pick exercises to solve. You have five exercises in four hours and you could therefore spend some 45 minutes on each exercise. That leaves you 15 minutes to relax...* Note that a **good motivation to your answer** must be included in your solutions in order to obtain maximum number of points! With "motivation" mathematical derivations are understood (and not only text). Also note that the questions in this exam are divided into logical sections. You may use **Swedish, English or German** in your answers. Notice that some questions are **"hidden" in the text** and therefore: read the instructions carefully! *Notice also that eventhough you do not fully know the answer, please add some elaborations on your reasoning around the question. Any (good...) conclusions might add up points in the end.*
Results	Available by 2010-07-01 (hopefully...)

Outline

1. CMOS, PERFORMANCE, ETC. (5 P)

Consider the circuit in Figure 1.1 below. Assume that the signal is fed through the bulk of the NMOS transistor rather than one of the other fun terminals. Further, assume that the transistor behaves according to the "school book", i.e., for saturation region we have

$$I_D=\alpha\cdot\left(V_{GS}-V_T\right)^2 \text{ where } \alpha=\frac{\mu_0 C_{ox}}{2}.\frac{W}{L}. \quad (1.1)$$

and for the threshold voltage we have some weird expression like

$$V_T=V_{T0}+\gamma\cdot\left(\sqrt{V_{SB}+2\phi}-\sqrt{2\phi}\right) \text{ where } V_{T0},\ \gamma, \text{ and } \phi \text{ are parameters.} \quad (1.2)$$

Express the DC gain in terms of V_{bias}, I_D, R_L, and transistor parameters. Minimize the degree of freedom in your expression. Make reasonable assumptions (and motivate them). Since you will find some of these results in your notes, we want to see some good derivations in your answers...

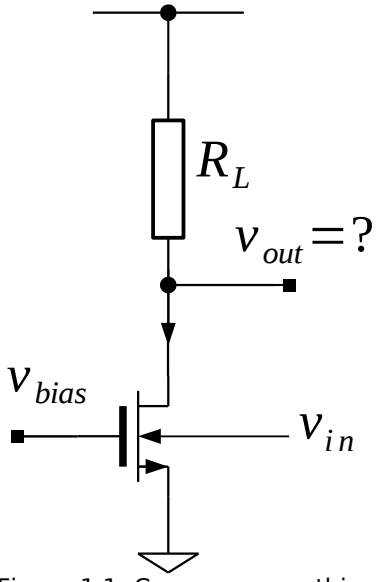

Figure 1.1: Common-something

Then express **the maximum and minimum input voltage on the bulk terminal**, such that the transistor is still in its saturation region. You probably need to use the V_{bias} and V_{out} voltage in your expression.

Sketch the output DC point as a function of the bulk DC point, indicate break points, etc.

- *This exercise will show that you have understood basic small-signal properties. It always helps with some figures for the small signal schematics too.*
- *Hint: How negative can the bulk terminal be? And also, do not forget the sign.*

2. GAIN STAGES, SWING, ETC. (5 P)

Consider the circuit in Figure 2.1 which is some kind of differential pair or so. You have two things to do for this exercise:

Derive the 3-dB bandwidth of the circuit and express the bandwidth in terms of transistor parameters and **input voltage DC level**.

How can you **maximize the bandwidth**? (No, C_L cannot be touched this time...)

Also derive the input and output voltage range for which all transistors are in their saturation regions. Use a minimum number of parameters in your expression.

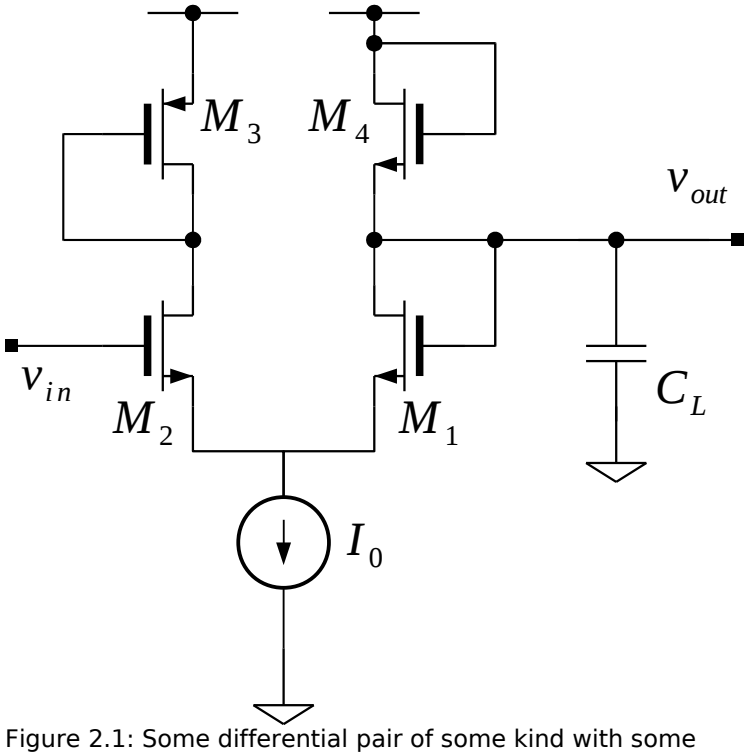

Figure 2.1: Some differential pair of some kind with some kind of load.

Make valid assumptions and motivate them well in your solutions.

- *This exercise will show that you have understood the relation between schematics and small-signal expressions as well as large-signal operation.*
- *Don't forget to sanity check your results! Hint: what should the DC gain be?*
- *Tip: the phrase "valid assumptions" is a very vague statement and you could probably decide on your own what "valid" means ...*

3. NOISE (5 P)

Consider the circuit in Figure 3.1 which consists of two PMOS and one NMOS transistor. With your experience you see that it is a common-gate stage.

Assume that all transistors are noisy and derive the **total output noise power and the input-referred noise spectral density** of the circuit.

Once again, this is a rather standard exercise for which you will find answers in the books and notes. Therefore, we **require clear illustrative solutions**.

Also, express **how the input-referred noise depends on the width** of the transistor connected to V_{b3}. Sketch a diagramme showing the noise spectral density as function of W_3.

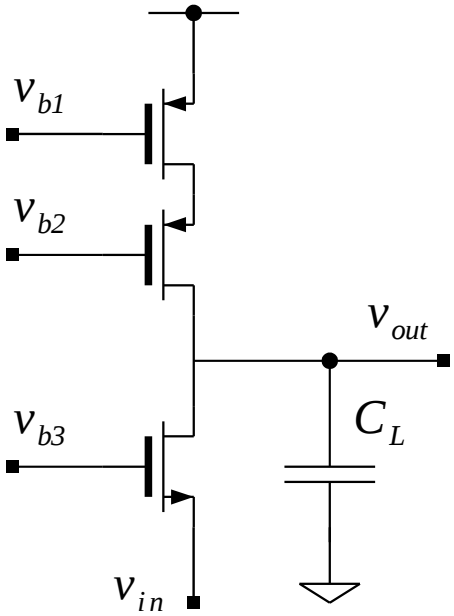

Figure 3.1: Phew! Three transistors...

- *Tip 1: Parts of this exercise is found in the course exercise manual!*
- *Tip 2: Use all the symmetries to speed up your conclusions.*
- *Tip 3: To find max SNR, minimize the expression w.r.t. the number of parameters.*
- *Don't forget that you have to consider the **total noise power** at the output. Hint: use the noise brickwall bandwidth: $p_1/4$ (see for exampleJohns Martin).*

4. OP/OTA (5 P)

OK, so a question about OP/OTA. Consider the feedback configuration in Figure 4.1. Now, assume the following transfer characteristics for the **open-loop amplifier**:

$$v_{OP,out}(s)=v_{OP,in}(s)\cdot\frac{A_0}{1+s/p_1}$$ where A_0 is a finite constant. (4.1)

Assume that the p_1 pole does not shift its position when the OP/OTA is in a feedback configuration. (This means that the p_1 pole is set internally in the OP/OTA and independent on the load).

Derive the overall transfer function for the amplifier and **express two shortcomings** compared to an ideal amplifier that this configuration suffers from, i.e., compare your results with the ideal transfer function:

$$v_{out}(s)=-\frac{R_0}{R_1}\cdot v_{in}$$ (4.2)

> ✗ *Don't just answer: property X is different. Isolate the property in your expression, motivate how and what impact it has on the overall transfer function!*

Also, assume that the maximum output current that can be delivered to the output is given by I_0. **Derive how the swing of the OP/OTA in feedback configuration is affected by this limited current!** Give an illustrative example.

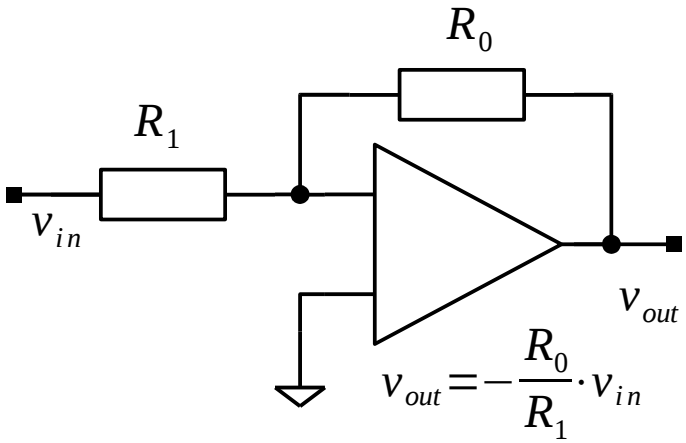

Figure 4.1: Closed-loop gain configuration.

5. SWITCHED CAPACITOR CIRCUITS (5 P)

Whew! Finally... the last question (this time...)

Consider the circuit in Figure 5.1 where you have an input signal, v_{in}, two main capacitors, C_1 and C_2 (and a parasitic load, C_{out}), two non-overlapping clock phases, ϕ_1 and ϕ_2.

The buffer is ideal and is connected in a negative feedback configuration achieving unity gain. The switches operate at the sample frequency $f_s=1/T$. For now we assume that the switches are ideal too and that the input is driven by an ideal source.

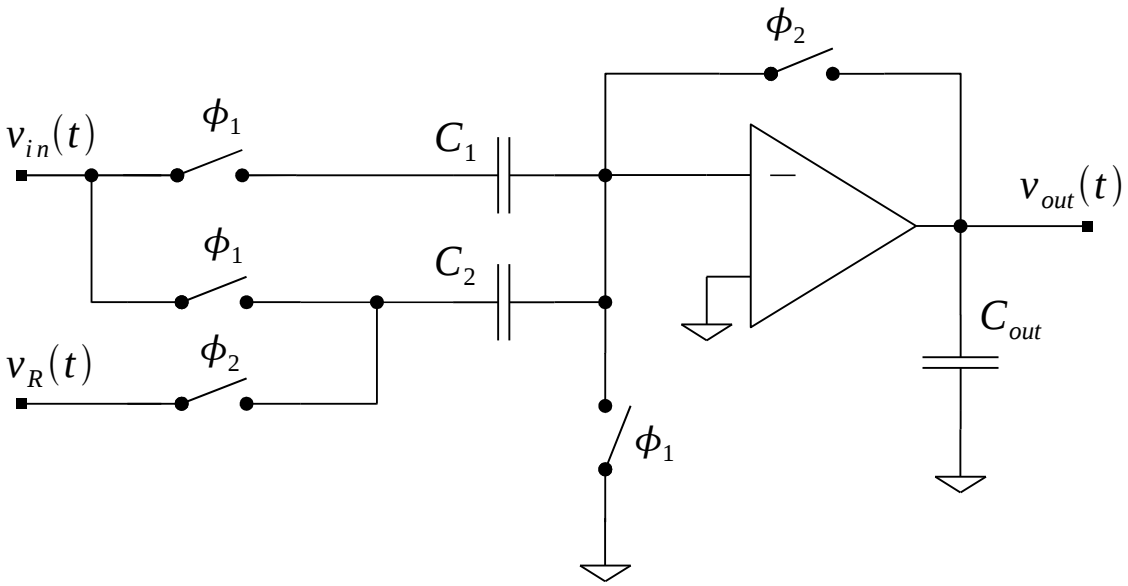

Figure 5.1: An SC circuit.

Derive the transfer function from input to output in a discrete-time sense, i.e., how relates $v_{out}(nT)$ and $V_{out}(z)$ to $v_{in}(nT)$ and $V_{in}(z)$ as well as $v_R(nT)$ and $V_R(z)$. Express the transfer function in the z-domain, i.e. $H(z)$ where z refers to the sample period as $z=e^{j\omega T}$. Show all steps to demonstrate your answer. Be careful with half-delays!

Explain **if the circuit is sensitive to parasitics or not**.

What kind of circuit is this? How does the transfer functions change with C_1 and C_2?

Once again! Don't be overwhelmed by the size of the exercise. Any (reasonable) try to answer the question can give you credit!