TSTE08, Analog and Discrete-time Integrated Circuits, 2010-03-16
Written exam, TENA

Date and time	2010-03-16, 8.00 - 12.00
Locations	U3, U4, and U6
Responsible teacher	J Jacob Wikner, jacwi50, +46-70-5915938
Aid	**Any written and printed material, including books.** **Note! No pocket calculator, no laptops, no ipods, no telephones, no internet.**
Instructions	A maximum of 25 points can be obtained, 10 points are required to pass, 15 for a grade four, and 20 for a grade five. (Hint! **Be strategic** when you pick exercises to solve. You have five exercises in four hours and you could therefore spend some 45 minutes on each exercise. That leaves you 15 minutes to relax...) Note that a **good motivation to your answer** must be included in your solutions in order to obtain maximum number of points! With "motivation" adequate mathematical derivations are understood (and not only text). Also note that the questions in this exam are divided into logical (?) sections. You may use **Swedish, English or German** in your answers. Notice that some questions are **"hidden" in the text** and therefore: read the instructions carefully! ✗ *Notice also that eventhough you do not fully know the answer, please add some elaborations on your reasoning around the question. Any (good...) conclusions might add up points in the end.*
Results	Available by 2010-04-01

Outline

1. MISC: CMOS, PERFORMANCE, ETC. (5 P)

You just graduated from the University and has got your first employment. Your task is to implement an analog circuits using new CMOS building blocks.

The strange thing with the technology provided is that in the saturation region the current of the transistor is now given by:

$$I_D=\alpha\cdot V_{eff}^3\cdot\left(1+\lambda^2\cdot V_{ds}^2\right), \text{ where } \alpha=\frac{\mu_0 C_{ox}}{2V_0}\cdot\frac{W}{L}. \quad (1.1)$$

$V_{eff}=V_{gs}-V_t$ and $\lambda\cdot V_{ds}<1$ are the "normal" definitions, but the parameter V_0 is added to compensate for the cube of V_{eff}. This transistor is in its saturation region as long as $V_{eff}<V_{ds}$ and is on as long as $V_{eff}>0$. Assume the linear region behaves as "usual".

Elaborate on the characteristics of transconductance (g_m), gain $(A_0=g_m/g_{ds})$ and output impedance $(r_{out}=1/g_{ds})$ for this type of transistor. **Derive these parameters and express them using compact formulae suitable for hand calculations!**

Sketch the DC transfer curve for this type of NMOS transistor used in a common-source amplifier with resistive load towards the positive supply (see Figure 1.1). Indicate the transistor operating regions in your graph and the break points by **referring to the parameters you just derived**.

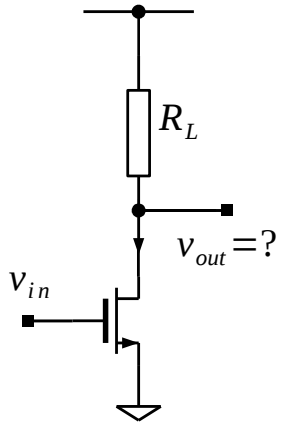

Figure 1.1: Common-source

Since you are a very pro-active person, also **show your product manager what would happen if you would have a general transistor model** as:

$$I_D=\alpha\cdot V_{eff}^a\cdot\left(1+\left(\lambda\cdot V_{ds}\right)^b\right), \quad (1.2)$$

(where $a\geq 1$ and $b\geq 1$ are real numbers and we assume that α will be adjusted to α/V_0^{a-2}) by illustrating for him/her what a and b values should be used to obtain a high-quality transistor suitable for analog amplifier design?

- *This exercise will show that you have understood basic small-signal properties and desirable features of a transistor.*
- *Tip: eq (1.1) is a subset of eq (1.2) ...*

2. GAIN STAGES (5 P)

Consider the circuit in Figure 2.1 which shows some strange circuit driven by a cascoded current source. You can assume that the reference current, I_0, is generated by a wide swing current mirror hence the two additional transistors illustrated in the figure. The ϕ_1 and $\check{\phi}_1$ are two non overlapping switching phases.

Determine the input and output range of the circuit that guarantees all transistors but M3 to be operating in the saturation region. Motivate your choise of bulk connections.

To properly present your results, **sketch the input and output waveforms**, v_{in} and v_{out}, for a couple of switched phases provided an input (v_{in}) sinusoid at a frequency lower than the switching frequency. The input sinusoid should cover the whole input range as defined before. Clearly indicate time, amplitude, etc.

Power consumption is of concern. **What happens to your input and output range** if you reduce I_0 to 50 % of its original value? **What happens to the bandwidth and DC gain of the circuit for the same case?**

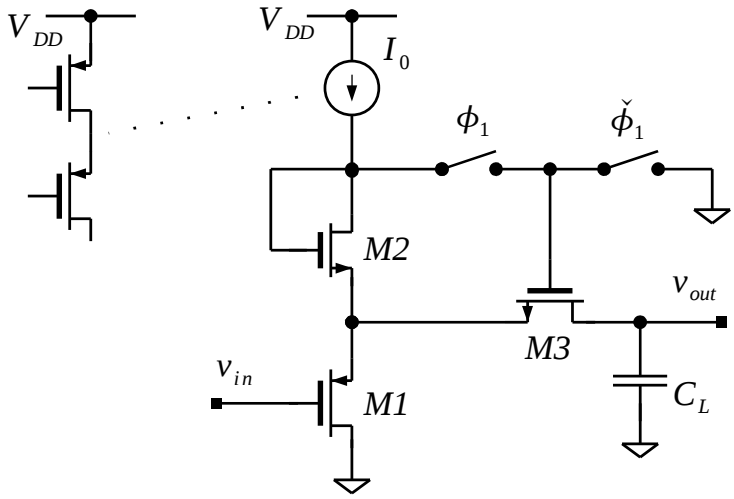

Figure 2.1: A circuit.

Why is this topology chosen for this kind of circuit?

- *This exercise will show that you have understood the relation between schematics and small-signal expressions as well as large-signal operation.*
- *Please do not feel that the exercise is too large for the exam. Answer the questions as good as you can. Any good answers can give you some*

credit!

- *Tip: When calculating DC gain, do a clever assumption w.r.t. the output resistance of the gain stage and w.r.t. the M3 operating region to save time.*

3. NOISE (5 P)

Consider the circuit in Figure 3.1. It is a hmmm-hmm-hmm stage consisting of a hmm-hmmm mirror. Assume that the mirror ratio is 1 to 1, i.e., M2 and M3 are of same size. Also assume all transistors are operating in their saturation region.

Further on, the layout of the circuit has been done by someone without "5+ years of experience" which means that the supplies and grounds will pick up noise. We can assume that the V_{SS0} nodes are well-defined, i.e., true ground. However V_{SS1} is not and the supplies V_{DD1} and V_{DD2} most certainly are not. We can assume that the noise voltages at each on of these three nodes correspond to the noise of 50-Ohm resistors, so the single-sided noise spectral density in each node is $S_0(f)=4kT\,R=200kT$.

And guess what? **All transistors are noisy** too, but we limit the exercise to only consider their thermal noise. So, you have in total six noise sources in this small circuit.

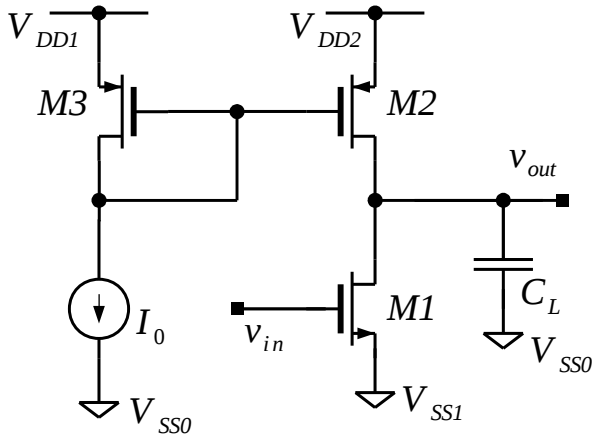

Figure 3.1: A simple (?) circuit.

Calculate the output- and input-referred noise spectral densities!

Elaborate on how you could maximize the signal-to-noise power ratio (SNR) at the output. Assume that the **output signal** swings from ground to supply and has a frequency within the operating bandwidth of the circuit, i.e., disregard the fact that the transistors have to be saturated for a short moment in your life. The load capacitance, C_L, cannot be reduced.

- *Well, this exercise will show that you have understood ... errh ... noise?*
- *Tip: Use symmetries in the circuit to speed up your calculations! Identify what kind of amplifier stage you have for different noise source and use the symmetry.*

- *Tip: Use for example the brickwall noise bandwidth to find the total noise power.*
- *Don't forget to sanity check your results!*

4. HIGH-GAIN STAGES (OP/OTA) (5 P)

OK, so normally we want really high gain in our amplifiers, but why? For example, assume you want a closed-loop small-signal gain of two, $A_{CL}=2$, you could connect two resistors in a feedback configuration as shown in Figure 4.1 and then choose $R_0=2R_1$. (Ignore the inversion for now)

So, why don't you use an open-loop amplifier with a small-signal gain of two, $A_0=2$, instead? Or would you? Outline pros and cons for the two approaches.

Motivate your answer by comparing a single-ended output, two-stage amplifier using negative feedback as in Figure 4.1 with an open-loop common-source stage with $A_0=2$.

First, present and motivate a circuit solution for the low-gain common-source stage. With "motivate" we understand that you must show the schematic, clarify how transistor sizes, currents, DC operating points, and gain are related. Use first-order approximations. Notice that for low-gain stages, quite a few parameters are dependent on eachother and can be used to derive compact formulas.

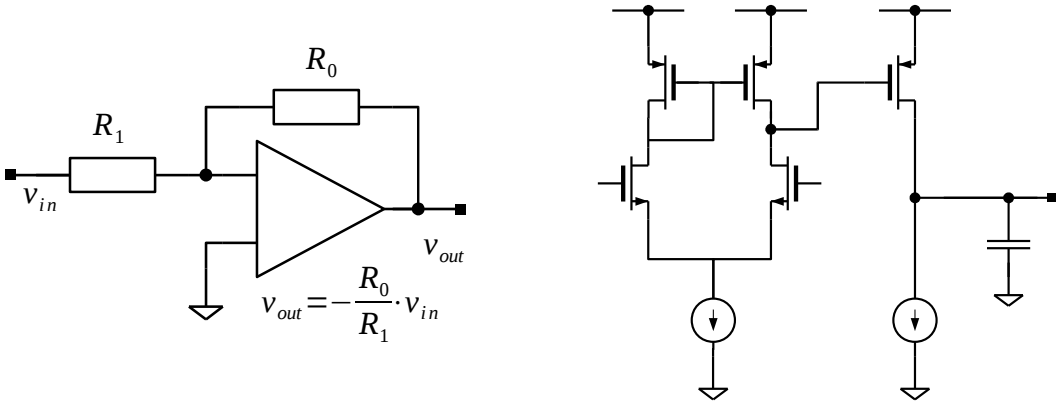

Figure 4.1: Closed-loop gain configuration and a two-stage amplifier.

Then, touch on two items such as for example: input and output range (IR, CMR, OR), speed (p_1, ω_{ug}), gain (A_0 vs A_{CL}), phase margin, sensitivity (mismatch, PSRR), driving capability (I, SR), linearity (THD), noise, power consumption, etc.

✗ *Notice! As stated you do not have to cover all items above for maximum point, pick two that illustrate differences between the two types of amplifiers and motivate which one of the two amplifiers is most suitable w.r.t. to that item. Tip: quite a few of the motivations are found in the*

course literature!

- ✗ *Don't just answer: SR is higher for amplifier B. Motivate why!!!*
- ✗ *Don't forget the motivation of your multiply-by-two open-loop circuit!*
- ✗ *In short: show that you understand the fundamental basics of analog building blocks!*

5. SWITCHED CAPACITOR CIRCUITS (5 P)

✗ Whew! Finally... the last question (this time...).

A Ph.D. student at our department is currently looking at high-speed switched-capacitor circuit. Now you will help him out a bit...

Consider the circuit in Figure 5.1 where you have an input signal, v_{in}, two capacitors, C_{in} and C_{out}, two non-overlapping clock phases, ϕ_1 and ϕ_2. The buffer is ideal and is connected in a negative feedback configuration achieving unity gain. The switches operate at the sample frequency $f_s=1/T$. For now we assume that the switches are ideal too and that the input is driven by an ideal source.

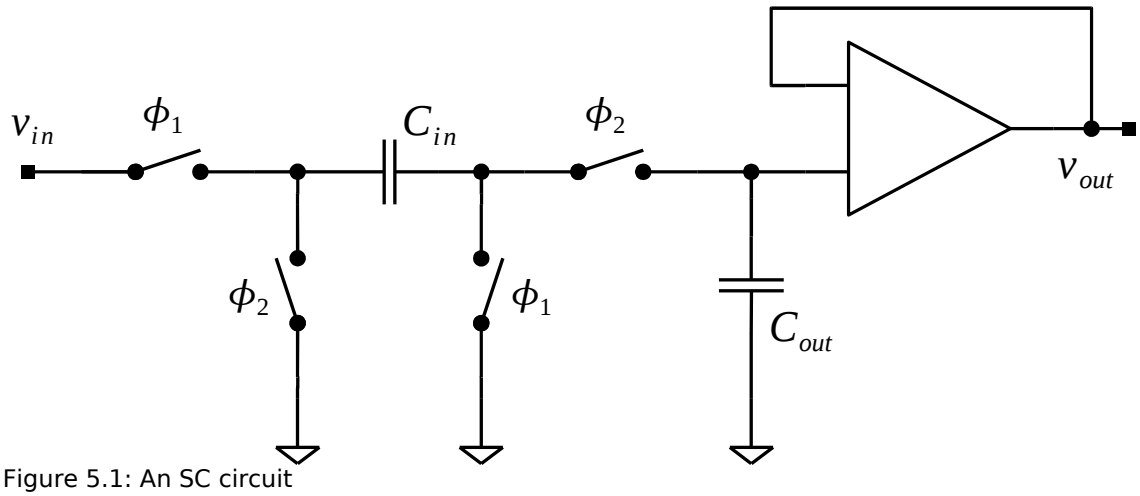

Figure 5.1: An SC circuit

Derive the transfer function from input to output in a discrete-time sense, i.e., how relates $v_{out}(nT)$ and $V_{out}(z)$ to $v_{in}(nT)$ and $V_{in}(z)$. Express the transfer function in the z-domain, i.e. $H(z)$ where z refers to the sample period as $z=e^{j\omega T}$.

Assume now that you have a spectrum analyzer measuring the continuous-time voltage, $v_{out}(t)$, **sketch the transfer function in the frequency domain**. **NOT IN THE SAMPLED DOMAIN!** Clearly identify power levels, frequencies, etc. **What is the DC gain?**

What kind of circuit is this? Elaborate on how the transfer function changes with the ratio of C_{in}/C_{out} and then explain **if the circuit is sensitive to parasitics or not?**

✗ Show that you after four years at the University have understood the concepts of sampled signals and the relationship between continuous-time and discrete-time frequency domains.

✗ *Once again! Don't be overwhelmed by the size of the exercise. Any (reasonable) try to answer the question can give you credit!*