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11.7 PROBLEMS

11.1 For an ideal 10-bit, unipolar D/A converter with $V_{LSB} = 1$ mV, what is the largest output voltage?

11.2 What is the SNR for an ideal 12-bit unipolar A/D converter with $V_{ref} = 3$ V, when a sinusoidal input of 1 V_{pp} is applied? What size input would result in an SNR of 0 dB?

11.3 Find the equivalent of (11.19) for 2's-complement coding.

11.4 Show that, by using 4-bit 2's-complement words, the correct final sum is obtained when the numbers +5, +5, and –7 are added together while any overflow effects are ignored.

11.5 Starting with two 4-bit 2's-complement words, we want to add +5 and +7 to obtain the correct answer of +12 with a 5-bit word. Show how an extra bit can be added at the left of each of the 4-bit words such that numbers up to ±15 can be represented. This approach is called *sign extension* and can be used to increase the word size of any number.

11.6 What is the representation of +8 and –8 in 5-bit 2's complement? Assuming a circuit added only one of these two numbers to an arbitrary 5-bit word, show a simple logic circuit (i.e., nand, nor, xnor, etc.) that would accomplish such an addition. (*Hint:* Note that the 4 LSBs in +8 and –8 are all 0 and thus do not need to be added.)

11.7 The following measurements are found from a 3-bit unipolar D/A converter with $V_{ref} = 8$ V: (–0.01, 1.03, 2.02, 2.96, 3.95, 5.02, 6.00, 7.08). In units of LSBs, find the offset error, gain error, maximum DNL, and maximum INL.

11.8 How many bits of absolute accuracy does the converter in Problem 11.7 have? How many bits of relative accuracy does it have?

11.9 A 10-bit A/D converter has a reference voltage, V_{ref}, tuned to 10.24 V at 25 °C. Find the maximum allowable temperature coefficient in terms of $(\mu V)/°C$ for the reference voltage if the reference voltage is allowed to cause a maximum error of $(\pm 1/2)$ LSB over the temperature range of 0 to 50 °C.

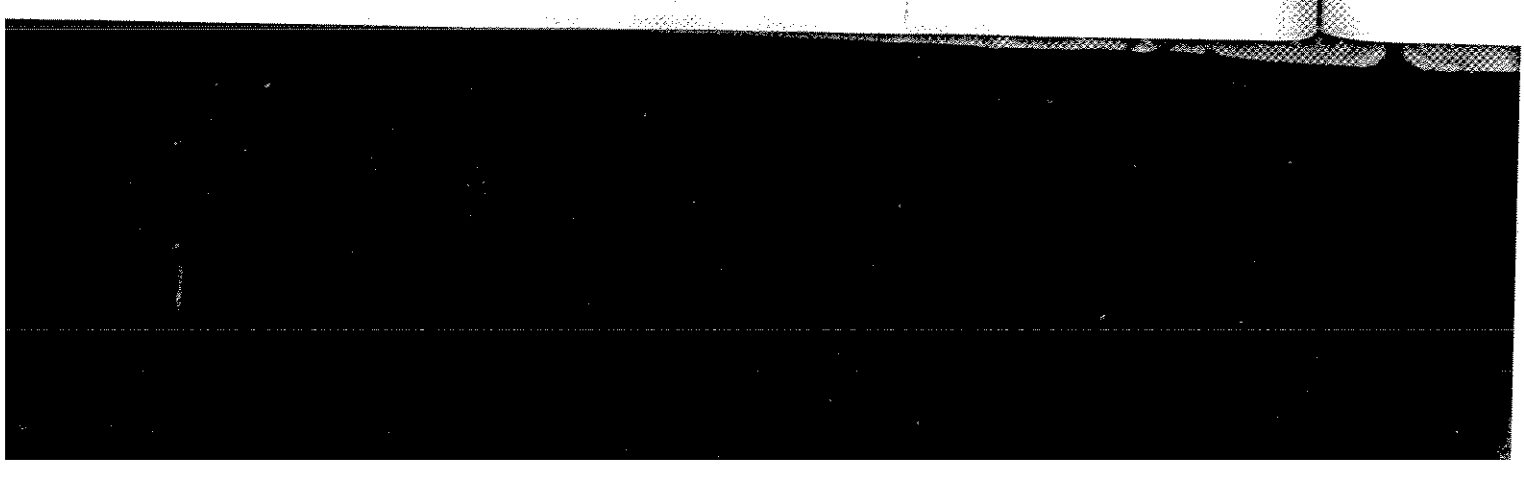
11.10 Consider the following measured voltage values for a 2-bit D/A with a reference voltage of 4 V:

$$\{00 \leftrightarrow 0.01 \text{ V}\} \quad \{01 \leftrightarrow 1.02 \text{ V}\} \quad \{10 \leftrightarrow 1.97 \text{ V}\} \quad \{11 \leftrightarrow 3.02 \text{ V}\}$$

In units of LSB, find the offset error, gain error, worst absolute and relative accuracies, and worst differential nonlinearity. Restate the relative accuracy in terms of an N-bit accuracy.

11.11 Find the maximum magnitude of quantization error for a 12-bit A/D converter having V_{ref} equal to 5 V and 0.5-LSB absolute accuracy.

11.12 What sampling-time uncertainty can be tolerated for a 16-bit A/D converter operating on an input signal from 0–20 kHz ?



segment is diverted where it is divided into binary-weighted currents, which are also switched to either ground or the output. Although this four-LSB segment is not guaranteed to be monotonic, its accuracy requirements are very relaxed, since it is used only for the LSBs.

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12.6 PROBLEMS

12.1 Derive an expression for the number of switches in a general N-bit resistor-string D/A converter similar to that shown in Fig. 12.1.

12.2 Assume that an 8-bit resistor-string D/A converter with digital decoding (see Fig. 12.3) has a total resistor-string resistance of 400 Ω, that its pass transistors have an on resistance of 400 Ω, and that the drain-source capacitances to

ground of its pass transistors are 0.1 pF. Ignoring all other effects and using the open-circuit time-constant approach, estimate the worst-case settling time to 0.1 percent.

12.3 Derive an expression for the number of switches in an N-bit folded resistor-string D/A converter similar to that shown in Fig. 12.4 (Assume N is even).

12.4 Assume that the first resistor string of a 10-bit multiple-R-string D/A converter must match to 0.1 percent whereas the second string must match to 1.6 percent since the converters realize the top 4 bits and lower 6 bits, respectively. For $V_{ref} = 5$ V, how much offsets in the opamps can be tolerated?

12.5 For a binary-weighted 10-bit resistor D/A converter (see Fig. 12.7), assume that R_F is chosen such that the output goes from 0 to $V_{ref} - V_{LSB}$. What is the resistor ratio between the largest and smallest resistors? What is the ratio between the currents through the switches for b_1 and b_{10}?

12.6 It is desired to realize a binary-weighted 4-bit resistor D/A converter, as shown in Fig. 12.7, that must be linear to 10 bits. Ignoring all other nonidealities except for resistance mismatch error, what percentage matching accuracy is required for each of the $b_2 - b_4$ resistors relative to the b_1 resistor?

12.7 Consider an 8-bit D/A converter built using binary-weighted capacitors, where capacitor tolerances are ±0.5 percent. What would be the worst-case differential nonlinearity in units of LSBs, and at what transition does it occur?

12.8 Consider the reduced-resistance-ratio approach shown in Fig. 12.8, where a single series resistor is applied to an N-bit converter, and where N is an even number. What is the improvement in the resistance ratio compared to using all binary-scaled resistances?

12.9 Draw the circuit for a reduced-resistance-ratio 8-bit D/A converter (see Fig. 12.8), where a resistor is inserted between b_4 and b_5. Ignoring R_F, what is the resistance spread? Now draw a similar circuit, but add resistors between b_2 and b_3 as well as between b_6 and b_7. What is this circuit's resistance spread?

12.10 Assuming all the switches in Fig. P12.10 are MOSFETS and are scaled so that each has 100 mV across the drain source when on (including s_4, which always remains on), show that no accuracy is lost.

12.11 For the 4-bit R-2R-ladder D/A converter shown in Fig. P12.10, what is the output error (in LSBs) when $R_A = 2.01R_B$? What is the output error when $R_C = 2.01R$?

12.12 Show that the D/A converter circuit shown in Fig. 12.11 operates correctly. Estimate the speed of this circuit if the opamp has infinite bandwidth, $R = 10$ kΩ, and all nodes have a capacitance of 0.5 pF to ground.

12.13 Consider the D/A converter shown in Fig. 12.11, where $I = 1$ mA, $R_f = 2$ kΩ and $R = 10$ kΩ. If this converter is perfectly linear but is found to have an offset error of 0.15LSB and a gain error of 0.2LSB, find the output levels for the inputs $b_1b_2b_3b_4$ equal to 0000, 1000, and 1111.

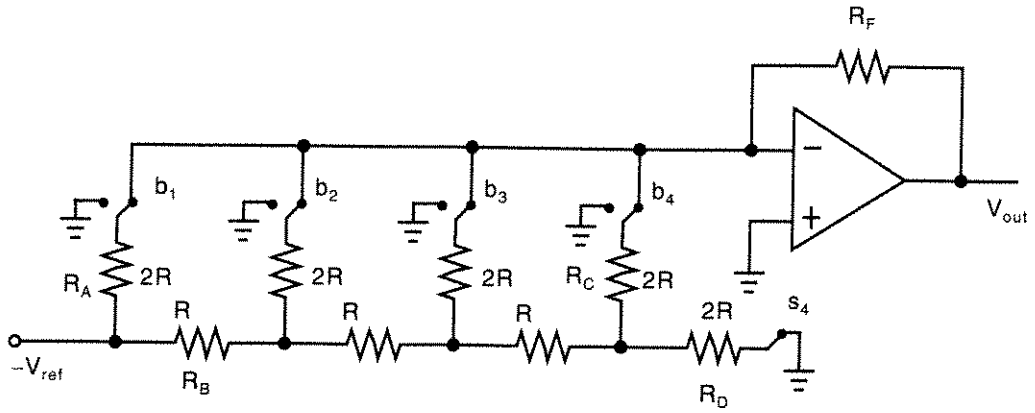

Fig. P12.10

12.14 A 12-bit binary-weighted D/A converter produces a glitch voltage of 0.5 V when the MSB is changed. What is the glitch voltage reduced to if a thermometer-code approach is used for the top 4 bits, whereas binary-weighting is used for the remaining 8 bits?

12.15 For the circuit in Fig. 12.17, sketch a typical waveform that would occur on the node connecting Q_1, Q_2, and Q_3 when the code signals, d_i and $\overline{d}_i$, are nonoverlapping. Repeat this sketch if the code signals are overlapping. Assume the code signals have logic swings from 0 to –5 V and that the threshold voltage for the transistors equals 1 V.

12.16 For the circuit in Fig. 12.18, sketch a typical waveform that would occur on the node connecting Q_1, Q_2, and Q_3 when the code signal, d_i, goes low-to-high and high-to-low. Assume here that the code signal has a logic swing of 0 to 5 V, that the threshold voltage for the transistors equals –1 V, and that V_{bias} is 1 V.

12.17 A D/A converter is realized using dynamically matched current sources, as shown in Fig. 12.20. Assuming all the transistors are ideal, find W/L for the Q_1 needed to set $V_{GS} = 3$ V when $I_{ref} = 50\ \mu A$, $V_t = 1$ V, and $\mu_n C_{ox} = 92\ \mu A/V^2$. If switch S_1 causes a random charge injection voltage of 1 mV, what is the expected percentage of random variation of the current being held on Q_1?

12.18 Repeat Problem 12.17 if the design does not incorporate the $0.9I_{ref}$ extra current source (i.e., if Q_1 must be the source for all of I_{ref}).

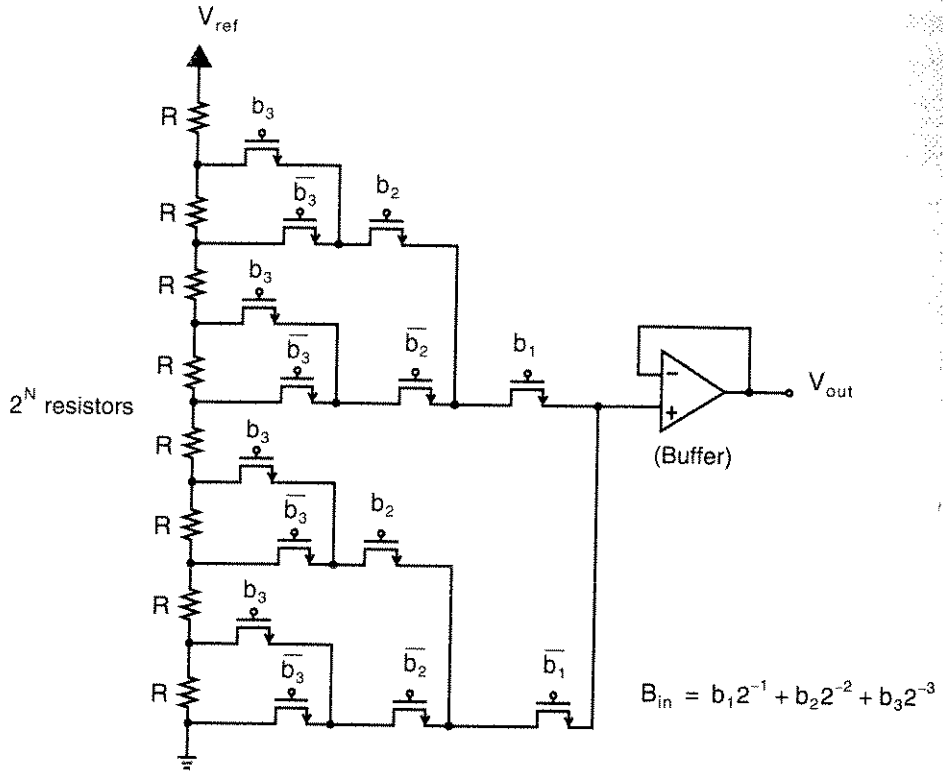

Fig. 12.1 Resistor-string 3-bit D/A converter with a transmission-gate, tree-like decoder.

With a resistor-string approach, if we assume the buffer's offset voltage does not depend on its input voltage, the D/A converter has guaranteed monotonicity since any tap on the resistor string must have a lower voltage than its upper, neighbor tap. Also, the accuracy of this D/A depends on the matching precision of R in the resistor string. Although this resistor-matching precision depends on the type of resistors used, the use of polysilicon resistors that have a resistivity of around 20–30 (ohms per square) can result in up to 10 bits of accuracy.

The delay through the switch network is the major limitation on speed. However, in a multiplying D/A, the delay through the resistor string would also be a major source of delay since V_{ref} would become a second input signal. A useful technique for estimating the settling-time behavior in RC type circuits (i.e., circuits that have only real-axis poles) is the *open-circuit time-constant* approach [Sedra, 1991]. Specifically, the dominant high-frequency time constant is estimated as the sum of the individual time constants due to each of the capacitances when all other capacitances are set to zero (i.e., replaced with open circuits). To find the individual time constant for a given capacitance, independent voltage sources are replaced with ground (independent current sources are opened), and the resistance seen by that capacitor is determined.

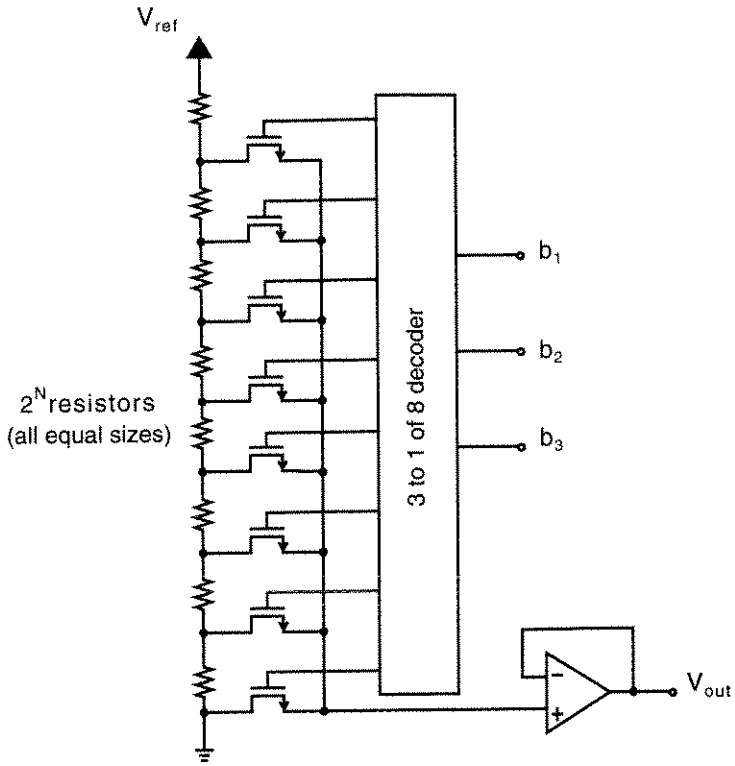

Fig. 12.3 Resistor-string 3-bit D/A converter with digital decoding.

Folded Resistor-String Converters

To reduce the amount of digital decoding and large capacitive loading, a *folded resistor-string D/A* can be used, as shown in Fig. 12.4 [Abrial, 1988]. This approach makes the decoding very similar to that for a digital memory, which reduces the total decoding area. To convert a digital input in this 4-bit example, the most significant bits, $\{b_1, b_2\}$, determine the single word line to be selected (all others will remain low). This operation connects a block of four adjacent resistor nodes to the four-bit lines. One of these bit lines is then connected to the output buffer by the bit-line decoder. Notice that the total number of transistor junctions on the output line is now $2\sqrt{2^N}$ because a set of transistors is connected directly to the output line and another set is connected to the chosen bit line. Thus, for a 10-bit converter, this approach would have a capacitive load of 64 junctions, as opposed to 1,024 junctions when we use the digital-decoding approach shown in Fig. 12.3. Unfortunately, the increase in speed is not equal to this large ratio since, when a word line goes high, all the bit lines must be pulled to new voltage levels—not just the one bit line connected to the output buffer.

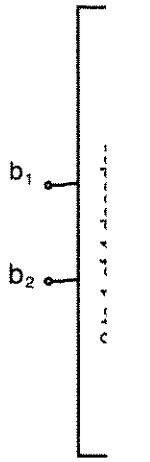

Fig. 12.4

Multiple

Binary-Weighted Resistor Converters

Binary-weighted resistor converters are popular for a bipolar technology so that bipolar differential pairs can be used for current switches. The basic architecture for a 4-bit converter is shown in Fig. 12.7.

If b_i is a 1, then the current to the ith resistor comes from the virtual ground of the opamp; otherwise, it comes from ground. Therefore, we have

$$V_{out} = -R_F V_{ref}\left(-\frac{b_1}{2R} - \frac{b_2}{4R} - \frac{b_3}{8R} - \cdots\right) = \left(\frac{R_F}{R}V_{ref}\right)B_{in} \tag{12.2}$$

where

$$B_{in} = b_1 2^{-1} + b_2 2^{-2} + b_3 2^{-3} + \cdots \tag{12.3}$$

Although this approach does not require many resistors or switches, it does have some disadvantages. The resistor and current ratios are on the order of 2^N, which may be large, depending on N. This large current ratio requires that the switches also be scaled so that equal voltage drops appear across them for widely varying current levels. Also, monotonicity is not guaranteed. Finally, this approach is prone to glitches for high-speed operation, as discussed on page 474.

Reduced-Resistance-Ratio Ladders

To reduce the large resistor ratios in a binary-weighted array, signals in portions of the array can be scaled by introducing a series resistor, as shown in Fig. 12.8. Here, note that the voltage node, V_A, is equal to one-fourth the reference voltage, V_{ref}, as a result of inserting the series resistor of value 3R. Also note that an additional 4R resistor was added (to ground) such that resistance seen to the right of the 3R resistor equals

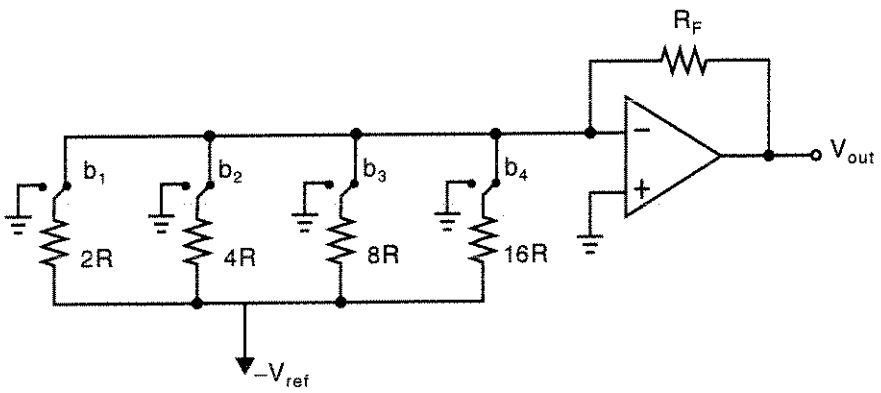

Fig. 12.7 Binary-weighted 4-bit resistor D/A converter.

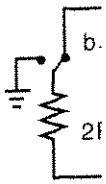

Fig. 12.8

R-2R-B

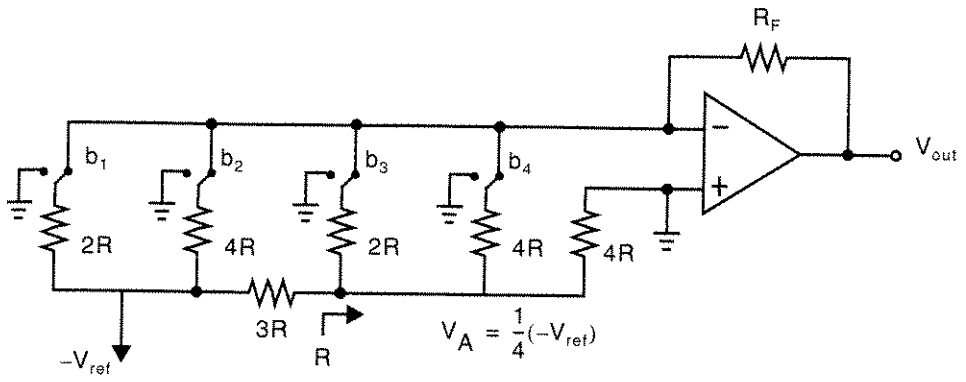

Fig. 12.8 Reduced-resistance-ratio 4-bit D/A converter.

R. Straightforward analysis shows that this converter has the same relationship to the binary digital signals as in the previous binary-weighted case, but with one-fourth the resistance ratio. Note, however, the current ratio has remained unchanged. Finally, note that, by repeating this procedure recursively to a binary-weighted ladder, one arrives at a structure commonly referred to as an *R-2R ladder,* described next.

R-2R-Based Converters

A very popular architecture for D/A converters uses R-2R ladders. These ladders are useful for realizing binary-weighted currents with a small number of components and with a resistance ratio of only 2, independent of the number of bits, N.

Consider the R-2R ladder network shown in Fig. 12.9. Analysis gives

$$\begin{aligned} R_4' &= 2R \\ R_4 &= 2R \parallel 2R = R \\ R_3' &= R + R_4 = 2R \\ R_3 &= 2R \parallel R_3' = R \end{aligned} \tag{12.4}$$

and so on. Thus, $R_i' = 2R$ for all i. This result gives the following current relationships:

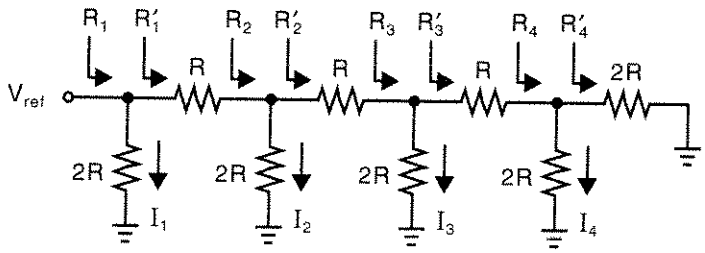

Fig. 12.9 R-2R resistance ladder.

of the R-2R ladder now exhibit some voltage swings (as opposed to the configuration in Fig. 12.10 where internal nodes all remain at fixed voltages).

Charge-Redistribution Switched-Capacitor Converters

The basic idea here is to simply replace the input capacitor of an SC gain amplifier by a *programmable capacitor array* (PCA) of binary-weighted capacitors, as shown in Fig. 12.12. As in the SC gain amplifier, the shown circuit is insensitive to opamp input-offset voltage, 1/f noise, and finite-amplifier gain. Also, an additional sign bit can be realized by interchanging the clock phases (shown in parentheses) for the input switches.

It should be mentioned here that, as in the SC gain amplifier, carefully generated clock waveforms are required to minimize the voltage dependency of clock feedthrough, and a deglitching capacitor should be used. Also, the digital codes should be

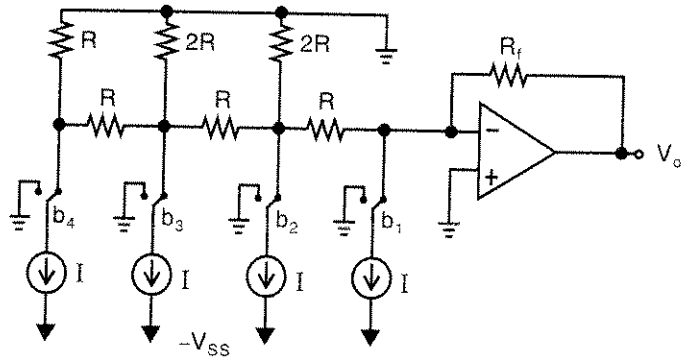

Fig. 12.11 R-2R ladder D/A converter with equal currents through the switches.

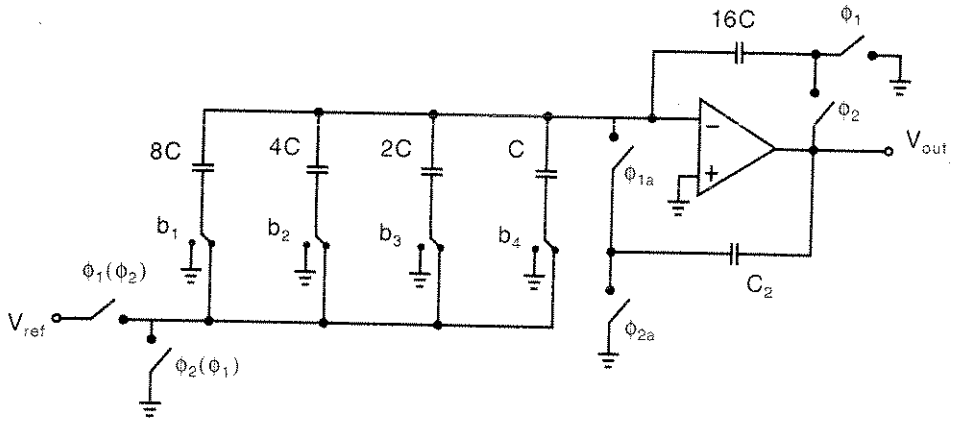

Fig. 12.12 Binary-array charge-redistribution D/A converter.

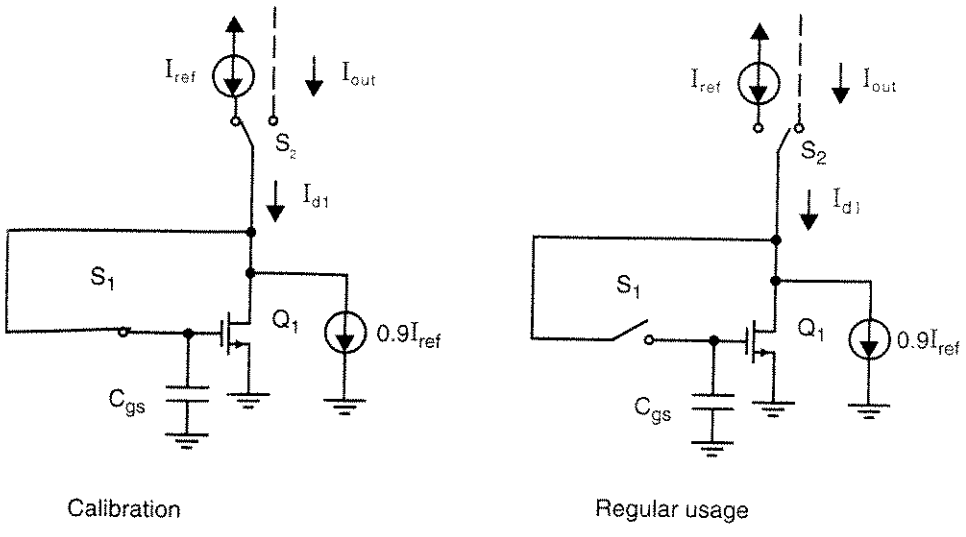

Fig. 12.20 Dynamically setting a current source, I_{d1}.

by 0.5LSB. Fortunately, having a large C_{GS} and V_{GS} has the added benefit of extending this calibration interval (every 1.7 ms in [Schouwenaars, 1988]).

Many other additional details are described in [Schouwenaars, 1988]. For example, during calibration, a p-channel-input common-gate amplifier is added to the diode-connected loop. This is typically done in dynamic switched-current circuits to control the drain-source voltage of Q_1 (i.e., to keep it constant independent of the actual current and to keep it matched to its value during regular use) and to speed up the circuit by decreasing the effect of parasitic capacitances on the large I_{ref} bus. Also, dummy switches are connected to S_1 to help minimize clock feedthrough by partially cancelling the charge injected.

The converter in [Schouwenaars, 1988] achieves 0.0025 percent distortion, 92 dB S/(N+D), 94 db S/N, and only dissipated 20 mW. The converter could also be run using only a 3-V power supply. The clocking frequency is limited to 44 kHz by the digital audio application. No mention is made on the upper limit of the clocking frequency.

12.4 HYBRID CONVERTERS

Combining the techniques discussed in Sections 12.1–12.3 for realizing different portions of a D/A converter results in hybrid designs. Hybrid designs are an extremely popular approach for designing converters because they combine the advantages of different approaches. For example, it is quite common to use a thermometer-code approach for the top few MSBs while using a binary-scaled technique for the lower LSBs. In this way, glitching is significantly reduced and accuracy is high for the MSB where it is needed most. However, in the LSBs where glitching and accuracy requirements are much reduced, valuable circuit area is saved with a binary-scaled approach. This section discusses some useful hybrid designs.

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13.11 PROBLEMS

13.1 What is the worst-case conversion time for an 18-bit dual-slope integrating A/D converter when the clock rate is 5 MHz?

13.2 Consider an 18-bit integrating A/D converter, as shown in Fig. 13.1, where V_{ref} equals 10 volts, $C_1 = 100$ pF, and a clock frequency of 1 MHz is used. What value of R_1 should be chosen such that the opamp output never exceeds 10 volts when $0 \text{ V} < V_{in} < 10 \text{ V}$?

13.3 Derive the equivalent of (13.8) for Fig. 13.1 when the opamp has an input-offset voltage of V_{off1} and the comparator has an input-offset voltage of V_{off2}.

13.4 What is the offset error (in LSBs) of the converter described in Problem 13.2 when the integrating opamp has an input-offset voltage of 20 mV?

13.5 What input-signal frequencies are completely attenuated by a dual-slope 16-bit integrating A/D having a clock frequency of 1 MHz ? For this same converter, what is the attenuation of an input signal at 60 Hz ?

13.6 Repeat Problem 13.5 with the converter's clock frequency being equal to 100 kHz.

13.7 Consider a 4-bit unipolar DAC-based successive-approximation A/D converter, as shown in Fig. 13.5. Find the sequence of the D/A converter's output levels for an input of 3.333 volts when $V_{ref} = 8$ V. What is the final digital output?

13.8 Consider a 4-bit unipolar charge-redistribution A/D converter, as shown in Fig. 13.7, where $V_{ref} = 8$ V. Find the sequence of the voltage level for V_x if the input signal is 3.333 volts.

13.9 Repeat Problem 13.8, assuming that a parasitic capacitance of 8 C is connected between the node at V_x and ground. Is the final digital result affected?

13.10 Show a method for modifying the unipolar charge-redistribution A/D converter shown in Fig. 13.7 such that the threshold offsets of $0.5V_{LSB}$ are correctly realized.

13.11 How is the digital code obtained from the signed charge redistribution A/D converter shown in Fig. 13.8 converted to a 2's complement code?

13.12 What value of error voltage V_{x1} would be measured in Fig. 13.11(*a*) if the total array capacitance equals 64 pF, the MSB (i.e., b_1) capacitor equals 31.5 pF, and there is a parasitic capacitance to ground of 10 pF on node V_x? For the same circuit, show that the error voltage, V_{e1}, that occurs when using the MSB capacitor during a normal conversion equals $0.5V_{x1}$.

13.13 For the same circuit as described in Problem 13.12, what value of error voltage V_{x2} would be measured in Fig. 13.11(*b*) if the MSB-1 (i.e., b_2) capacitor equals 16.4 pF? Show that the error voltage, V_{e2}, that occurs when using the MSB-1 capacitor during a normal conversion equals $0.5(V_{x2} - V_{e1})$.

13.14 Assuming switch resistances are all about 1 kΩ, estimate the settling time needed for a 12-bit charge-redistribution A/D converter where the total array capacitance equals 128 pF.

13.15 Draw a block diagram similar to that for Fig. 13.22 for a 10-bit two-step A/D converter where the first stage determines 4 bits. Indicate the accuracy needed in all the blocks.

13.16 Show that the circuit shown in Fig. 13.25 results in all time constants being equal when each of the latches has the same input capacitance and the amplifiers have zero output impedance.

13.17 Consider the clocked comparator shown in Fig. 13.18, where

$$\mu_n C_{ox} = 2\,\mu_p C_{ox} = 100\ \mu A/V^2$$

$$2\left(\frac{W}{L}\right)_n = \left(\frac{W}{L}\right)_p = 2$$

$$|V_{tn}| = |V_{tp}| = 1 \text{ V}$$

$$V_{DD} = 5 \text{ V}$$

and $V_{SS} = 0$ V

If the MOSFETS in the inverter are ideal except for each having a 100-kΩ output impedance when active, find the minimum differential input that will cause a 1-volt change (use a linear analysis). Assuming this minimum differential input corresponds to (1/2) LSB, what is the maximum number of bits that this comparator could determine in a flash A/D converter?

13.18 In Section 13.6, it was stated that the interpolated signals will have the correct threshold crossings if V_1 and V_2 in Fig. 13.24 are linear in the region $0.25 < V_{in} < 0.5$. In fact, this region is larger than what is actually necessary. What is the minimum region of V_{in} that V_1 and V_2 should be linear over?

13.19 Many very-high-speed A/D converters do not use a sample and hold since it would limit their speed, but instead allow the input signal to be applied to the array of comparators, which are all clocked "simultaneously." Qualitatively, explain why a clocked flash or interpolating A/D converter might operate faster than a sample-and-hold circuit.

13.20 In an N-bit folding A/D converter (with no interpolation), what is the product of the folding rate times the number of folding blocks?

13.21 Find an expression for the number of latches in an N-bit folding A/D converter where the folding rate is $FR = 2^F$.

13.22 Assuming the input capacitance of a differential stage is the same in either a flash or folding/interpolating A/D converter, what reduction of input capacitance over a flash converter would be achieved with an 8-bit folding/interpolating A/D converter having four folding blocks, each with a folding rate of eight? If a straight interpolating A/D converter is to have the same reduction in input capacitance, how many resistors are required between "input comparators"?

13.23 Draw the clock waveforms of the sample-and-hold circuits for the time-interleaved A/D converter shown in Fig. 13.34.

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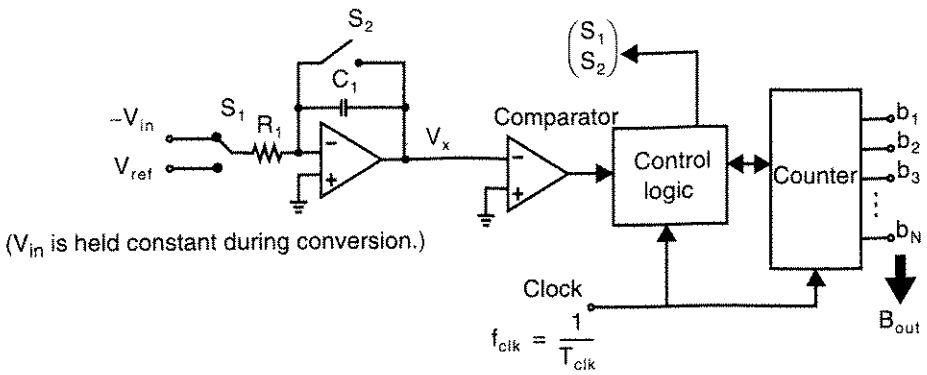

Fig. 13.1 Integrating (dual slope) A/D converter.

where T_{clk} is the period for one clock cycle. During this interval, switch S_1 is connected to $-V_{in}$ such that V_x ramps up proportional to the magnitude of V_{in}. Assuming V_x is initially equal to zero (due to a pulse on S_2), we have the following relationship for V_x:

$$V_x(t) = -\int_0^t \frac{(-V_{in})}{R_1C_1}\,d\tau = \frac{V_{in}}{R_1C_1}t \tag{13.2}$$

Thus, at the end of phase (I), the value of V_x is equal to $V_{in}T_1/R_1C_1$.

Phase (II) Phase (II) occurs for a variable amount of time, T_2, as shown in Fig. 13.2 for three different input voltages. At the beginning of this phase, the counter is reset and switch S_1 is connected to V_{ref}, resulting in a constant slope for the decaying voltage at V_x. To obtain the digital output value, the counter simply counts until V_x is less than zero, at which point that count value equals the digitized value of the input

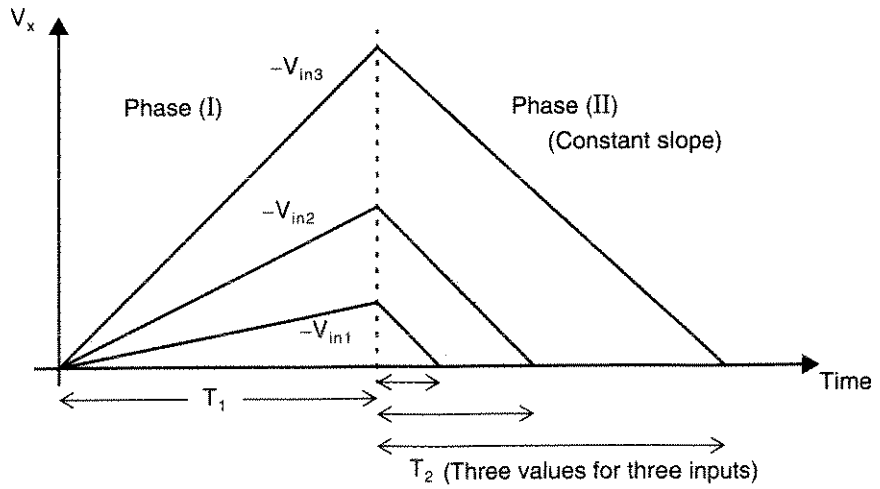

Fig. 13.2 Operation of the integrating converter for three different input voltages.

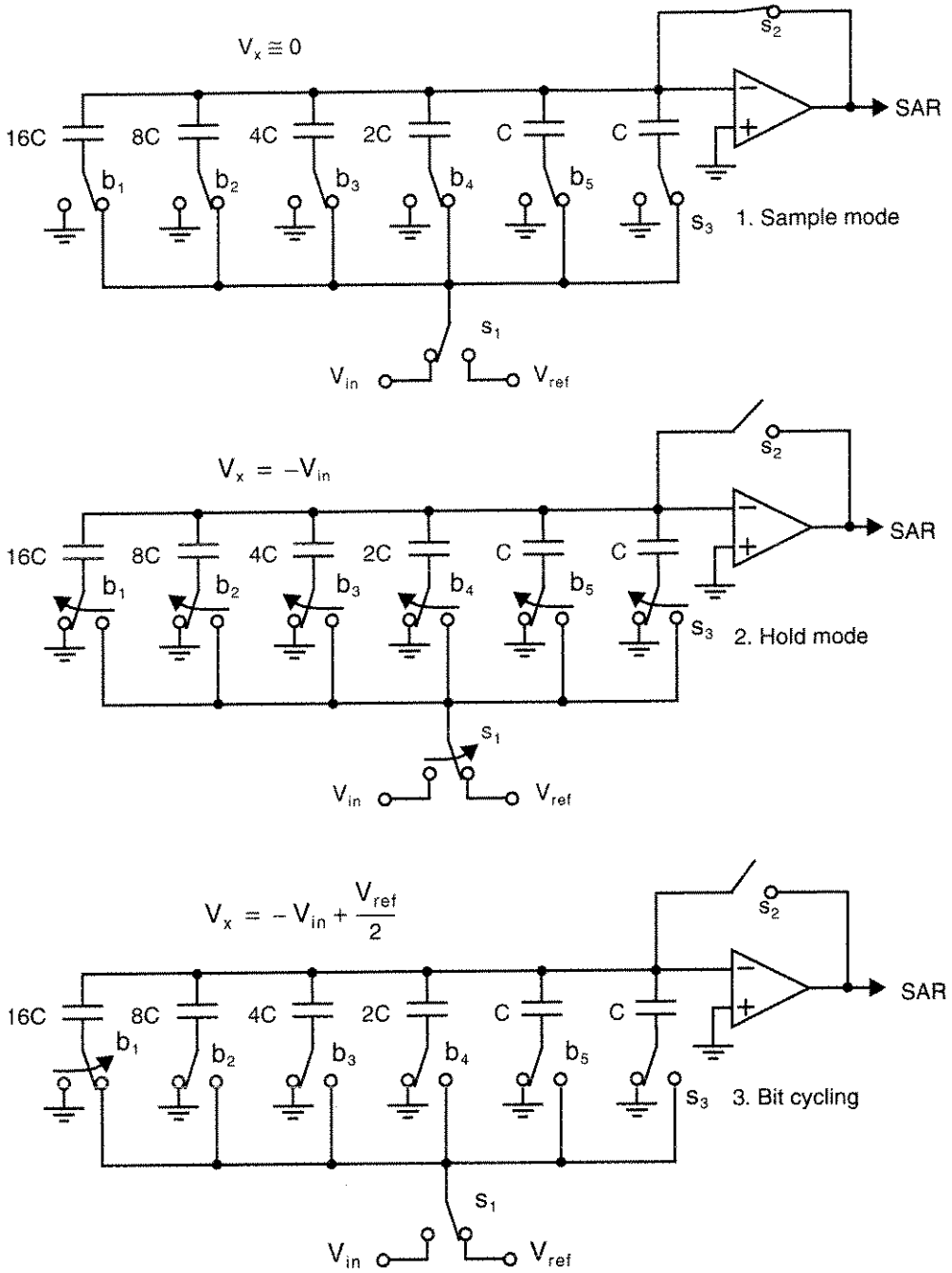

Fig. 13.7 A 5-bit unipolar charge-redistribution A/D converter.

cross talk, limited bandwidth, etc. These bubbles usually occur near the transition point of the thermometer code. Fortunately, these bubbles can usually be removed with little extra complexity by replacing the two-input NAND gates shown in Fig. 13.16 with three-input NAND gates, as shown as shown in Fig. 13.18 [Steyaert, 1993]. With this modification, there must now be two 1s immediately above a 0 in determining the transition point in the thermometer code. However, this circuit will not eliminate the problem of a stray 0 being two places away from the transition point, which may cause a large decoding error. Another digital approach for reducing the effect of bubble errors is to allow bubble errors in the lower 2 LSBs but have the remaining MSBs determined by looking for transitions between every *fourth* comparator [Gendai, 1991]. With this approach, bubble errors that occur within four places of the transition point do not cause any large errors. An alternate approach to reduce the effect of distant bubble errors is to create two encoders (one AND type and one OR type) rather than a single encoder [Ito, 1994]. When an unexpected output pattern occurs at the NAND outputs, the errors in two different encoders tend to be equal in magnitude but opposite in sign. Thus, the final output is taken as the average of the two encoder outputs, which is performed by adding the two outputs and dropping the LSB (to divide by two).

An alternate method to remove bubble errors that does not increase the power dissipation is shown in Fig. 13.19. Here, extra transistors have been added to the inputs of the slave latches, which are driven by the comparator master latches [van Valburg, 1992]. These extra transistors make the value stored in a slave latch not just a function of its master latch, but also a function of the two adjacent master latches. If a bubble occurs, the outputs from the two adjacent master latches are the same, but different from the center master latch. In this case, the values from the adjacent master latches overrule the center master latch. Note that with this approach, the power dissipation is not increased because the added transistors make use of existing current in the slave latch. Alternatively, this same voting scheme can be implemented entirely in digital form.

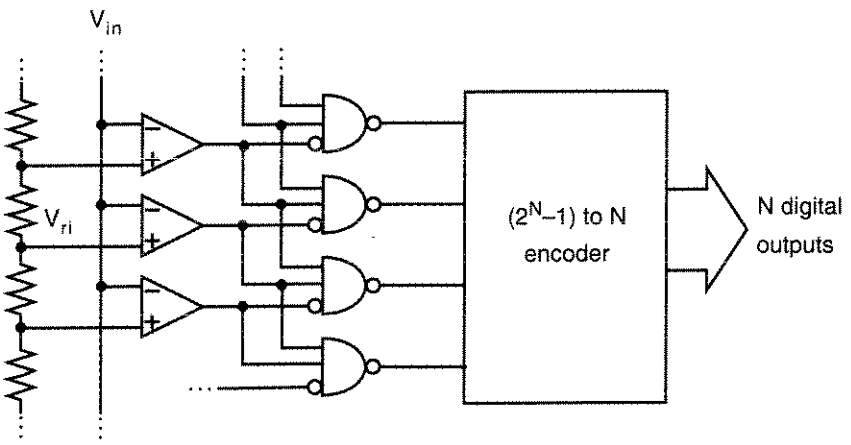

Fig. 13.18 Using three-input NAND gates to remove single bubble errors.

value from the input signal. To ease the requirements in the circuitry for finding the remaining LSBs, the quantization error is first multiplied by 16 using the gain amplifier, and the LSBs are determined using the 4-bit LSB A/D. With this approach, rather than requiring 256 comparators as in an 8-bit flash converter, only 32 comparators are required for a two-step A/D converter. However, this straightforward approach would require all components to be at least 8-bit accurate. To significantly ease the accuracy requirements of the 4-bit MSB A/D converter, digital error correction is commonly used and is discussed next.

Digital Error Correction

The block diagram for a two-step converter with digital error correction is shown in Fig. 13.22. Although the second sample and hold (S/H_2) is not necessary, its purpose is to allow the first S/H_1 to sample a new input signal before the gain amplifier has finished settling. However, the first S/H_1 is critical and its performance often limits the overall linearity. The reason for digital error correction is to significantly ease the requirements placed on the 4-bit MSB A/D converter. Without error correction, this first A/D converter needs to be at least 8-bit accurate. However, with error correction, the requirements on this MSB A/D converter are that it need only be 4-bit accurate. To see how this correction works and why a second-stage 5-bit converter is needed (rather than 4-bit), consider the quantization error that occurs in an ideal converter. Defining $V_{LSB} = V_{ref}/2^8$ (i.e., always relative to 8-bit accuracy), we have for an

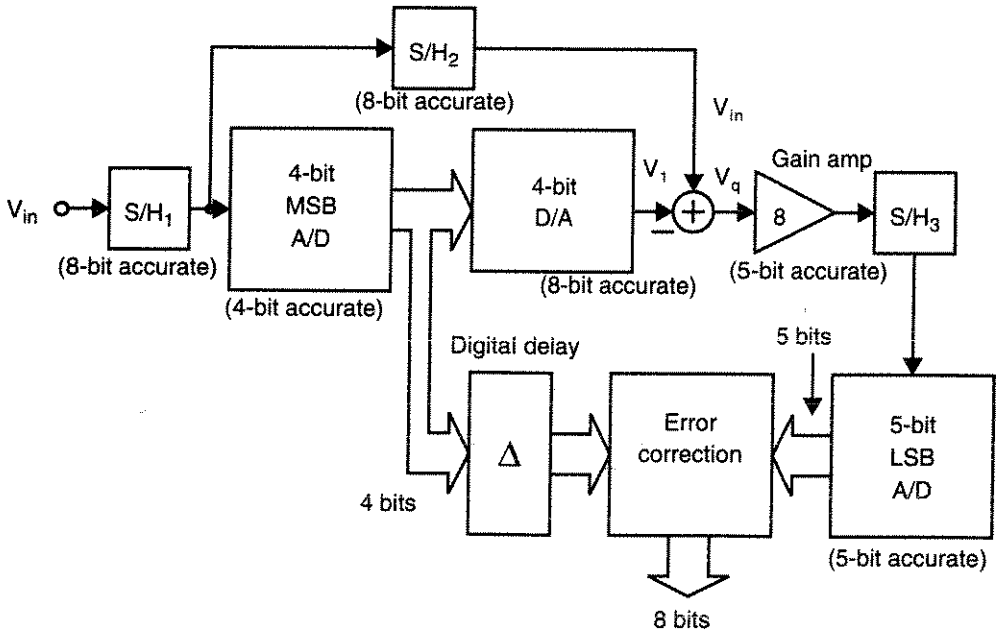

Fig. 13.22 An 8-bit two-step A/D converter with digital error correction.

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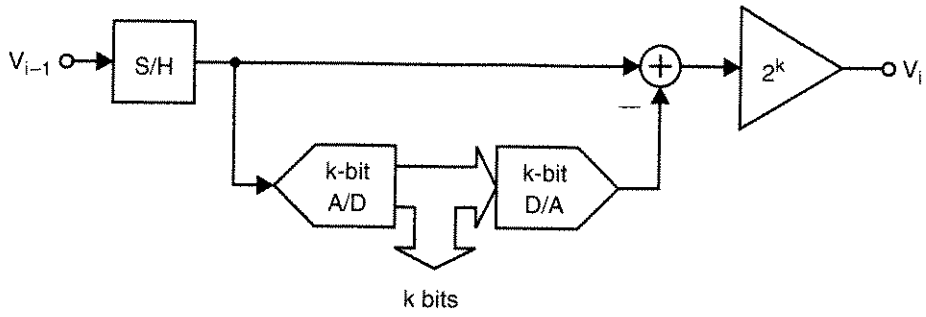

Fig. 13.33 A multi-bit digital approximator (DAPRX).

13.9 TIME-INTERLEAVED A/D CONVERTERS

Very-high-speed A/D conversions can be realized by operating many A/Ds in parallel [Black, 1980]. The system architecture for a four-channel A/D is shown in Fig. 13.34. Here, ϕ_0 is a clock at four times the rate of ϕ_1 to ϕ_4. Additionally, ϕ_1 to ϕ_4 are delayed with respect to each other by the period of ϕ_0, such that each converter will

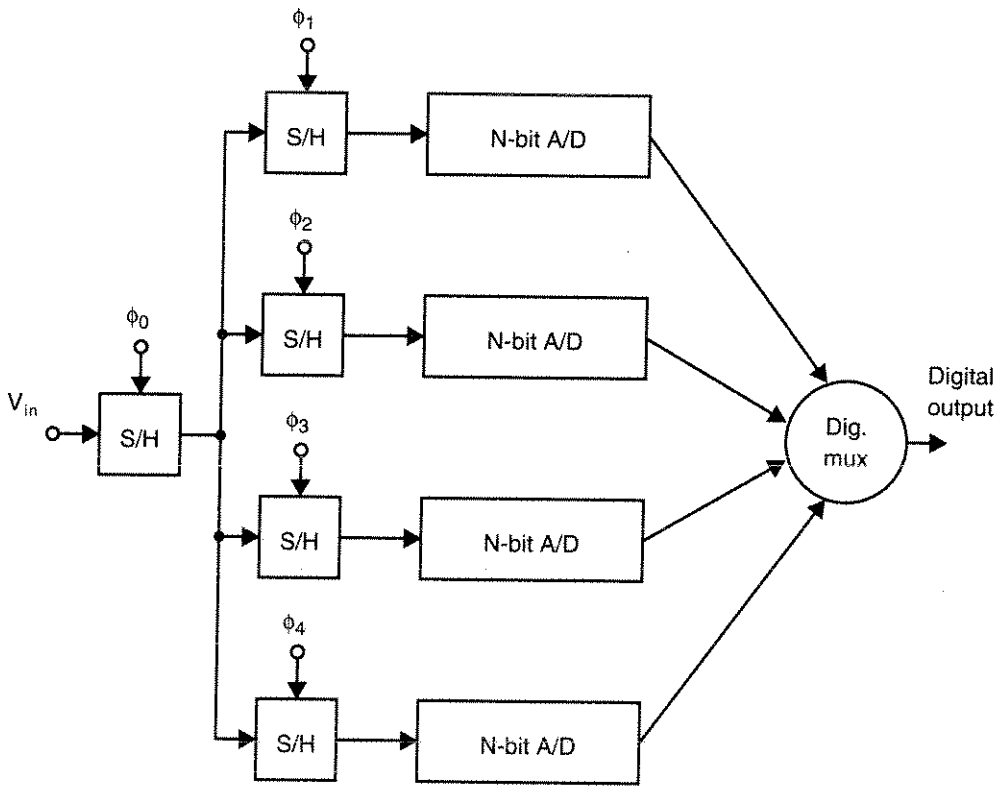

Fig. 13.34 A four-channel time-interleaved A/D converter.

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14.11 PROBLEMS

14.1 Assuming oversampling with no noise shaping and using (14.14), find the approximate sampling rate required to obtain a maximum SNR of 80 dB on a signal with a 1-kHz bandwidth using a 1-bit quantizer.

14.2 Repeat Example 14.4, except use a dc input level of $1.2/3$. At what frequency would a tone appear (relative to the sampling rate, f_s)?

14.3 Repeat Example 14.4, except use a dc input level of 1.1 to see if the internal state of the modulator saturates.

14.4 Repeat Example 14.4, except use an input sequence of $\{10, -10, 10, -10, 10, -10, \ldots\}$ to see if the internal state of the modulator saturates. This problem demonstrates that a large level input signal can be applied to a modulator if its signal power resides at a frequency where the gain of $H(z)$ is low.

14.5 Given that an 8-bit A/D converter has a SNR of 50 dB but is linear to 12 bits, what is the sampling rate required to achieve 12 bits of accuracy using straight oversampling on a signal bandwidth of 1 MHz?

14.6 Repeat Problem 14.5, assuming that the 8-bit A/D converter is placed inside a first-order delta-sigma modulator. What is the sampling rate if a second-order modulator is used?

14.7 Repeat Problem 14.1, assuming a first-order modulator is used. What is the sampling rate if a second-order modulator is used?

14.8 Assuming a 1-bit output signal of ± 1 and a sinusoidal signal of ± 0.5 peak-to-peak, what is the ratio of the signal power to quantization noise power before any filtering is applied?

14.9 What does the block $G(z) - 1$ need to be in Fig. 14.13 in order that a second-order noise transfer function is realized equal to $(1 - z^{-1})^2$?

14.10 Show a switched-capacitor modulator so that the second-order modulator shown in Fig. 14.10 is realized.

14.11 Show that the sequence of $\{1, 1, -1, 1, 1, -1, 1, 1, -1, \ldots\}$ into a cascade of three integrators and differentiators shown in Fig. 14.19 gives the correct running average. Assume that the adders have infinite width and that $M = 4$.

14.12 At first glance, the impulse response of a running average filter of length 4 is the same as that for a hold system that holds the input signal for length 4. By producing a block diagram for each system, explain the difference between the two systems.

14.13 Verify (14.42).

14.14 Show the block diagram for a MASH architecture that realizes third-order noise shaping using a second-order modulator (as shown in Fig. 14.10) and a first-order modulator.

14.15 Sketch the noise transfer function from 0 to 4 MHz for the second-order bandpass modulator shown in Fig. 14.23, assuming the sampling rate, f_s, equals 4 MHz.

14.16 Show how the block diagram in Fig. 14.23 can be modified so that the bandpass modulator places zeros at $\pm f_s/8$ rather than $\pm f_s/4$.

14.17 Using the "typical" waveform pattern shown in Fig. 14.24, find the practical average outputs when 0, $1/2$, and $-1/2$ have been applied to the first-order modulator shown in Fig. 14.7.

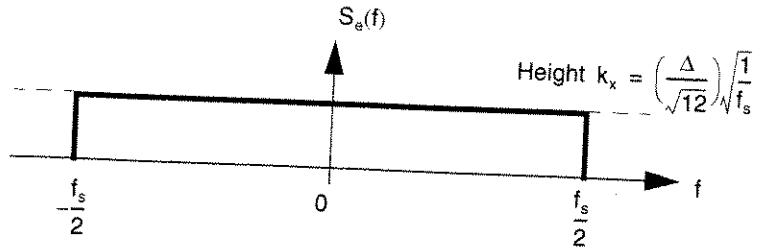


Fig. 14.2 Assumed spectral density of quantization noise.

$\pm f_s/2$, or mathematically,

$$\int_{-f_s/2}^{f_s/2} S_e^2(f)\,df = \int_{-f_s/2}^{f_s/2} k_x^2\,df = k_x^2 f_s = \frac{\Delta^2}{12} \tag{14.1}$$

Solving this relation gives

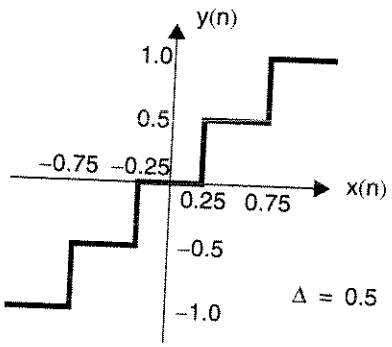
$$k_x = \left(\frac{\Delta}{\sqrt{12}}\right)\sqrt{\frac{1}{f_s}} \tag{14.2}$$

EXAMPLE 14.1

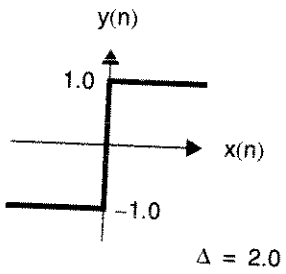
Find the output and quantization errors for two different quantizers, as shown in Fig. 14.3, when the input values are

$$x(n) = \{0.01, 0.31, -0.11, 0.80, 0.52, -0.70\} \tag{14.3}$$

Also find the expected power and the power density height, $S_e^2(f)$, of the quantization noise when the sampling frequency is normalized to 2π rad/sample.



Quantizer I
(Five-level quantizer)



Quantizer II
(Two-level quantizer)

Fig. 14.3 Two example quantizers.

EXAMPLE 14.3

Given that a 1-bit A/D converter has a 6-dB SNR, what sample rate is required using oversampling (no noise shaping) to obtain a 96-dB SNR (i.e., 16 bits) if $f_0 = 25$ kHz ? (Note that the input into the A/D converter has to be very active for the white-noise quantization model to be valid—a difficult arrangement when using a 1-bit quantizer with oversampling without noise shaping).

Solution

Oversampling (without noise shaping) gives 3 dB/octave where 1 octave implies doubling the sampling rate. We require 90 dB divided by 3 dB/octave , or 30 octaves. Thus, the required sampling rate, f_s, is

$$f_s = 2^{30} \times 2f_0 \cong 54{,}000 \text{ GHz !}$$

This example shows why noise shaping is needed to improve the SNR faster than 3 dB/octave , since 54,000 GHz is highly impractical.

The Advantage of 1-bit D/A Converters

While oversampling improves the signal-to-noise ratio, it does not improve linearity. For example, if a 16-bit linear converter is desired while using a 12-bit converter with oversampling, the 12-bit converter must have an integral nonlinearity error less than $1/2^4$ LSB (here, LSB refers to that for a 12-bit converter). In other words, the component accuracy would have to match better than 16-bit accuracy (i.e., $100 \times (1/2^{16}) = 0.0015$ percent accuracy). Thus, some sort of auto calibration or laser trimming must be used to obtain the required linearity. However, as we saw in Example 14.3, with a high enough sampling rate, the output from a 1-bit converter can be filtered to obtain the equivalent of a 16-bit converter. *The advantage of a 1-bit D/A is that it is inherently linear.*[2] This linearity is a result of a 1-bit D/A converter having only two output values and, since two points define a straight line, no trimming or calibration is required. This inherent linearity is one of the major motivations for making use of oversampling techniques with 1-bit converters. In fact, the reader may be aware that many audio converters presently use 1-bit converters for realizing 16- to 18-bit linear converters (with noise shaping). In addition, 20-bit linearity has been reported without the need for any trimming [Leopold, 1991]. Finally, it should be mentioned that there are other advantages when using oversampling techniques, such as a reduced requirement for analog anti-aliasing and smoothing filters.

2. This assumes that second-order errors due to imperfections such as signal-dependent power supply, or reference voltages, or memory in the D/A converter are not present.

result implies that the average value (i.e., dc value) of $u(n)$ must equal the average value (i.e., dc value) of $y(n)$.

Again, the similarity of this configuration and an opamp having unity-gain feedback is emphasized. The open-loop transfer function of an opamp is closely approximated by a first-order integrator having very large gain at low frequencies.

EXAMPLE 14.4

Find the output sequence and state values for a dc input, $u(n)$, of $1/3$ when a two-level quantizer of ± 1.0 is used (threshold at zero) and the initial state for $x(n)$ is 0.1.

Solution

The output sequence and state values are given in Table 14.2.

Table 14.2 First-order modulator example

n	x(n)	x(n + 1)	y(n)	e(n)
0	0.1	–0.5667	1.0	0.9
1	–0.5667	0.7667	–1.0	–0.4333
2	0.7667	0.1	1.0	0.2333
3	0.1	–0.5667	1.0	0.9
4	–0.5667	0.7667	–1.0	–0.4333
5	...	...	...	...

Note that the average of $y(n)$ exactly equals $1/3$ as expected. However, also note that the output pattern is periodic, which implies that the quantization noise is not random in this example. (However, the result is much more satisfying than applying $1/3$ directly into a 1-bit quantizer using straight oversampling, which would give all 1s as its output.)

Frequency Domain View From a frequency domain view, the signal transfer function, $S_{TF}(z)$, is given by

$$S_{TF}(z) = \frac{Y(z)}{U(z)} = \frac{1/(z-1)}{1+1/(z-1)} = z^{-1} \tag{14.19}$$

and the noise transfer function, $N_{TF}(z)$, is given by

$$N_{TF}(z) = \frac{Y(z)}{E(z)} = \frac{1}{1+1/(z-1)} = (1-z^{-1}) \tag{14.20}$$

We see here that the signal transfer function is simply a delay, while the noise transfer function is a discrete-time differentiator (i.e., a high-pass filter).

To find the magnitude of the noise transfer function, $|N_{TF}(f)|$, we let $z = e^{j\omega T} = e^{j2\pi f/f_s}$ and write the following:

Noise Transfer-Function Curves

The general shape of zero-, first-, and second-order noise-shaping curves are shown in Fig. 14.11. Note that over the band of interest (i.e., from 0 to f_0), the noise power decreases as the noise-shaping order increases. However, the out-of-band noise increases for the higher-order modulators.

EXAMPLE 14.5

Given that a 1-bit A/D converter has a 6-dB SNR, what sample rate is required to obtain a 96-dB SNR (or 16 bits) if $f_0 = 25$ kHZ for straight oversampling as well as first- and second-order noise shaping?

Solution

Oversampling with No Noise Shaping From before, straight oversampling requires a sampling rate of 54,000 GHz.

First-Order Noise Shaping First-order noise shaping gives 9 dB/octave where 1 octave is doubling the OSR. Since we lose 5 dB, we require 95 dB divided by 9 dB/octave, or 10.56 octaves. Thus, the required sampling rate, f_s, is

$$f_s = 2^{10.56} \times 2f_0 \cong 75 \text{ MHz}$$

This compares very favorably with straight oversampling, though it is still quite high.

Second-Order Noise Shaping Second-order noise shaping gives 15 dB/octave, but loses 13 dB. Thus we required 103 dB divided by 15 dB/octave, resulting in a required sampling rate of only 5.8 MHz. However, this simple calculation does not take into account the reduced input range for a second-order modulator needed for stability.

Quantization Noise Power of 1-bit Modulators

Assuming the output of a 1-bit modulator is ± 1, then one can immediately determine the total power of the output signal, $y(n)$, to be a normalized power of 1 watt. Since $y(n)$ consists of both signal and quantization noise, it is clear that the signal power can never be greater than 1 watt. In fact, as alluded to earlier, the signal level is often limited to well below the ± 1 level in higher-order modulators to maintain stability. For example, assuming that the maximum peak signal level is only ± 0.25, then the maximum signal power is 62.5 mW. And since the signal power plus quantization noise power equals 1 W, the maximum signal power is about 12 dB below

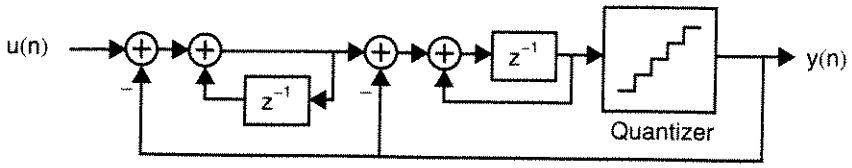


Fig. 14.10 Second-order ΔΣ modulator.

$$N_{TF}(f) = (1 - z^{-1})^2 \tag{14.28}$$

Additionally, the magnitude of the noise transfer function can be shown to be given by

$$|N_{TF}(f)| = \left[2 \sin\left(\frac{\pi f}{f_s}\right)\right]^2 \tag{14.29}$$

resulting in the quantization noise power over the frequency band of interest being given by

$$P_e \cong \frac{\Delta^2 \pi^4}{60}\left(\frac{1}{OSR}\right)^5 \tag{14.30}$$

Again, assuming the maximum signal power is that obtained in (14.11), the maximum SNR for this case is given by

$$SNR_{max} = 10 \log\left(\frac{P_s}{P_e}\right) = 10 \log\left(\frac{3}{2} 2^{2N}\right) + 10 \log\left[\frac{5}{\pi^4}(OSR)^5\right] \tag{14.31}$$

or, equivalently,

$$SNR_{max} = 6.02N + 1.76 - 12.9 + 50 \log(OSR) \tag{14.32}$$

We see here that doubling the OSR improves the SNR for a second-order modulator by 15 dB or, equivalently, a gain of 2.5 bits/octave.

The realization of the second-order modulator using switched-capacitor techniques is straightforward and is left as an exercise for the interested reader.

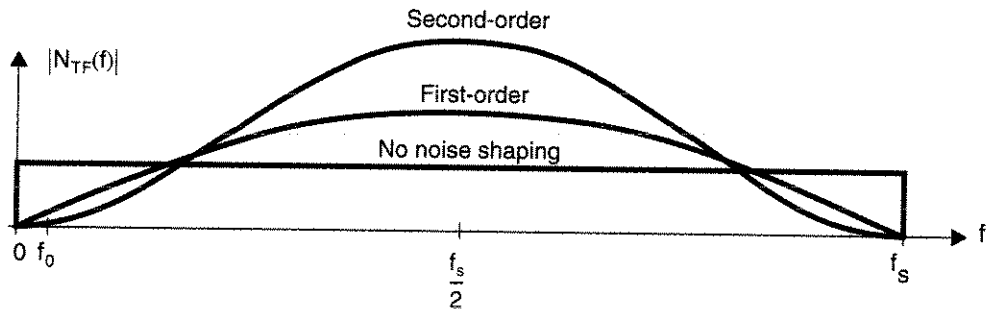


Fig. 14.11 Some different noise-shaping transfer functions.

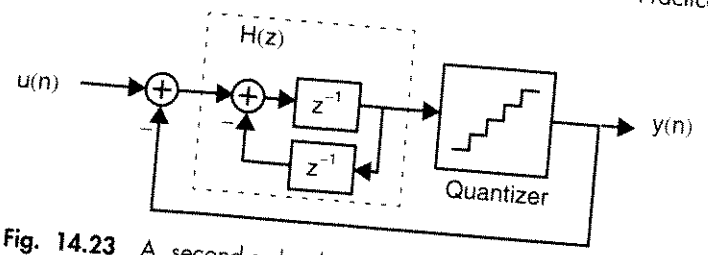


Fig. 14.23 A second-order bandpass oversampling modulator that shapes the quantization noise away from $f_s/4$.

Note that this second-order example has poles at $\pm j$, and therefore the noise transfer function, $N_{TF}(z)$, has only one zero at j and another zero at $-j$. For this reason, the dynamic range increase of a second-order bandpass converter equals that of a first-order low-pass converter that also has only one zero at dc. Specifically, the dynamic range increase of a second-order bandpass converter is 1.5 bits/octave or, equivalently, 9 dB/octave. To obtain the equivalent dynamic range increase of a second-order low-pass converter (i.e., 15 dB/octave), a fourth-order bandpass converter would have to be used. The first design of an integrated bandpass oversampling A/D converter was presented in [Jantzi, 1993].

14.7 PRACTICAL CONSIDERATIONS

Stability

As with any feedback-type system, delta-sigma modulators have the potential to go unstable. A stable modulator is defined here as one in which the input (or inputs) to the quantizer (or quantizers) remains bounded such that the quantization does not become *overloaded*. An overloaded quantizer is one in which the input signal goes beyond the quantizer's normal range, resulting in the quantization error becoming greater than $\pm\Delta/2$.

Unfortunately, the stability of higher-order 1-bit modulators is not well understood as they include a highly nonlinear element (a 1-bit quantizer), resulting in the system being stable for one input but unstable for another. As a general rule of thumb, keeping the peak frequency response gain of the noise-transfer function, $N_{TF}(z)$, less than 1.5 often results in a stable modulator [Chao, 1990].[7] In mathematical terms,

$$\left|N_{TF}(e^{j\omega})\right| \le 1.5 \qquad \text{for } 0 \le \omega \le \pi \tag{14.45}$$

should be satisfied for a 1-bit quantizer. It should be noted that this stability criterion has little rigorous justification and that there does not presently exist any necessary and sufficient stability criterion for $\Delta\Sigma$ modulators having arbitrary inputs. There is,

7. A figure of 2 was used in the reference but 1.5 appears to be a more practical choice.

15.2 Based on the block diagram of Fig. 15.9, find transconductance values for a first-order filter with a dc gain of 10 and a pole at 15 MHz (no finite zero). Assume the integrating capacitors are sized $C_A = 5$ pF.

15.3 Find the transconductance and capacitance values of the second-order filter of Fig. 15.11 for a low-pass filter with a pole frequency of 10 MHz, $Q = 1$, and a dc gain of 5.

15.4 Derive the design equations for the biquad circuit shown in Fig. 15.24.

15.5 Consider the transconductor shown in Fig. 15.13. Find the transconductance of this circuit for finite opamp gains A.

15.6 In the transconductor of Fig. 15.12(*b*), find the minimum collector voltages of Q_1, Q_2 such that they remain in the active region for $v_i = \pm 1$ V around a common-mode voltage of 2 V. Repeat for the transconductor of Fig. 15.13.

15.7 In the transconductor of Fig. 15.14, find the new transconductance value if the base-emitter areas of Q_7, Q_8 are four times those of Q_3, Q_4.

15.8 Consider the transconductor of Fig. 15.14, where we want $G_m = 1$ mA/V. What are reasonable values for I_1 and I_2 such that all transistors do not fall below 20 percent of their nominal bias current when the peak value of $v_i = v_i^+ - v_i^-$ is 500 mV?

15.9 Consider the linearized two-differential pairs shown in Fig. 15.20, where $I_1 = 2$ mA. Find the percentage of error between an ideal linear transconductor and the true output current when $v_i = 48$ mV.

15.10 Consider the circuit Fig. 15.21, with $I_1 = 100\ \mu$A, $I_2 = 10\ \mu$A, $(W/L)_9 = 2$, $V_C = 5$ V, and $v_i^- = 2.5$ V.

- **a.** Find the transconductance, G_m.
- **b.** Assuming a perfectly linear transconductor, find i_{o1} when v_i^+ equals 2.6 V and 3 V.
- **c.** Find the true value of i_{o1} when v_i^+ equals 2.6 V and 3 V by taking into account the triode equation for Q_9 (assume everything else is ideal). Compare your results with those in part b.

15.11 Choose reasonable transistor sizes for the circuit in Fig. 15.25 to realize a transconductor that has $G_m = 0.3$ mA/V, $k_1/k_3 = 6.7$, and a peak differential-input voltage of 1 V.

15.12 Consider the circuit in Fig. 15.30, where all transistors have $W/L = 10\ \mu m/2\ \mu m$, $V_{DD} = -V_{SS} = 2.5$ V, and $V_{C1} = -V_{C2} = 2.0$ V. Find the transconductance of the circuit.

15.13 Show that the transconductance of Fig. 15.32 is given by

$$G_m = \left(\frac{n}{n+1}\right) 4\sqrt{kI_B}$$

15.14 Consider the transconductor shown in Fig. 15.34, where all transistors have size $W/L = 10\ \mu m/2\ \mu m$, $I_B = 50\ \mu$A, and $V_{DD} = -V_{SS} = 3$ V. What

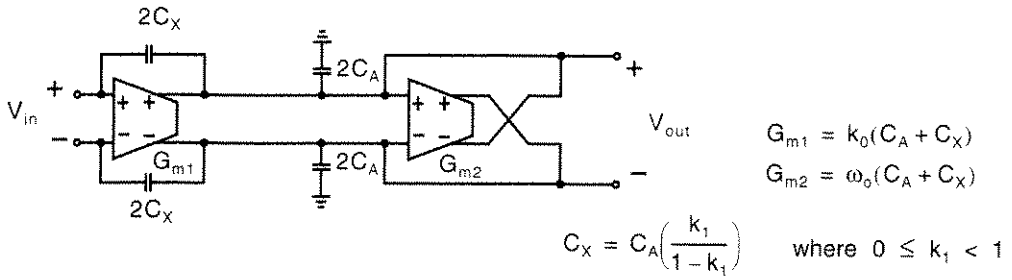


Fig. 15.9 A fully differential general first-order G_m-C filter.

than 1. Such a result should come as no surprise since the high-frequency gain of this circuit is simply a capacitor-divider circuit, and hence the restriction on k_1. Such a restriction on the maximum magnitude of the high-frequency gain would not occur if a G_m-C opamp filter were used since the feed-in capacitor could go into the virtual ground of an opamp and high-frequency gains greater than one would be possible.

Finally, the equivalent fully differential first-order G_m-C filter is shown in Fig. 15.9. Note that capacitor sizes are doubled here, in relation to the single-ended case, so that the same design equations occur. Also note that the same restriction holds on k_1, although a negative value of k_1 can be realized by cross-coupling the feed-in capacitor pair, C_X.

EXAMPLE 15.2

Based on Fig. 15.9, find component values for a first-order filter with a dc gain of 0.5, a pole at 20 MHz, and a zero at 40 MHz. Assume the integrating capacitors are sized $C_A = 2$ pF.

Solution

A first-order filter with a zero at 40 MHz and a pole at 20 MHz is given by

$$H(s) = \frac{k(s + 2\pi \times 40 \text{ MHz})}{(s + 2\pi \times 20 \text{ MHz})} \tag{15.15}$$

The leading coefficient is determined by setting the dc gain to 0.5, resulting in $k = 0.25$. Thus, we have

$$H(s) = \frac{0.25s + 2\pi \times 10 \text{ MHz}}{s + 2\pi \times 20 \text{ MHz}} \tag{15.16}$$

and equating this transfer function to (15.9) results in

$$k_1 = 0.25 \tag{15.17}$$

$$k_0 = 2\pi \times 10^7 \tag{15.18}$$

$$\omega_o = 4\pi \times 10^7 \tag{15.19}$$

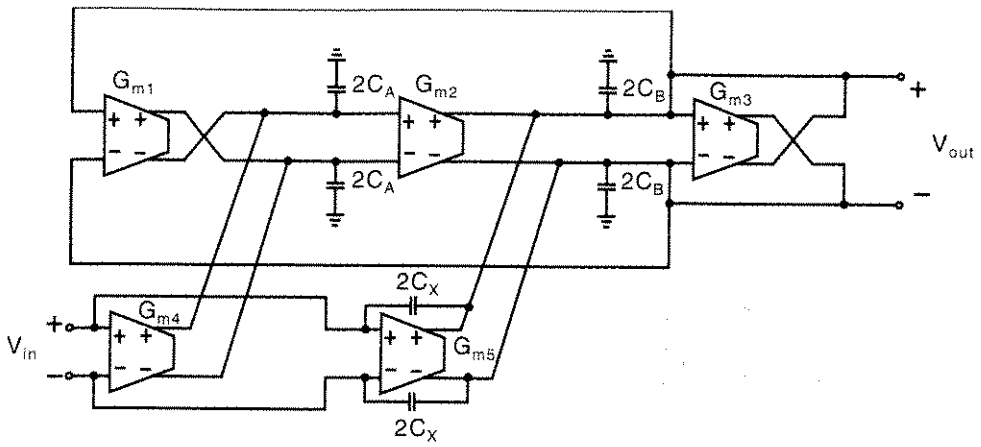


Fig. 15.11 A general second-order filter using fully differential G_m-C technology.

$$k_1 = \frac{G_{m5}}{C_X + C_B} \tag{15.26}$$

$$k_0 = \frac{G_{m2}G_{m4}}{C_A(C_X + C_B)} \tag{15.27}$$

and

$$\omega_o^2 = \frac{G_{m1}G_{m2}}{C_A(C_X + C_B)} \tag{15.28}$$

For Q, we note that

$$\frac{\omega_o}{Q} = \frac{G_{m3}}{C_X + C_b} \tag{15.29}$$

and so, by using (15.28), we can solve for Q, resulting in

$$Q = \sqrt{\left(\frac{G_{m1}G_{m2}}{G_{m3}^2}\right)\left(\frac{C_X + C_B}{C_A}\right)} \tag{15.30}$$

Although the preceding equations are for analyzing a given circuit, they can also be used for design, resulting in the following design equations:

$$C_X = C_B\left(\frac{k_2}{1 - k_2}\right) \quad \text{where } 0 \le k_2 < 1$$

$$G_{m1} = \omega_o C_A \quad G_{m2} = \omega_o(C_B + C_X) \quad G_{m3} = \frac{\omega_o(C_B + C_X)}{Q}$$

$$G_{m4} = (k_o C_A)/\omega_o \quad G_{m5} = k_1(C_B + C_X)$$

Note that for this design, there is a restriction on the high-frequency gain coefficient, k_2, similar to that occurring in the first-order case.

make the simplifying assumption that the V_{be} voltages of the transistors are constant. As a result, we see that the differential input voltage, v_i, appears across the two $R_E/2$ resistors in Fig. 15.12(*a*) and across R_E in Fig. 15.12(*b*). Thus, the emitter current I_{E1} is given by

$$I_{E1} = I_1 + \frac{v_i}{R_E} \tag{15.36}$$

and the emitter current I_{E2} is given by

$$I_{E2} = I_1 - \frac{v_i}{R_E} \tag{15.37}$$

Ignoring base currents, these two emitter currents equal their respective collector currents. Then defining i_{o1} to be the difference in the output collector currents from I_1 (as shown), we have

$$i_{o1} = \frac{v_i}{R_E} \tag{15.38}$$

Thus, we see that the transconductance of these two differential input circuits is a fixed value of $1/R_E$. One important difference between the two fixed transconductors of Fig. 15.12 is that, in the case of $v_i = 0$, a bias current of I_1 flows through the two $R_E/2$ resistors in Fig. 15.12(*a*), whereas no bias current is flowing through R_E in Fig. 15.12(*b*). As a result, the common-mode voltage of Fig. 15.12(*b*) can be closer to ground. For example, if a bias current of $I_1 = 100\ \mu A$ is used together

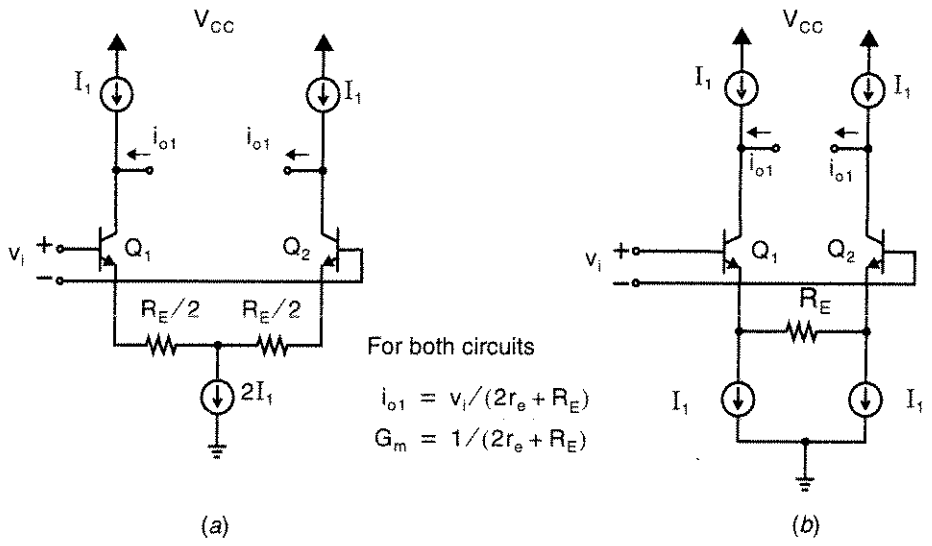


Fig. 15.12 Fixed transconductors using resistors. The lower common-mode range of the circuit in (*a*) is not as low as that of the circuit in (*b*) due to bias currents flowing through the $R_E/2$ resistors.