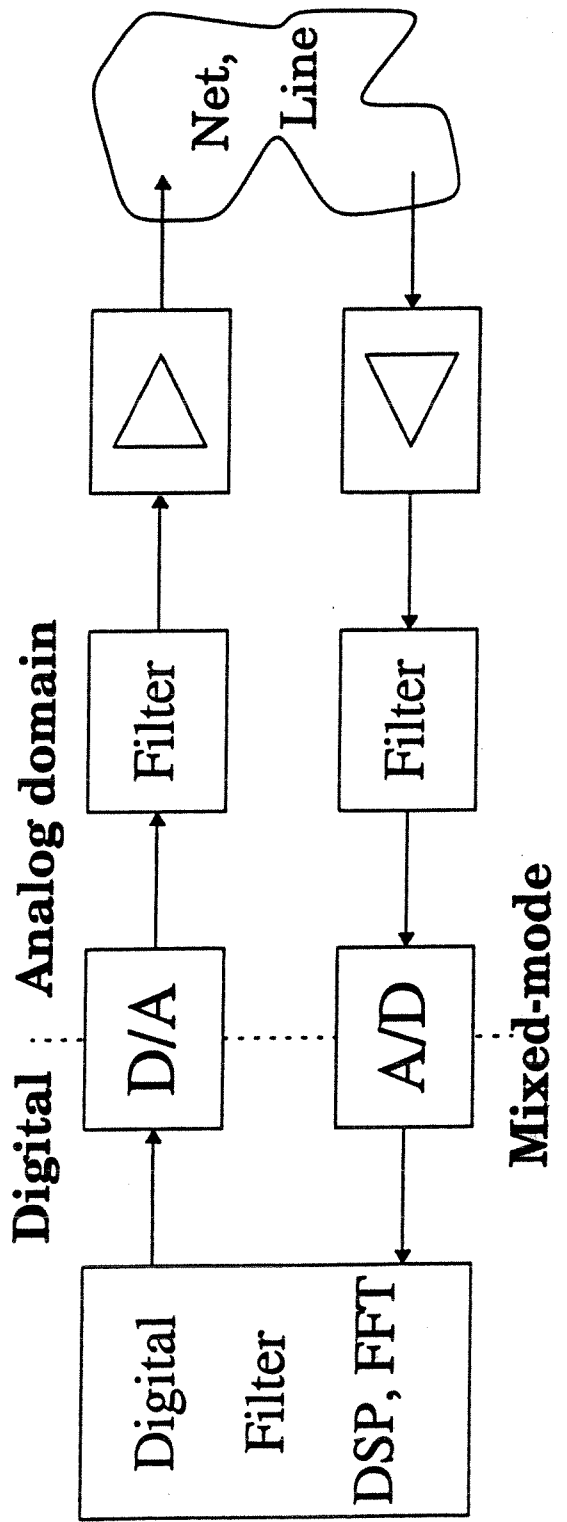
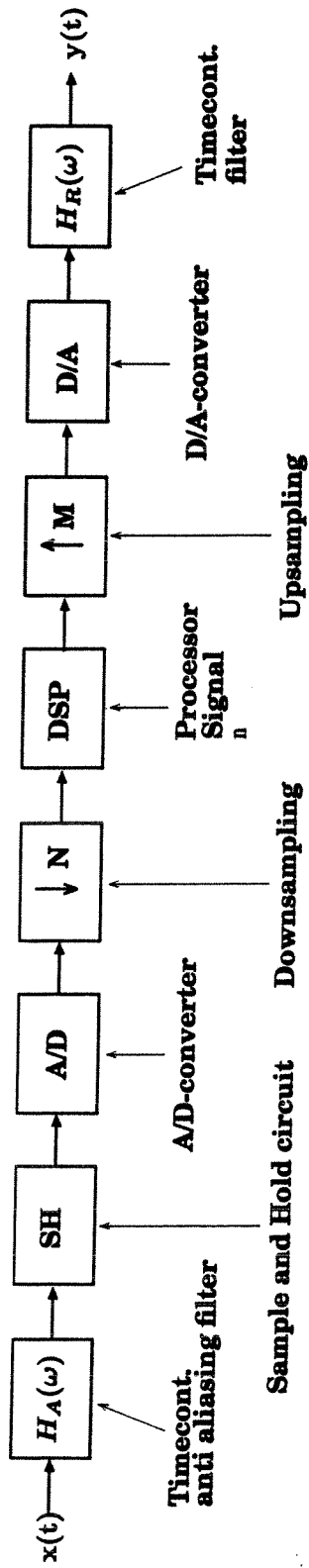


Blockdiagram. Digital Signal Processing of time continuous signals.



Traditional view of the telecommunication system.

ANALOG PERFORMANCE METRICS

- | TIME DOMAIN | FREQUENCY DOMAIN |
|--|--|
| <ul style="list-style-type: none"> ● STEP ANSWER $g(t)$ ○ RISE TIME (10-90%) ○ SETTLING TIME (5%) ○ SLEW RATE $\frac{dg(t)}{dt} \Big _{\max}$ ● OVERSHOOT/GLITCH ● POWER DISSIPATION | <ul style="list-style-type: none"> ● SNR (SIGNAL NOISE RATIO) ● THD (TOTAL HARMONIC DISTORTION) ● SNDR (SIGNAL NOISE DISTORTION RATE) ● SFDR (SPURIOUS-FREE DYNAMIC RANGE) ● BANDWIDTH ● POWER DISSIPATION |

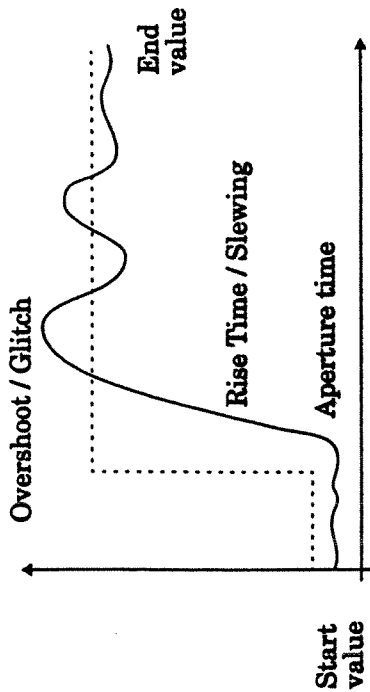


Figure 1.2: Time-domain characteristics.

NOISE AND DISTORSION METRICS

$$SNR = 10 \log \frac{P_s}{P_n} \quad [dB]$$

$$THD = 10 \log \frac{P_s}{P_{d, Harm}} \quad [dB]$$

$$SNDR = 10 \log \frac{P_s}{P_{n+d}} \quad [dB]$$

$$SFDR = 10 \log \frac{P_s}{P_{d, max}} \quad [dB]$$

- P_s = signal power
- P_n = noise power
- $P_{d, Harm}$ = power of all harmonic distortion
- P_{n+d} = total power of noise and distortion
- $P_{d, max}$ = power of the strongest spurious peak

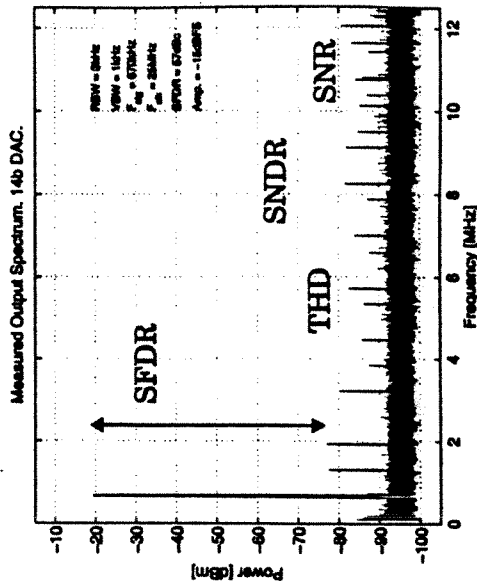
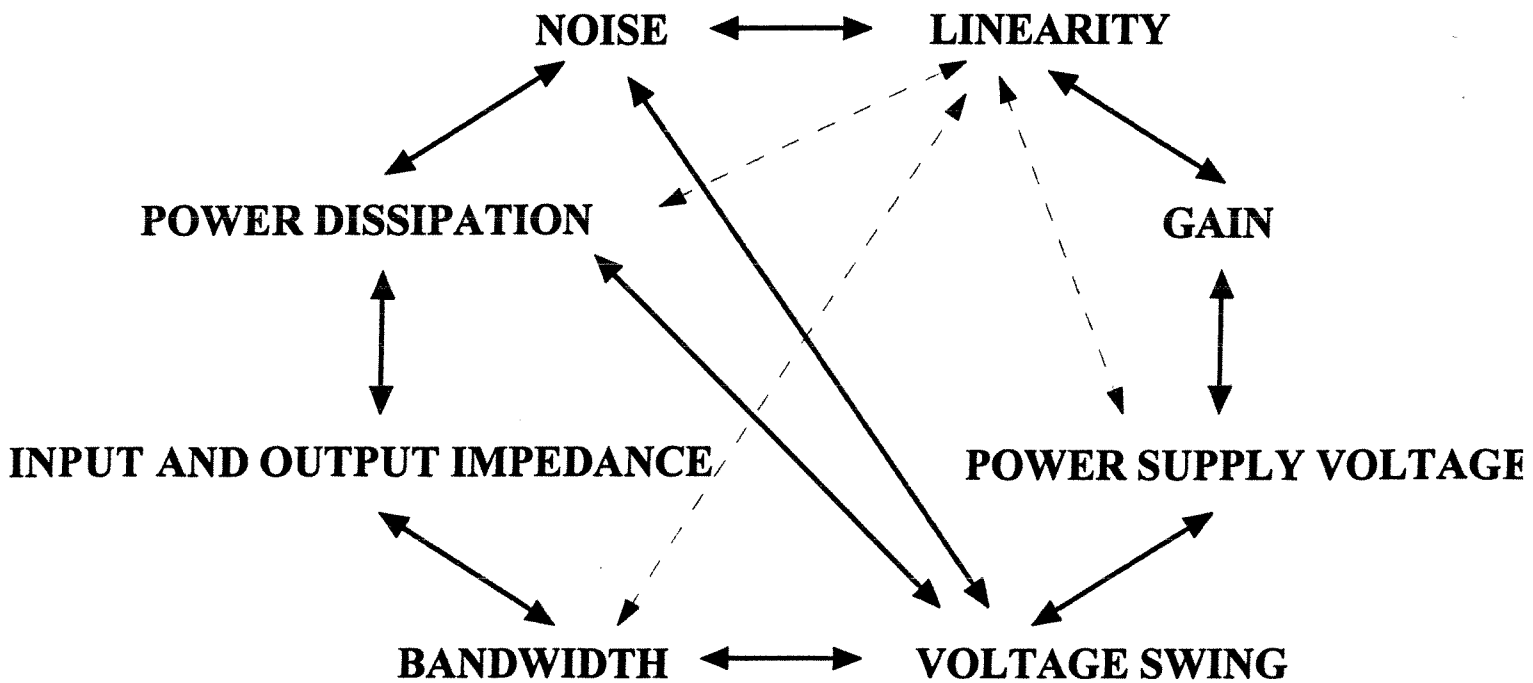


Figure 1.3: Frequency-domain characteristics.

DIGITAL PERFORMANCE METRICS**TIME DOMAIN**

- **CLOCK FREQUENCY**
- **NUMBER OF DIGITS**
- **POWER DISSIPATION**

DESIGN OCTAGONE

BENEFITS OF SC-FILTER

- A. SC-filters just require capacitors, switches (MOS-transistors) and operational amplifiers.
- B. Can be implemented in standard CMOS-processes or integrated circuits.
- C. Coefficient values is determined by capacitor ratios, which can be implemented with a higher grade of accuracy. (THE MAIN ADVANTAGE OF SC-FILTERS)

DRAWBACKS OF SC-FILTER

- A. Need linear capacitors, which require special CMOS-processes with additional poly-silicon layer.
- B. Need good matching between capacitors which imply a large chip-area.
- C. Operational amplifiers imply a lower limit on the supply voltage required.

SHORTCOMINGS THAT AFFECT V_{OUT} FROM AN SC-CIRCUIT

- A. Parasitic capacitors.
- B. Resistance in switches.
- C. Finite gain of OP-amp.
- D. Finite input-resistance of OP-amp.
- E. Finite bandwidth of OP-amp.
- F. Input offset voltage of OP-amp. (Mismatch between transistors in the input differential pair.)

CHARGE REDISTRIBUTION ANALYSIS

RULES:

- A. Both plates of a capacitor always have the same amount of charge. (Positive (+) on one plate and negative (-) on the other.)
- B. Not connected capacitor plates will keep their charge.
- C. If both plates of a capacitor are connected to the same potential, the capacitor will be discharged.
- D. Only the output of an ideal OP-amp (not the input) gives/takes charge; as much as needed.
- E. A switch-capacitor network without any DC-path to ground strives towards equilibrium. (CHARGE CONSERVATION)

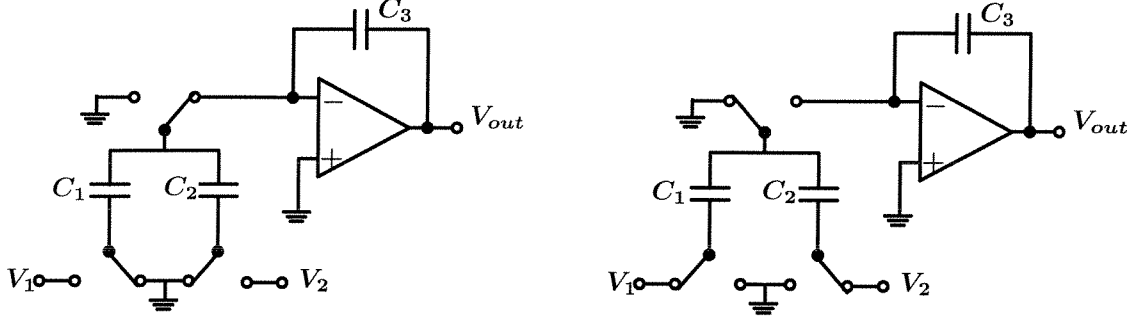
PARASITIC SENSITIVITY

RULES:

- A. Parasitics continuously connected to input voltage source (ideal) or to OP-amp. (ideal) output do not affect $H(z)$.
(Ideal sources can give/take as much charge as needed)
- B. Parasitics connected between "ground-ground" or between "ground-virtual ground" in both phases do not affect $H(z)$.
(The capacitors charge is zero all the time.)
- C. Parasitics that charge from a voltage source or from OP-amp. output during one phase and discharge to ground during next phase do not affect $H(z)$.
- D. Parasitics connected to capacitor plates that are charging during one phase and not connected during next phase do not effect $H(z)$.
(Capacitors can not discharge.)
- E. Parasitics that charge from a voltage source or from OP-amp. output during one phase and discharge to a sensitive node (eg. another capacitor plate) during next phase does affect $H(z)$.

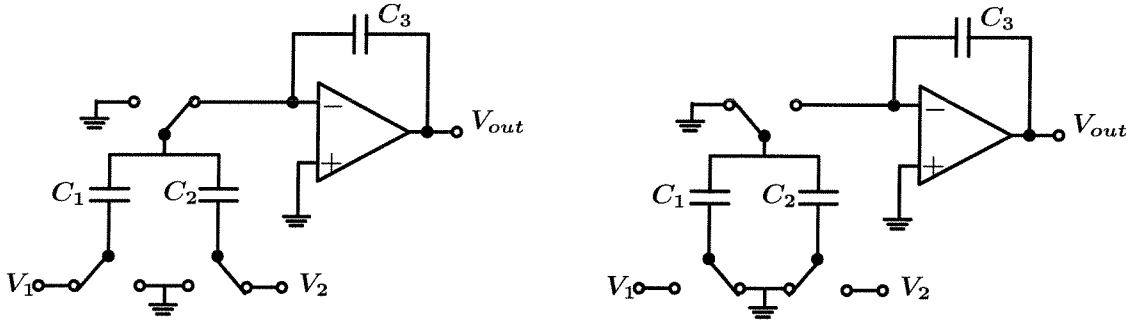
SUMMATORS (Not sensitive for parasitics.)

A. Integrator, summing, non-inverting. Phase 1: Integrator, summing, non-inverting. Phase 2:



$$V_{out} = \frac{C_1}{C_3} \cdot \frac{z^{-1}}{1 - z^{-1}} \cdot V_1(z) + \frac{C_2}{C_3} \cdot \frac{z^{-1}}{1 - z^{-1}} \cdot V_2(z)$$

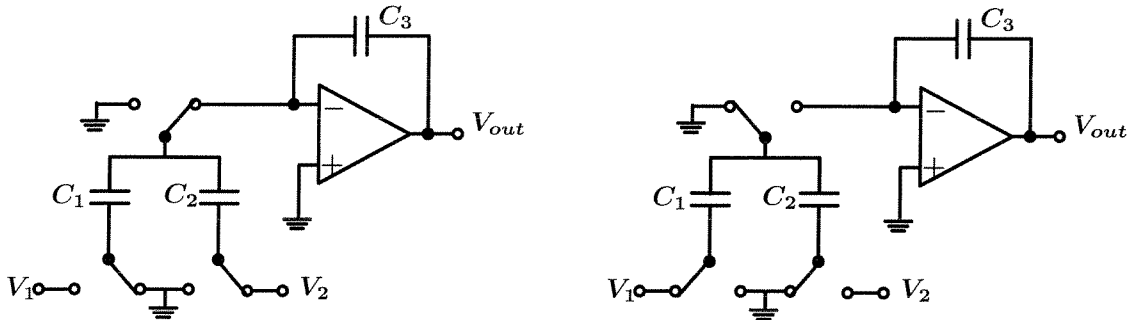
B. Integrator, summing and inverting. Phase 1: Integrator, summing and inverting. Phase 2:



$$V_{out} = -\frac{C_1}{C_3} \cdot \frac{1}{1 - z^{-1}} \cdot V_1(z) - \frac{C_2}{C_3} \cdot \frac{1}{1 - z^{-1}} \cdot V_2(z)$$

C. Integrator, differens-counting. Phase 1:

Integrator, differens-counting. Phase 2:

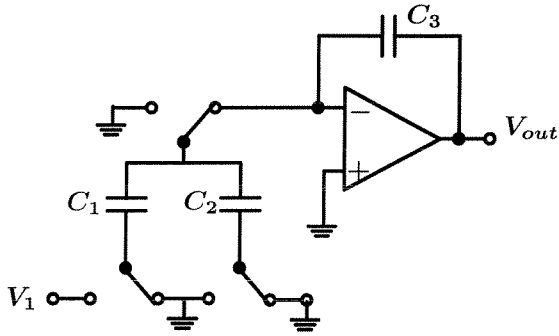


$$V_{out} = \frac{C_1}{C_3} \cdot \frac{z^{-1}}{1 - z^{-1}} \cdot V_1(z) - \frac{C_2}{C_3} \cdot \frac{1}{1 - z^{-1}} \cdot V_2(z)$$

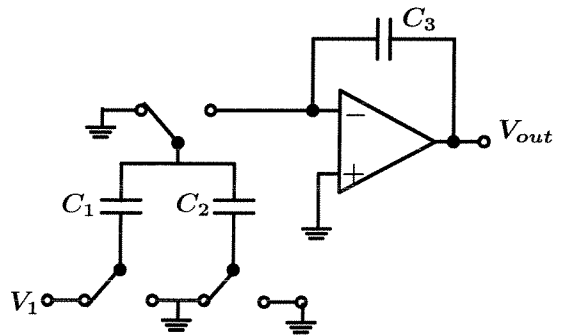
Integrator, differens-counting. Superposition.

I. V_1 included. V_2 replaced by short-circuit.

Phase 1:

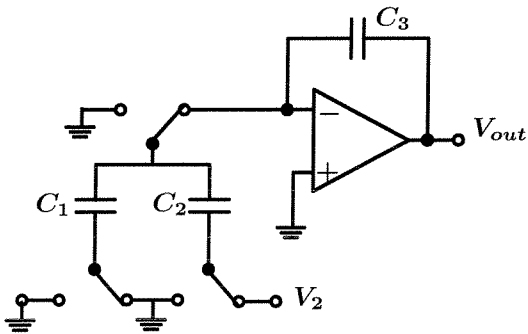


Phase 2:

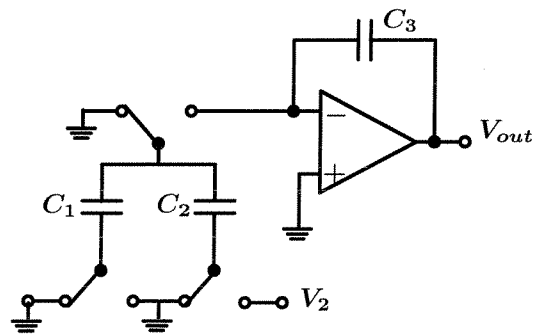


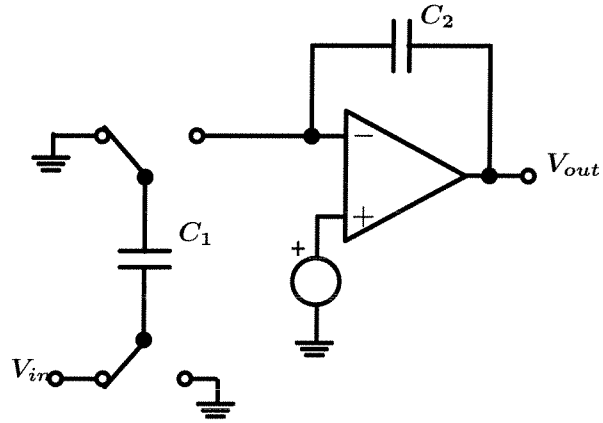
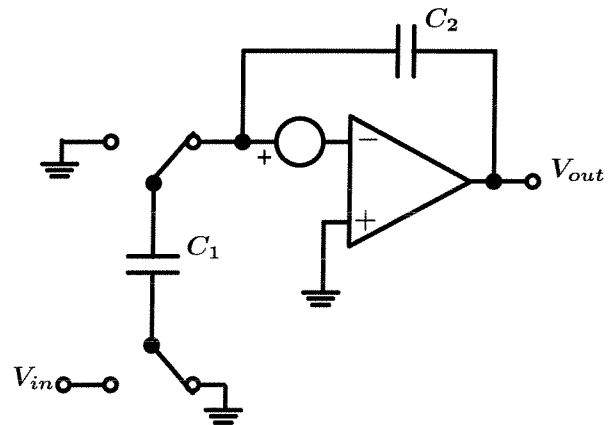
II. V_2 included. V_1 replaced by short-circuit.

Phase 1:

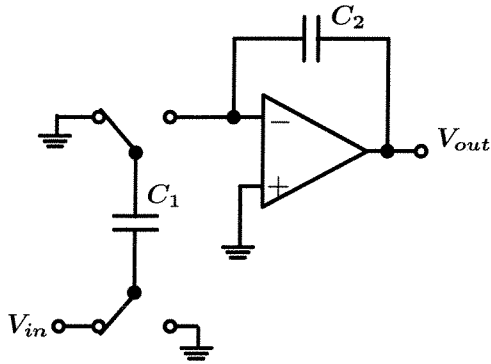


Phase 2:

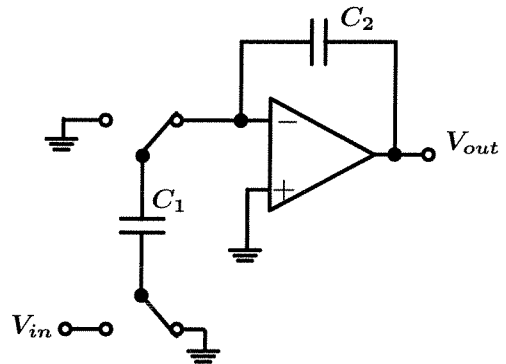


Equivalent Circuit considering Offset Voltage**Equivalent Circuit considering Finite Gain**

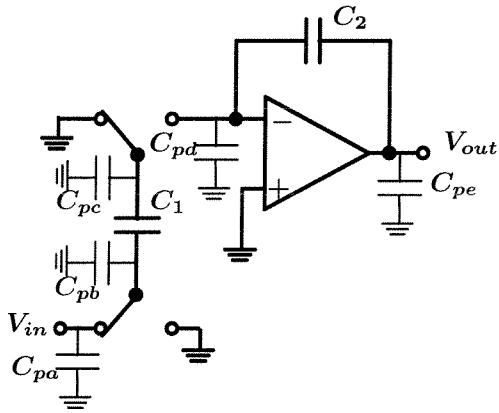
Integrator(accumulator). Phase 1:



Integrator(accumulator). Phase 2:



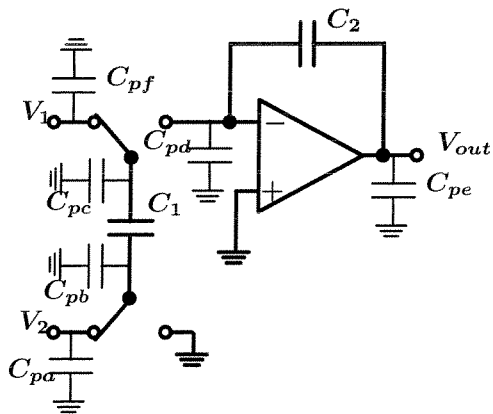
Integrator with parasitic capacitances



Top plate connection

	Phase 1	Phase 2	Affecting H(z)
C_{pa}			
C_{pb}			
C_{pc}			
C_{pd}			
C_{pe}			

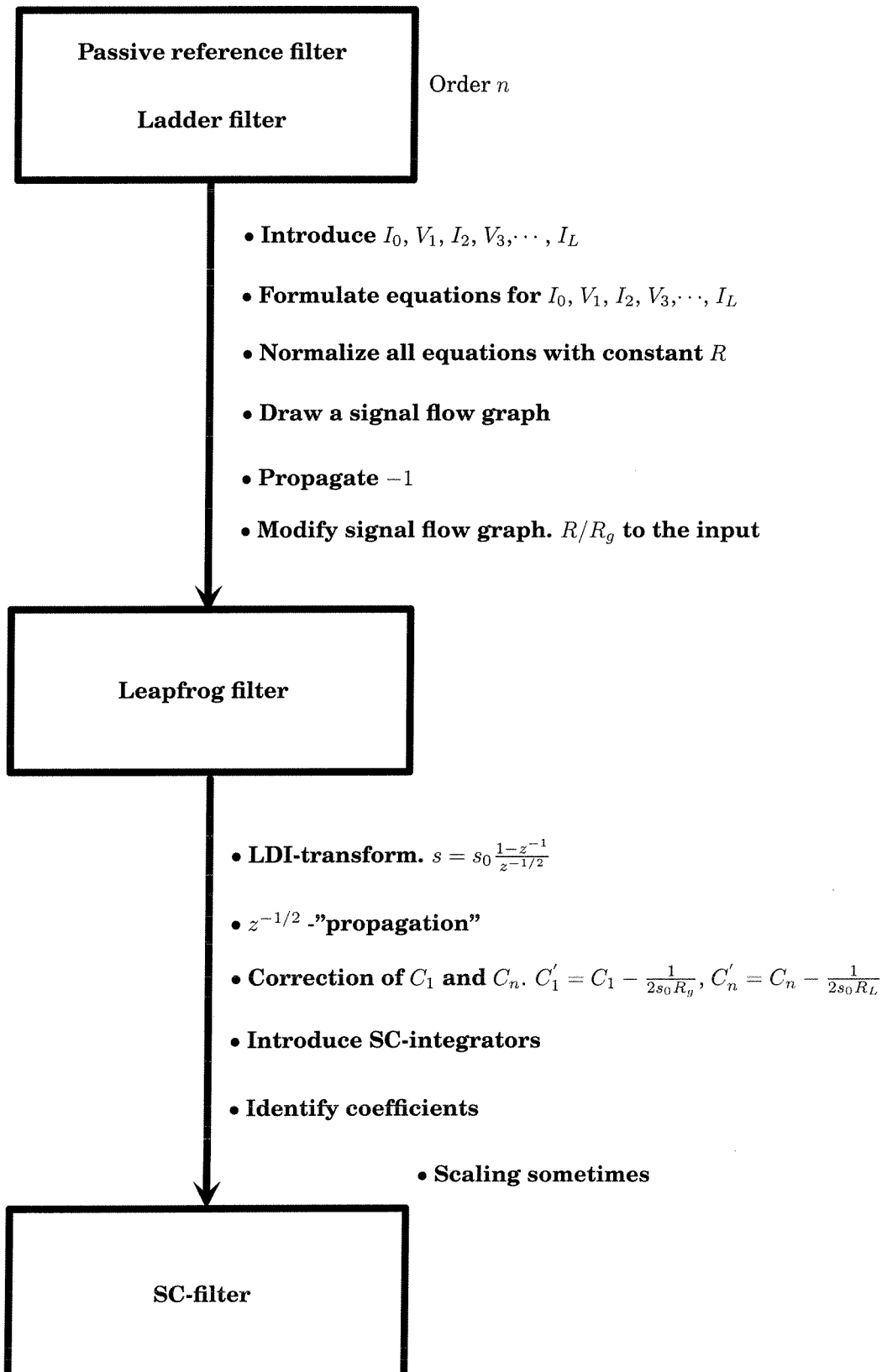
Summing integrator with parasitics



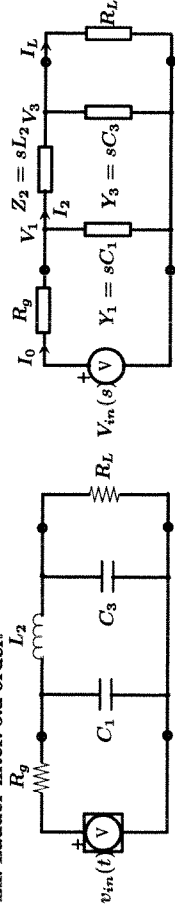
Top plate connection

	Phase 1	Phase 2	Affecting H(z)
C_{pa}			
C_{pb}			
C_{pc}			
C_{pd}			
C_{pe}			
C_{pf}			

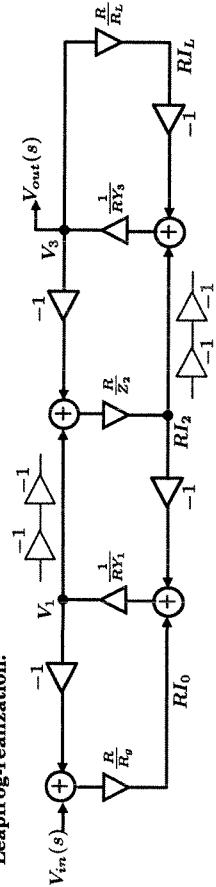
DESIGN OF LEAPFROG SC-FILTER



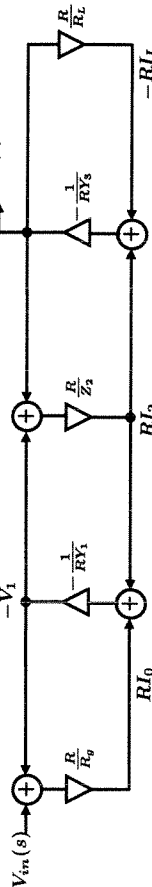
Ex. Ladder-filter: 3-d order.



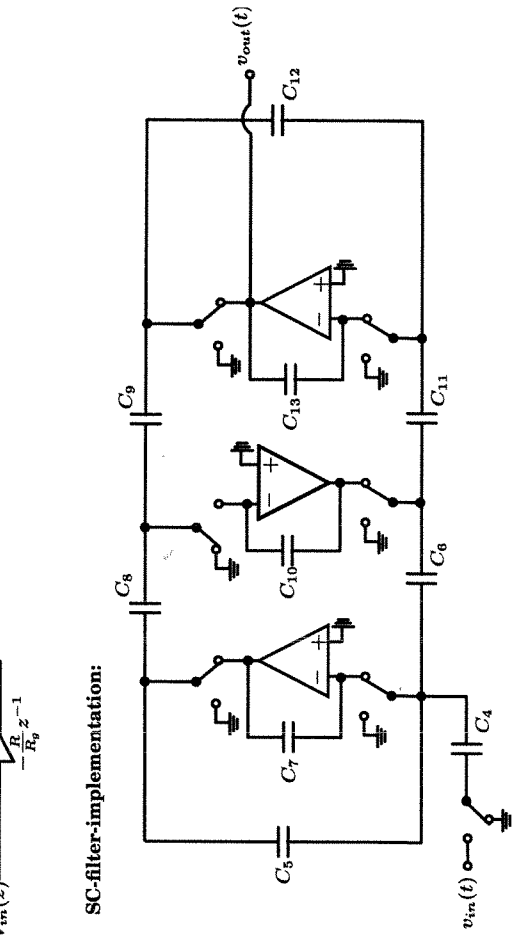
Leapfrog-realization:



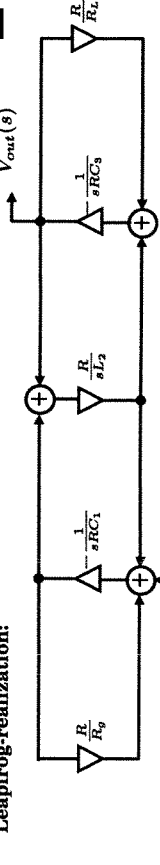
LDI-transformation:



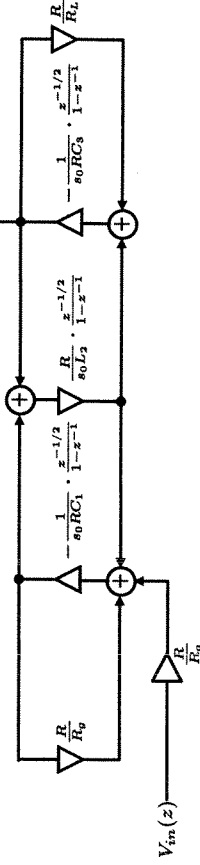
SC-filter-implementation:



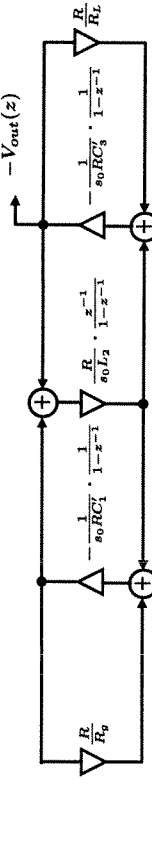
Leapfrog-realization:



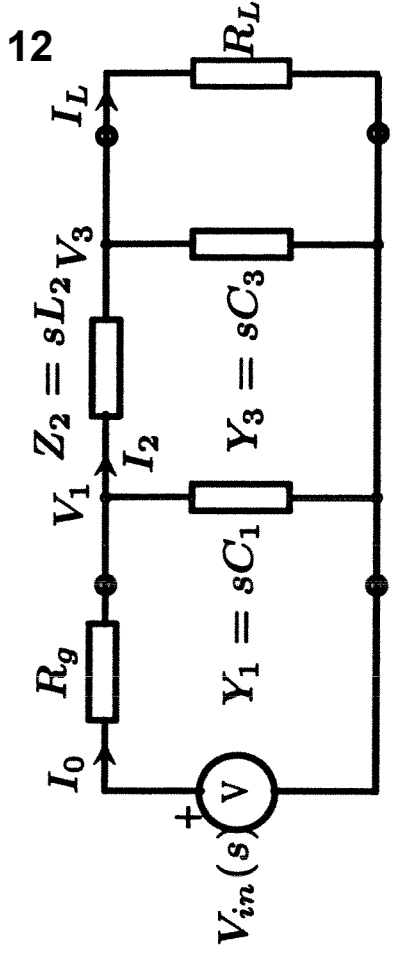
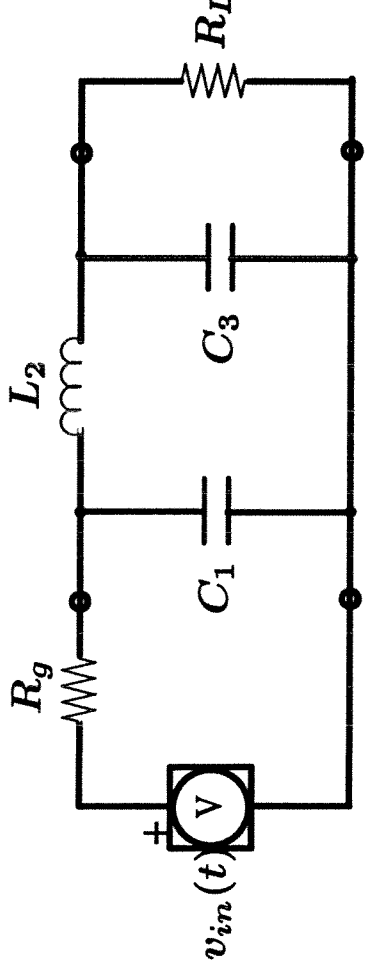
LDI-transformation:



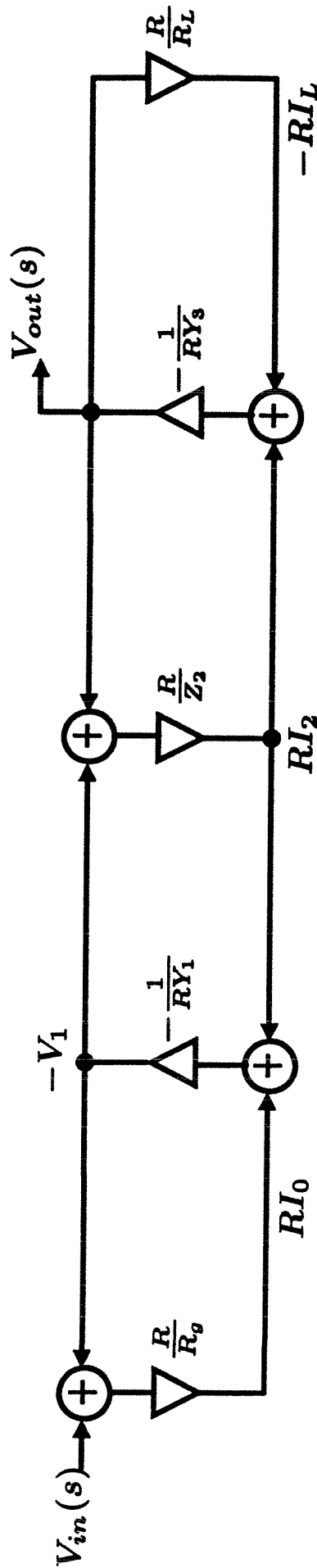
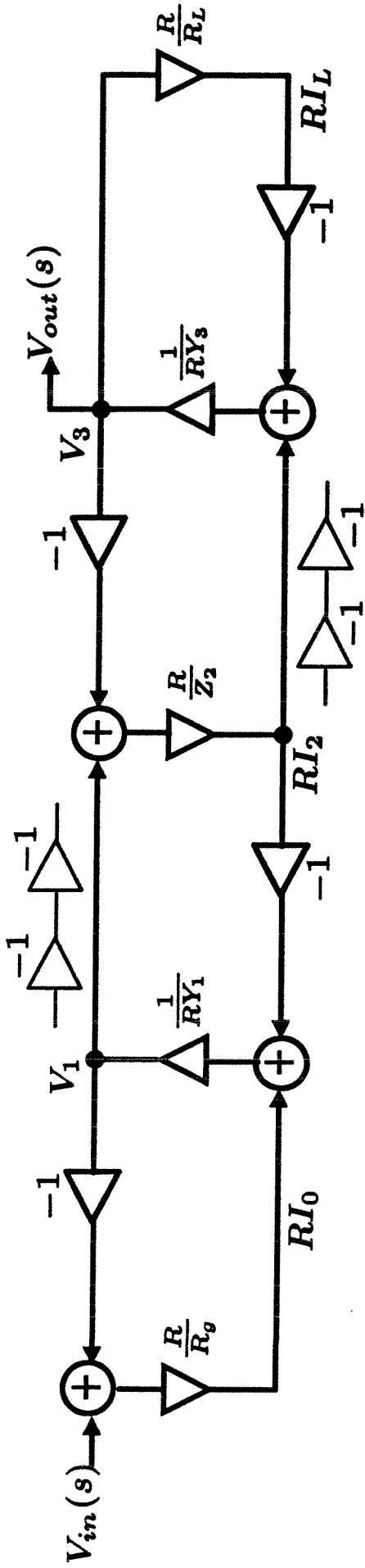
SC-filter-implementation:

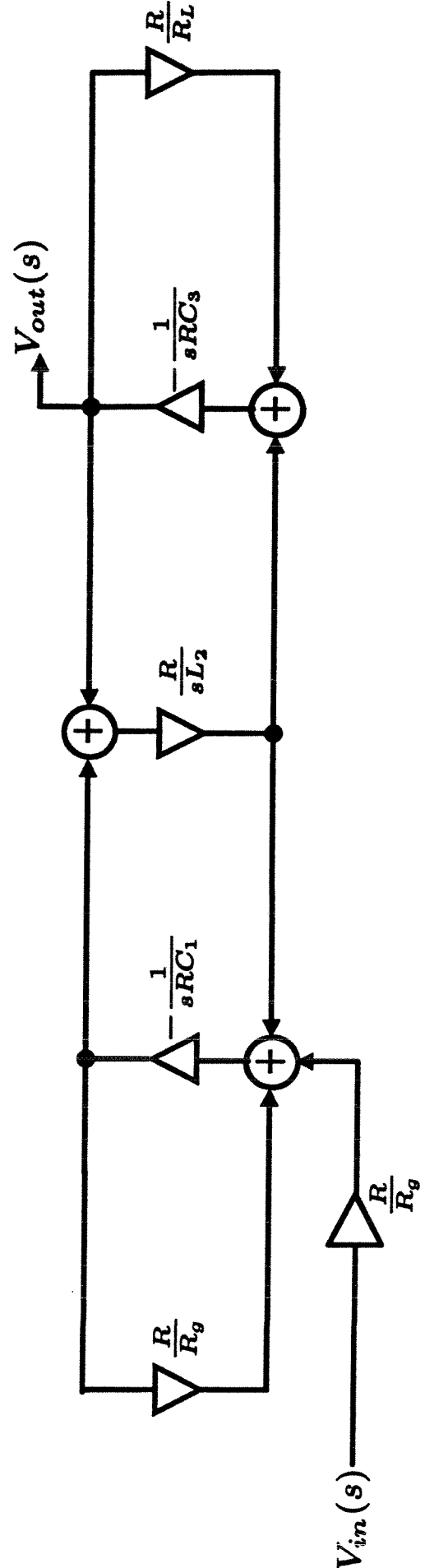
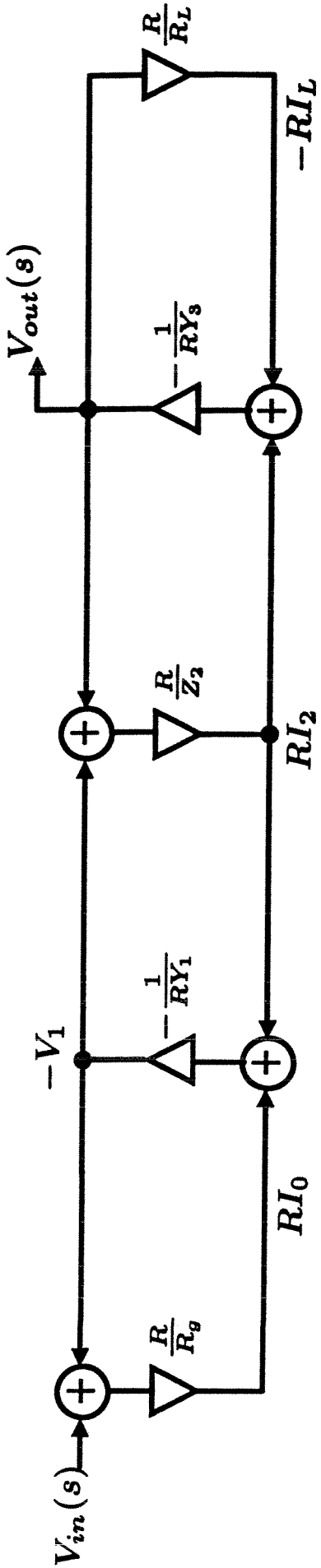


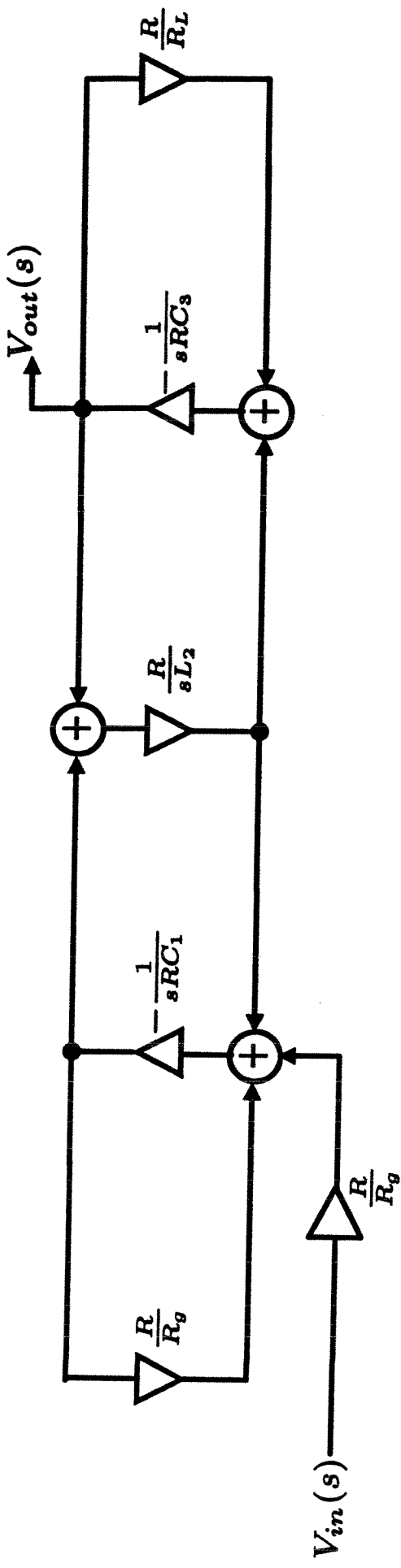
Ex. Ladder-filter. 3:d order.



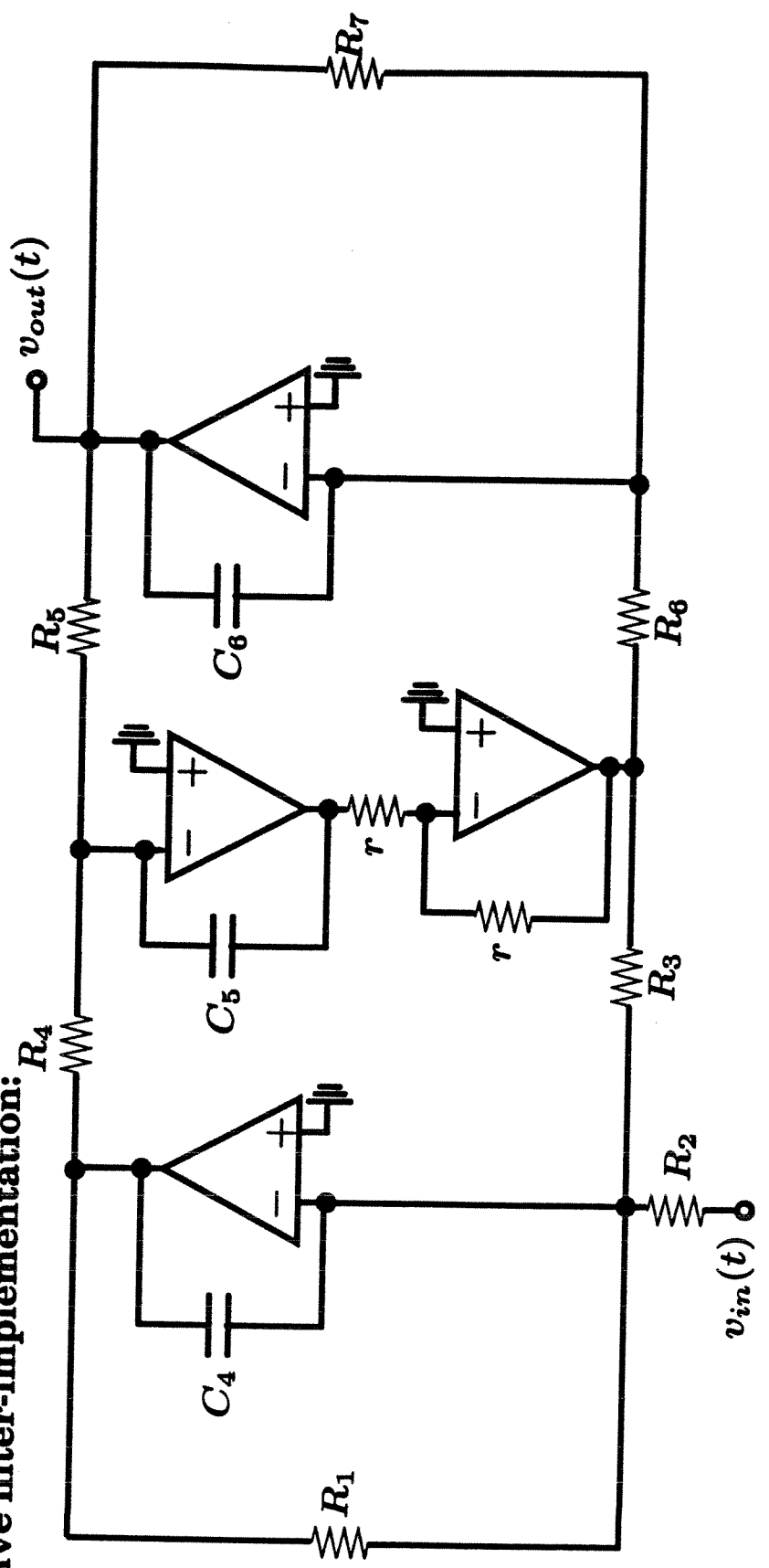
Leapfrog-realization:



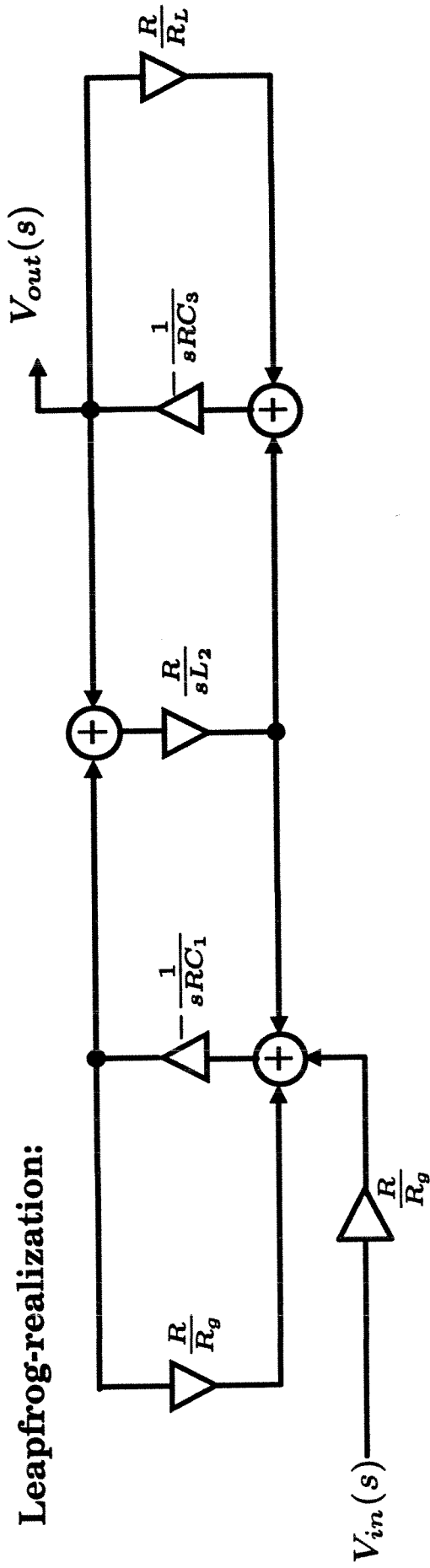




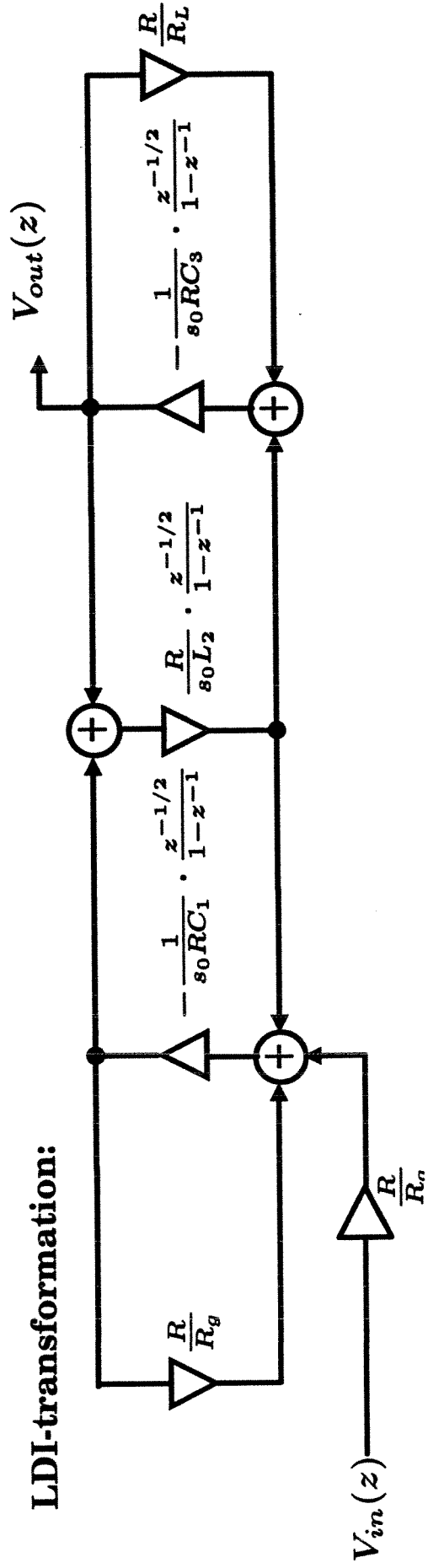
RC-active filter-implementation:



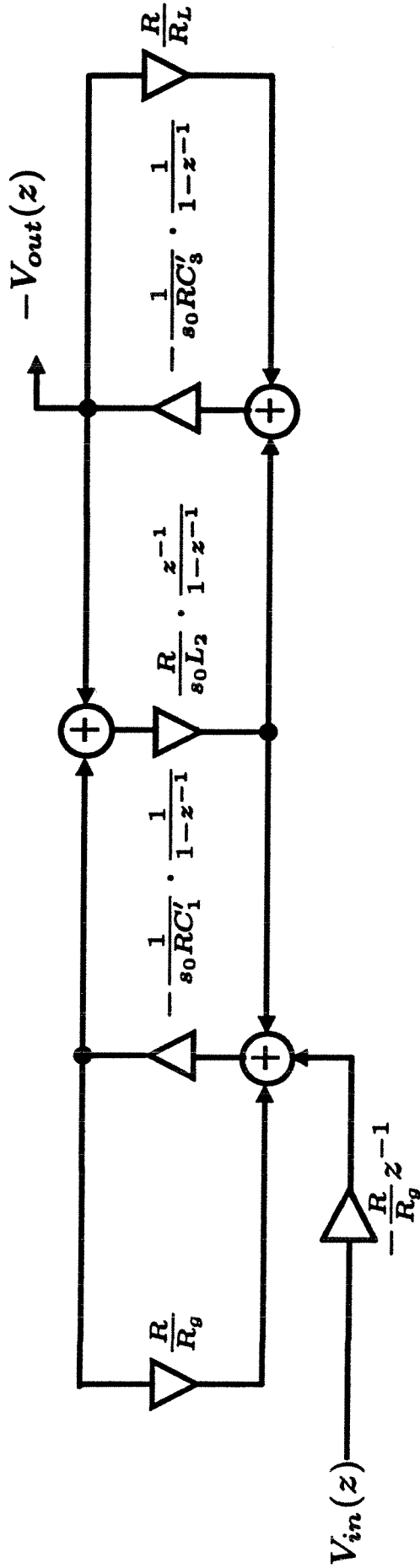
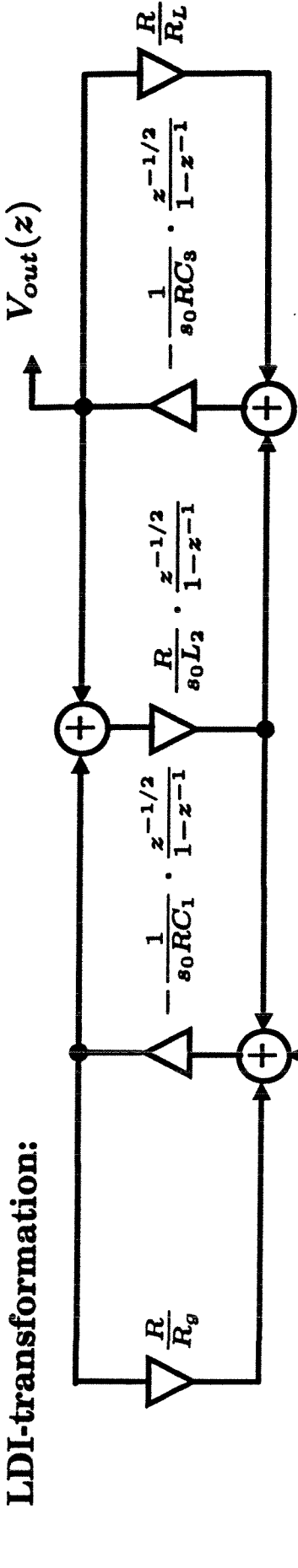
Leapfrog-realization:

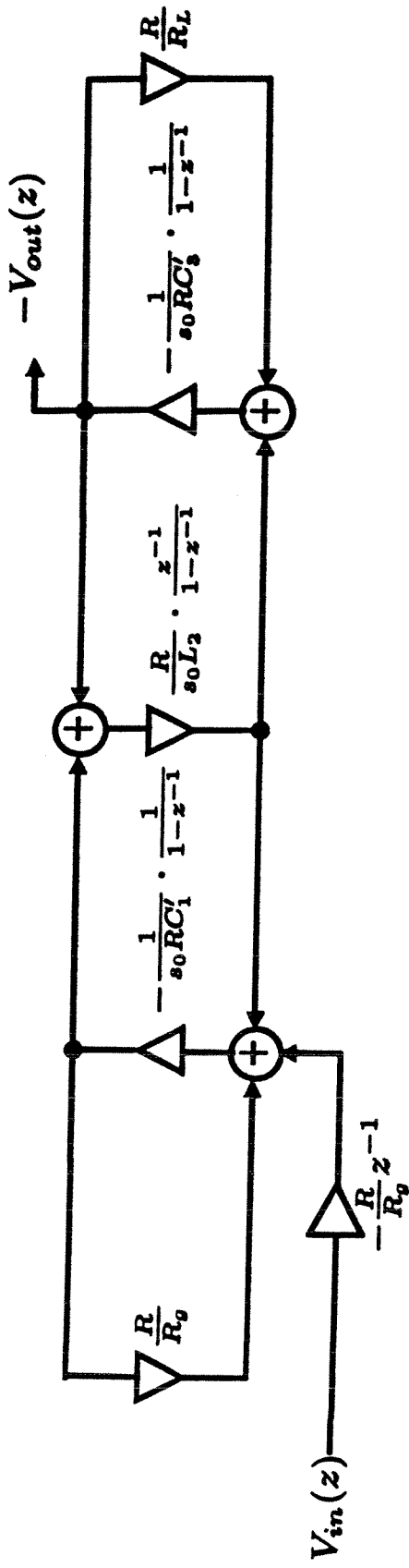


LDI-transformation:

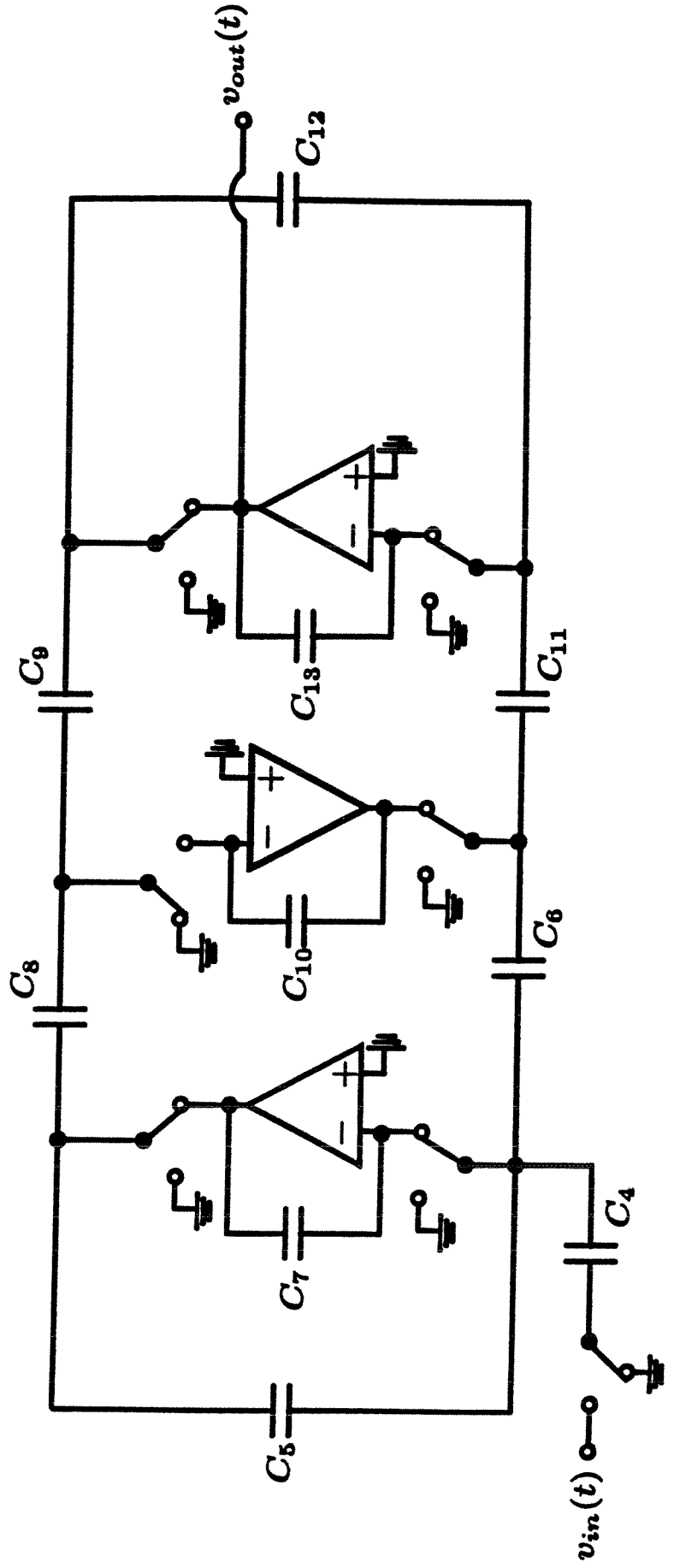


LDI-transformation:





SC-filter-implementation:



IDENTIFYING COEFFICIENTS LEAPFROG SC-FILTER

$$\begin{cases} V_I = \frac{1}{s_0 R_g C'_1} \cdot \frac{z^{-1}}{1-z^{-1}} \cdot V_{in} - \frac{1}{s_0 R_g C'_1} \cdot \frac{1}{1-z^{-1}} \cdot V_I - \frac{1}{s_0 R C'_1} \cdot \frac{1}{1-z^{-1}} \cdot V_{II} \\ V'_I = \frac{C_4}{C_7} \cdot \frac{z^{-1}}{1-z^{-1}} \cdot V_{in} - \frac{C_5}{C_7} \cdot \frac{1}{1-z^{-1}} \cdot V'_I - \frac{C_6}{C_7} \cdot \frac{1}{1-z^{-1}} \cdot V'_{II} \end{cases}$$

Identification gives:

$$\begin{cases} \frac{C_4}{C_7} = \frac{1}{s_0 R_g C'_1} = \frac{1}{s_0 R_g (C_1 - \frac{1}{2s_0 R_g})} = \frac{1}{s_0 R_g C_1 - 0.5} \\ \frac{C_5}{C_7} = \frac{1}{s_0 R_g C'_1} = \frac{1}{s_0 R_g C_1 - 0.5} \\ \frac{C_6}{C_7} = \frac{1}{s_0 R C'_1} = \frac{1}{s_0 R (C_1 - \frac{1}{2s_0 R_g})} \end{cases}$$

$$\begin{cases} V_{II} = \frac{R}{s_0 L_2} \cdot \frac{z^{-1}}{1-z^{-1}} \cdot V_I + \frac{R}{s_0 L_2} \cdot \frac{z^{-1}}{1-z^{-1}} \cdot V_{III} \\ V'_{II} = \frac{C_8}{C_{10}} \cdot \frac{z^{-1}}{1-z^{-1}} \cdot V'_I + \frac{C_9}{C_{10}} \cdot \frac{z^{-1}}{1-z^{-1}} \cdot V'_{III} \end{cases}$$

Identification gives:

$$\frac{C_8}{C_{10}} = \frac{C_9}{C_{10}} = \frac{R}{s_0 L_2}$$

$$\begin{cases} V_{III} = -\frac{1}{s_0 R C'_3} \cdot \frac{1}{1-z^{-1}} \cdot V_{II} - \frac{1}{s_0 R_L C'_3} \cdot \frac{1}{1-z^{-1}} \cdot V_{III} \\ V'_{III} = -\frac{C_{11}}{C_{13}} \cdot \frac{1}{1-z^{-1}} \cdot V'_{II} - \frac{C_{12}}{C_{13}} \cdot \frac{1}{1-z^{-1}} \cdot V'_{III} \end{cases}$$

Identification gives:

$$\begin{cases} \frac{C_{11}}{C_{13}} = \frac{1}{s_0 R C'_3} = \frac{1}{s_0 R (C_3 - \frac{1}{2s_0 R_L})} \\ \frac{C_{12}}{C_{13}} = \frac{1}{s_0 R_L C'_3} = \frac{1}{s_0 R_L (C_3 - \frac{1}{2s_0 R_L})} = \frac{1}{s_0 R_L C_3 - 0.5} \end{cases}$$

$$s_0 = \frac{\omega_{ac}}{2 \sin \frac{\omega_c T}{2}}$$

ω_{ac} = cutoff-frequency for the analog reference filter.

ω_c = cutoff-frequency for the discrete-time SC-filter.