TSEI05 Analog Timediscrete Integrated Circuits

- Lecture 11
  - Transmission Lines, Applications

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When is transmission line effects important?

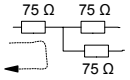
- Wavelength vs wire length

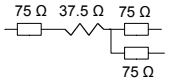
  conductor length $\geq \lambda = c / f$

- Examples
  - Phone wire: length = 5 km => problem when frequency > 50 kHz
    (ADSL uses up to at least 2 MHz)
  - CPU clock signal:
    2.4 GHz => length > 10 cm
    (lower if taking dielectric constant into account)

High frequency systems

- TV antenna system
  - 75 ohm antenna
  - How to split signal to two different rooms
    - 75-75/2 = 37.5 Ω series resistor
    - Loose 50% power!
- VGA screen extension cord
  - Possible problem if connector have different impedance compared to wire





Termination

- Assume driver low impedance (<< Z0)
- Assume reciever end high impedance (>> Z0), mostly capacitive load
- End resistor only to GND
  - Give high current when '1'
- End resistor to both GND and VCC
  - Reduce DC current
    - Calculate max current as thevenin equivalent (DC point + R1//R2 internal resistance)
  - Select R1 and R2 such that R1//R2 equal Z0
  - Lower current, but both when '0' and '1'

Forking wires

- Common wire from driver, forking to reach two recievers
- End resistor in forked wire
  - If Z0 in whole network, then fork gives reflection
  - If 2Z0 in wires after fork point then no reflection
    - Use 2Z0 also for termination
    - Requires both wire impedance 2Z0 as well as resistive termination of 2Z0

Daisy-chain configuration

- End resistor using daisy-chain configuration
  - Single wire runs to all elements in sequence
    - Have short main wire to gate input length
  - Drawback: reflection in reciver connections
    - Reciever is high impedance, mostly capacitive load
    - Assume Z0 = sqrt(L/C), long wires
    - Termination of wire from driver into C//Z0

$$Z_L(\omega)=\frac{1}{(j\omega C)}\|Z_0(\omega)=\frac{Z_0(\omega)\frac{1}{j\omega C}}{Z_0(\omega)+\frac{1}{j\omega C}}=\frac{Z_0(\omega)}{1+j\omega C Z_0(\omega)}$$

Daisy-chain configuration, cont.

- Reflection in first reciever connection
  - Calculate the reflection parameter R for this case

$$R(\omega)=\frac{Z_L(\omega)-Z_0(\omega)}{Z_L(\omega)+Z_0(\omega)}=\frac{\frac{Z_0(\omega)}{1+j\omega C Z_0(\omega)}-Z_0(\omega)}{\frac{Z_0(\omega)}{1+j\omega C Z_0(\omega)}+Z_0(\omega)}=\frac{Z_0(\omega)-Z_0(\omega)-j\omega C Z_0(\omega)Z_0(\omega)}{Z_0(\omega)+Z_0(\omega)+j\omega C Z_0(\omega)Z_0(\omega)}=$$

$$=\frac{\frac{1}{1+j\omega C Z_0(\omega)}-1}{\frac{1}{1+j\omega C Z_0(\omega)}-1}=\frac{1-1-j\omega C Z_0(\omega)}{1+1+j\omega C Z_0(\omega)}=\frac{-j\omega C Z_0(\omega)}{2+j\omega C Z_0(\omega)}$$

  - High frequency components (large ω) are reflected!
- End resistor placement: Not in front of gate.
  - Use an extension of the wire followed by a termination (daisychain gate and termination resistor).

Source terminator

- Add serie resistor between driver output and transmission line
  - Cut waveform in half before going out on transmission line
  - Reflection at end is +1 (high impedance reciever => open end)
    - Total voltage at end is 2*wave = 2*1/2 signal = 1! Full swing!
  - Reflected signal is killed at the source when arriving due to the source termination
  - Drive current goes to zero when reflected wave arrives

Serie resistor selection

- Cascading driver internal resistance with serie resistance. Sum must equal Z0
- NOTE: Not possible to daisy chain recievers in source termination case!
- How close must source termination be?
  - A small stub between the driver and source termination will produce reflection (e.g., bonding wires + pcb wires)
  - The stub is inductive => large impedance for high frequency

Comparison end vs source termination

- Source usually resistive plus small inductance
- End usually capacitive
- Mismatch between Z0 and capacitive load in end termination probably worse than serie resistor mismatch (usually less reflections in source termination)
- Worst case drive current is $\Delta V/2Z0$. For end termination with Vcc/2 bias this is also true (voltage swing is only half, but Z0 impedance)

AC Biasing

- Use a capacitance in series with the end termination resistance R, R=Z0
- Must have a DC balanced signal (equal time in 1 and 0 state)
- Waste less current (split terminator always have a current from Vcc to Gnd)
- The driving circuit does not see any difference

Accuracy requirements for termination

- Problem knowing both transmission line impedance and resistor value
- Safe choise: source and end termination
  - Kill reflections in both ends

How to fit a 5mm wide cable to a 1 mm chip

- Physical scaling of dimensions
- Tapered connections