3 — Solutions and Comments to Exercises

In this section we present suggested solutions to the exercises given in Section 2.

3.1 — DC analysis

1. DC analysis on a common-source gain stage with cascodes.

   We neglect the body effect and channel-length modulation in the DC calculations (AC analysis is performed in Ex. 9).

   We define the effective gate-source voltage of an NMOS transistor as

   $$V_{eff,n} = V_{GS} - V_T \tag{1.1}$$

   and, similarly, the effective source-gate voltage of a PMOS transistor as

   $V_{eff,p} = V_{SG} - V_T$ (different V_T for NMOS and PMOS transistors!)

   We have the simplified current equation for a saturated transistor

   $$I_D \approx \alpha \cdot V_{eff}^2 \tag{1.2}$$

   Since the transistor sizes are equal for $M1$ and $M2$, and they have the same drain current, they will also have the same V_{eff}. Similarly, $M3$ and $M4$ will have the same V_{eff}.

   For NMOS transistors ($M1$ and $M2$)

   $$V_{eff,n} = \sqrt{\frac{I_D}{\alpha}} \approx 0.105 \text{ V} \tag{1.3}$$

   and for PMOS transistors

   $$V_{eff,p} = \sqrt{\frac{I_D}{\alpha}} \approx 0.185 \text{ V} \tag{1.4}$$

   (α different for NMOS and PMOS transistors!)

   Thus, $V_{in,DC} = V_{eff,n} + V_T = 0.105 + 0.47 \approx 0.58$ V. $V_{bias,2}$ is not determined by the current alone, we also need to know V_{DS} for $M1$. We have

   $$V_{bias,2} = V_{DS,1} + V_{GS,2} = V_{DS,1} + V_{eff,n} + V_T \tag{1.5}$$

   To ensure that $M1$ is properly saturated we choose

   $$V_{DS,1} = V_{eff,n} + 0.2 \text{ V} \tag{1.6}$$

   and thus

   $$V_{bias,2} = 2 \cdot V_{eff,n} + V_T + 0.2 \text{ V} \approx 0.88 \text{ V} \tag{1.7}$$

   We make a similar analysis for the PMOS part and find that

   $$V_{bias,4} = V_{DD} - (V_{eff,p} + V_T) = 3.3 - (0.185 + 0.62) \approx 2.50 \text{ V} \tag{1.8}$$

   To ensure that $M4$ is properly saturated we set

   $V_{SD,4} = V_{eff,p} + 0.2$ V and find that

   $V_{bias,3} = V_{DD} - (2 \cdot V_{eff,p} + V_T + 0.2) \approx 3.3 - (2 \cdot 0.185 + 0.62 + 0.2) = 2.11$ V

   The output range is now given by the following relations

   $$V_{out} \geq V_{DS,1} + V_{eff,n} = 2 \cdot V_{eff,n} + 0.2 \approx 0.41 \text{ V} \tag{1.9}$$

and

$$V_{out} \leq V_{DD} - (V_{SD,4} + V_{eff,p}) = V_{DD} - (2 \cdot V_{eff,p} + 0.2) \approx 2.73 \text{ V} \qquad (1.10)$$

2. DC analysis on a bias circuit.

Here we assume that all transistors are operating in the saturation region and that the channel-length modulation is neglected. Choose a suitable value of V_x, e.g., $V_x = 2V$. The maximum current through the circuit is

$$I_D \leq \frac{P_{diss}}{V_{DD}} = 5\mu A \qquad (2.1)$$

The current through all the transistors is equal and

$$I_D = \frac{K_1}{2}\frac{W_1}{L_1}(V_{DD} - V_x - V_{T1})^2 \qquad (2.2)$$

$$I_D = \frac{K_2}{2}\frac{W_2}{L_2}(V_x - V_{bias} - V_{T2})^2 \qquad (2.3)$$

$$I_D = \frac{K_3}{2}\frac{W_3}{L_3}(V_{bias} - V_{T3})^2. \qquad (2.4)$$

Moreover,

$$V_{T2} = V_{T0} + \gamma(\sqrt{2\Phi_F - V_{SB}} - \sqrt{2\Phi_F}). \qquad (2.5)$$

Eq. (2.1) and Eq. (2.4) gives

$$\frac{W_3}{L_3} = \frac{2I_D}{K_3(V_{bias} - V_{T3})^2} \approx 3.3. \qquad (2.6)$$

Eq. (2.1) and Eq. (2.2) gives

$$\frac{W_1}{L_1} = \frac{2I_D}{K_1(V_{DD} - V_x - V_{T1})^2} \approx 0.37. \qquad (2.7)$$

Eq. (2.5) yields

$$V_{T2} = 0.846V, \qquad (2.8)$$

and from Eq. (2.1) and Eq. (2.3) we obtain

$$\frac{W_2}{L_2} = \frac{2I_D}{K_2(V_x - V_{bias} - V_{T2})^2} \approx 0.56. \qquad (2.9)$$

3. DC analysis on a common-gate amplifier.

a) The transistor M_1 is in the cut-off regime as long as $V_{b1} - V_{T1} < V_1$ no (very small) current will flow through transistor M_1 so the output voltage will be equal to V_{dd}.

When the input voltage is lower than, but close to, $V_{b1} - V_{T1}$ the transistor will be

saturated since $V_{DS} = V_{out} - V_1 > V_{b1} - V_1 - V_T > 0$, and V_{out} is close to $V_{dd} \geq V_{b1}$. The input voltage for which the transistor M_1 enters the linear region is depending on the value of V_{b1}, and can be computed as follows.

b) The current through transistor M_1 in saturation is

$$I_{D1} = \alpha(V_{b1} - V_1 - V_{T1})^2(1 + \lambda(V_{out} - V_1)) \qquad (3.1)$$

In saturation the current through transistor M_1 must equal I_{bias}.

$$I_{bias} = \alpha(V_{b1} - V_1 - V_{T1})^2(1 + \lambda(V_{out} - V_1)) \qquad (3.2)$$

Solving for $V_{out} - V_1$ gives the following expression.

$$V_{out} - V_1 = \frac{1}{\lambda}\frac{I_{bias}}{\alpha(V_{b1} - V_1 - V_{T1})} - \frac{1}{\lambda} \qquad (3.3)$$

The transistor operates in the saturation region when $V_{out} - V_1 = V_{b1} - V_1 - V_{T1}$. Inserting Eq. (3.3) into previous equation and solving for V_1 gives the input voltage where the transition between the saturation and linear operation appears.

3.2 — AC analysis

4. Derivation of small-signal parameters.

a) In the linear region we have the following expression for the current I_D.

$$I_D \approx \mu_0 \cdot C_{ox} \cdot \frac{W}{L} \cdot \left((V_{GS} - V_T) \cdot V_{DS} - \frac{V_{DS}^2}{2}\right) \qquad (4.1)$$

Further we have

$$g_m = \frac{dI_D}{dV_{GS}} = \mu_0 \cdot C_{ox} \cdot \frac{W}{L} \cdot V_{DS} \qquad (4.2)$$

$$g_{ds} = \frac{dI_D}{dV_{DS}} = \mu_0 \cdot C_{ox} \cdot \frac{W}{L} \cdot (V_{GS} - V_T - V_{DS}) \qquad (4.3)$$

I_D is affected by the bulk-source voltage through variations in the threshold voltage, i.e.,

$$g_{mbs} = \frac{dI_D}{dV_{BS}} = \frac{\partial I_D}{\partial V_T} \cdot \frac{\partial V_T}{\partial V_{BS}} = -g_m \cdot \frac{\partial V_T}{\partial V_{BS}} \qquad (4.4)$$

We have the following relation for the threshold voltage

$$V_T \approx V_{T,0} + \gamma(\sqrt{2\Phi_F - V_{BS}} - \sqrt{2\Phi_F}) \qquad (4.5)$$

yielding

$$\frac{\partial V_T}{\partial V_{BS}} = -\frac{\gamma}{2 \cdot \sqrt{2\Phi_F - V_{BS}}} \qquad (4.6)$$

and thus

$$g_{mbs} = \frac{\gamma}{2 \cdot \sqrt{2\Phi_F - V_{BS}}} \cdot g_m \qquad (4.7)$$

This relation is also valid in the saturated region.

b) In the saturated region we have the following expression for I_D

$$I_D \approx \frac{\mu_0 \cdot C_{ox}}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_T)^2 \cdot (1 + \lambda \cdot V_{DS}) \tag{4.8}$$

Thus

$$g_m = \frac{dI_D}{dV_{GS}} \approx \mu_0 \cdot C_{ox} \cdot \frac{W}{L} \cdot (V_{GS} - V_T) = \sqrt{\left(\mu_0 \cdot C_{ox} \cdot \frac{W}{L} \cdot (V_{GS} - V_T)\right)^2}$$
$$\approx \sqrt{2 \cdot \mu_0 \cdot C_{ox} \cdot \frac{W}{L} \cdot I_D} \tag{4.9}$$

and

$$g_{ds} = \frac{dI_D}{dV_{DS}} = \frac{\mu_0 \cdot C_{ox}}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_T)^2 \cdot \lambda \approx \lambda \cdot I_D \tag{4.10}$$

5. Simple gain stages with resistive load.

First considering the common-source stage.

a) The ESSS is shown in Figure 30. Where $R = 1/G$.

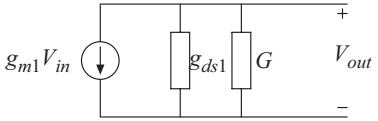


Figure 30: The ESSS of a common-source gain stage with resistive load.

b) The transfer function can be computed by using nodal analysis in the output node.

$$g_{m1}V_{in} + V_{out}(g_{ds1} + G) = 0 \tag{5.1}$$

The transfer function is

$$\frac{V_{out}}{V_{in}} = -\frac{g_{m1}}{g_{ds1} + G} \tag{5.2}$$

The output resistance can be computed by adding a voltage source V_x between the output node and ground. Then compute the current delivered by that voltage source when the input source/sources is zero (V_{in} equals zero).

$$\left.\frac{V_x}{I_x}\right|_{V_{in}=0} = \frac{1}{g_{ds1} + G} = R \parallel \frac{1}{g_{ds1}} \tag{5.3}$$

c) The transistor M_1 is in the cut-off regime when V_{in} is below V_T, yielding the output voltage equal to V_{DD}. Increasing the input voltage will give the

$V_{ds1} > V_{gs1} - V_{T1} > 0$ and the transistor will operate in the saturation region and the output voltage will decrease quadratically with the input voltage. Increasing the voltage further will result in a transistor operating in the linear region and the output voltage will then decrease linearly with the input voltage.

d) Obviously, $V_{in} > V_T$. In the saturation region it holds that

$$V_{out} \approx V_{DD} - R\alpha(V_{in} - V_T)^2. \tag{5.4}$$

For saturation it is required that

$$V_{out} \geq V_{in} - V_T. \tag{5.5}$$

Combining Eq. (5.4) and Eq. (5.5) yields

$$(V_{in} - V_T)^2 + \frac{(V_{in} - V_T)}{R\alpha} - \frac{V_{DD}}{R\alpha} \leq 0. \tag{5.6}$$

The maximum input voltage is computed with equality in Eq. (5.6), hence

$$V_{in,\,max} = V_T - \frac{1}{2R\alpha} + \sqrt{\frac{1}{4R^2\alpha^2} + \frac{V_{DD}}{R\alpha}} \tag{5.7}$$

(The solution $\ldots - \sqrt{\ldots}$ is obviously false, since it yields $V_{in,\,max} < V_T$)

a) The ESSS of the common drain, common gate, and CMOS inverter is shown in Figure 31.

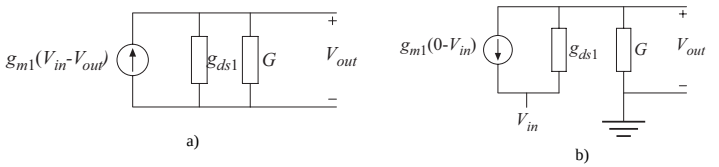


Figure 31: The ESSS for the a) common drain and b) common gate

b) Using nodal analysis at the output node gives the following DC gain and output resistance.

	CS	CD	CG
DC gain	$-\frac{g_{m1}}{g_{ds1} + G}$	$\frac{g_{m1}}{g_{m1} + g_{ds1} + G}$	$\frac{g_{m1}}{g_{ds1} + G}$
Output resistance	$\frac{1}{g_{ds1} + G}$	$\frac{1}{g_{m1} + g_{ds1} + G}$	$\frac{1}{g_{ds1} + G}$

c) Common-drain amplifier: The transistor M_1 is cut off until $V_{in} < V_{out} + V_T$. Then will it be in the saturation region.

Common-gate amplifier: The transistor will be in the linear or saturation region when the input voltage is low. An increased voltage will result that the transistor will be cut off.

d)

e) The ESSS of the common-drain circuit with the bulk effect is shown in Figure 32.

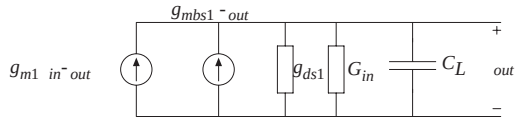


Figure 32: The ESSS of the common-drain circuit including the bulk effect.

The transfer function is given by

$$\frac{V_{out}}{V_{in}} = \frac{g_{m1}}{g_{m1} + g_{mbs1} + g_{ds1} + G_{in}} \tag{5.8}$$

The ESSS of the common-gate amplifier when the bulk effect is considered is shown in Figure 33.

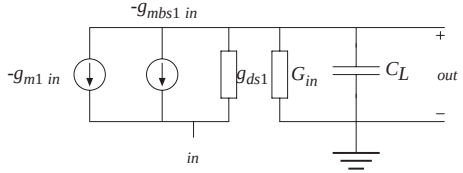


Figure 33: The ESSS of a common-gate amplifier when the bulk effect is considered.

The transfer function is

$$\frac{V_{out}}{V_{in}} = \frac{g_{ds1} + g_{m1} + g_{mbs1}}{g_{ds1} + G_{in}} \tag{5.9}$$

6. Common-gate amplifier with non ideal input source.
The small-signal equivalent is shown in Figure 34 where $R_{in} = 1/G_{in}$.

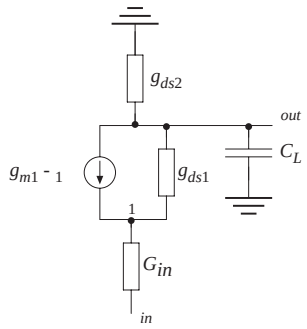


Figure 34: ESSS for the common-gate amplifier valid for low frequencies.

Using nodal analysis in the nodes V_1 and V_{out} gives the following equations

$$-g_{m1}V_1 + (V_{out} - V_1)g_{ds1} + (V_{in} - V_1)G_{in} = 0 \tag{6.1}$$

$$-g_{m1}V_1 + (V_{out} - V_1)g_{ds1} + V_{out}(g_{ds2} + sC_L) = 0 \tag{6.2}$$

Solving for V_1 in Eq. (6.1) and inserting it into Eq. (6.2) results in

$$\frac{V_{out}}{V_{in}} = \frac{G_{in}(g_{m1} + g_{ds1})}{g_{ds1}G_{in} + g_{ds2}(G_{in} + g_{m1} + g_{ds1}) + sC_L(g_{m1} + G_{in} + g_{ds1})} \approx \frac{G_{in}g_{m1}}{g_{ds1}G_{in} + g_{ds2}(G_{in} + g_{m1}) + sC_L(g_{m1} + G_{in})} \tag{6.3}$$

where $g_{m1} \gg g_{ds1}$ is assumed.

The DC gain is computed by setting $s = 0$ and the location of the first pole is computed from Eq. (6.3) by comparing with the transfer function

$$\frac{V_{out}}{V_{in}} = \frac{A_0}{1 + \frac{s}{p_1}} \tag{6.4}$$

The DC gain and the first pole can then be expressed as

$$A_0 \approx \frac{G_{in}g_{m1}}{g_{ds2}(g_{m1} + G_{in}) + g_{ds1}G_{in}} \tag{6.5}$$

$$p_1 = \frac{g_{ds2}(g_{m1} + G_{in}) + g_{ds1}G_{in}}{(g_{m1} + G_{in})C_L} \tag{6.6}$$

b) C_{gs1} is connected from node V_1 to ground. The nodal analysis in node V_1 and V_{out} gives:

$$-g_{m1}V_1 + (V_{out} - V_1)g_{ds1} + (V_{in} - V_1)G_{in} - V_1 sC_{gs1} = 0 \quad (6.7)$$

$$g_{m1}V_1 + (V_{out} - V_1)g_{ds1} + V_{out}(g_{ds2} + sC_L) = 0 \quad (6.8)$$

Solving for V_1 in Eq. (6.8)

$$\frac{V_1}{V_{out}} = \frac{g_{ds1} + g_{ds2} + sC_L}{g_{m1} + g_{ds1}} \quad (6.9)$$

Inserting into Eq. (6.7) gives

$$\frac{V_{out}}{V_{in}} = \frac{G_{in}(g_{m1} + g_{ds1})}{a + bs + cs^2} \quad (6.10)$$

where

$$a = g_{ds1}G_{in} + g_{ds2}(G_{in} + g_{m1} + g_{ds1}) \quad (6.11)$$

$$b = C_{gs1}(g_{ds1} + g_{ds2}) + C_L(g_{ds1} + G_{in} + g_{m1}) \quad (6.12)$$

$$c = C_{gs1}C_L \quad (6.13)$$

The load capacitance is often much larger than the parasitic capacitances. This results in that the load capacitor will be give rise to the dominant pole and the parasitic capacitances will contribute to the pole located much higher in frequency. When it is a large difference between the capacitances, the poles will be well separated. For well separated poles the following approximation holds.

$$\left(1 + \frac{s}{p_1}\right)\left(1 + \frac{s}{p_2}\right) = 1 + s\left(\frac{1}{p_1} + \frac{1}{p_2}\right) + \frac{s^2}{p_1 p_2} \approx 1 + \frac{s}{p_1} + \frac{s^2}{p_1 p_2} \quad (6.14)$$

Comparing Eq. (6.14) and Eq. (6.10) gives the following poles.

$$p_1 \approx \frac{a}{b} = \frac{g_{ds1}G_{in} + g_{ds2}(G_{in} + g_{m1} + g_{ds1})}{C_{gs1}(g_{ds1} + g_{ds2}) + C_L(g_{ds1} + G_{in} + g_{m1})} \approx \frac{g_{ds1}G_{in} + g_{ds2}(G_{in} + g_{m1})}{C_L(G_{in} + g_{m1})} \quad (6.15)$$

$$p_2 \approx \frac{a}{cp_1} = \frac{b}{c} \approx \frac{g_{ds1} + G_{in} + g_{m1}}{C_{gs1}} \quad (6.16)$$

7. Amplifier stages with active load.

a) The ESSS of the four amplifier stages is shown in Figure 35.

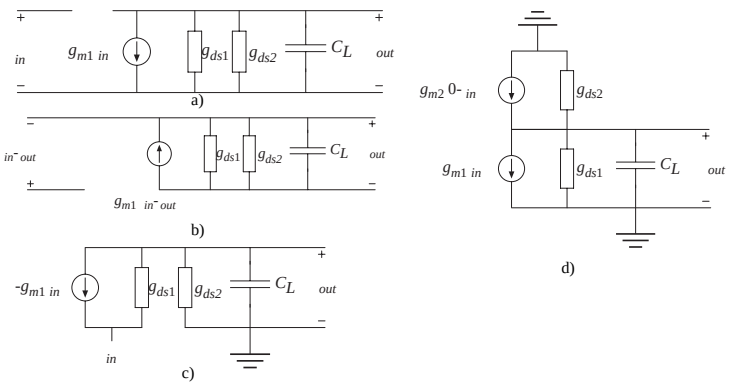


Figure 35: The ESSS of the amplifiers with active load. a) Common source, b) common drain, c) common gate, and d) CMOS inverter

The bulk effect is neglected.

b and c) To calculate the DC gain and the dominating pole only the capacitance C_L needs to be considered.

Nodal analysis of the *common-source* amplifier

$$g_{m1}V_{in} + V_{out}(g_{ds1} + g_{ds2} + sC_L) = 0 \quad (7.1)$$

gives the transfer function

$$\frac{V_{out}}{V_{in}} = -\frac{g_{m1}}{g_{ds1} + g_{ds2} + sC_L} = -\frac{g_{m1}}{g_{ds1} + g_{ds2}} \frac{1}{1 + \frac{s}{\frac{g_{ds1} + g_{ds2}}{C_L}}} = -\frac{A_0}{1 + \frac{s}{p_1}} \quad (7.2)$$

where A_0 is the DC gain and p_1 is the dominating pole.

The output resistance is compute by adding a voltage source at the output, V_x, and compute the current delivered from the source when the input source is zeroed. This gives $I_x = V_x(g_{ds1} + g_{ds2})$ and the output resistance

$$r_{out} = \frac{V_x}{I_x} = \frac{1}{g_{ds1} + g_{ds2}} \quad (7.3)$$

Nodal analysis for the *common-drain* amplifier

$$-g_{m1}(V_{in} - V_{out}) + V_{out}(g_{ds1} + g_{ds2} + sC_L) = 0 \quad (7.4)$$

gives the transfer function

$$\frac{V_{out}}{V_{in}} = \frac{g_{m1}}{g_{m1}+g_{ds1}+g_{ds2}} \frac{1}{1+\dfrac{s}{\dfrac{g_{m1}+g_{ds1}+g_{ds2}}{C_L}}} \tag{7.5}$$

The output current through the output source equals $I_x = V_x(g_{ds1}+g_{ds1}+g_{m1})$ and the output resistance

$$r_{out} = \frac{V_x}{I_x} = \frac{1}{g_{ds1}+g_{ds2}+g_{m1}} \tag{7.6}$$

The *common-gate* amplifier:

$$-g_{m1}V_{in} + (V_{out}-V_{in})g_{ds1} + V_{out}(g_{ds2}+sC_L) = 0 \tag{7.7}$$

gives the transfer function

$$\frac{V_{out}}{V_{in}} = \frac{g_{m1}+g_{ds1}}{g_{ds1}+g_{ds2}} \frac{1}{1+\dfrac{s}{\dfrac{g_{ds1}+g_{ds2}}{C_L}}} \tag{7.8}$$

The output current through the output source equals $I_x = V_x(g_{ds1}+g_{ds2})$ an the output resistance

$$r_{out} = \frac{V_x}{I_x} = \frac{1}{g_{ds1}+g_{ds2}} \tag{7.9}$$

The *CMOS inverter*

$$(g_{m1}+g_{m2})V_{in} + (g_{ds1}+g_{ds2}+sC_L)V_{out} = 0 \tag{7.10}$$

giving the transfer function

$$\frac{V_{out}}{V_{in}} = -\frac{g_{m1}+g_{m2}}{g_{ds1}+g_{ds2}} \frac{1}{1+\dfrac{s}{\dfrac{g_{ds1}+g_{ds2}}{C_L}}} \tag{7.11}$$

The output resistance is given by

$$r_{out} = \frac{V_x}{I_x} = \frac{1}{g_{ds1}+g_{ds2}} \tag{7.12}$$

Summary:

	DC gain	**Output resistance**	**Bandwidth**
Common source	$-\dfrac{g_{m1}}{g_{ds1}+g_{ds2}}$	$\dfrac{1}{g_{ds1}+g_{ds2}}$	$\dfrac{g_{ds1}+g_{ds2}}{C_L}$

Common drain	$\dfrac{g_{m1}}{g_{m1}+g_{ds1}+g_{ds2}}$	$\dfrac{1}{g_{m1}+g_{ds1}+g_{ds2}}$	$\dfrac{g_{m1}+g_{ds1}+g_{ds2}}{C_L}$
Common gate	$\dfrac{g_{m1}+g_{ds1}}{g_{ds1}+g_{ds2}}$	$\dfrac{1}{g_{ds1}+g_{ds2}}$	$\dfrac{g_{ds1}+g_{ds2}}{C_L}$
CMOS inverter	$-\dfrac{g_{m1}+g_{m2}}{g_{ds1}+g_{ds2}}$	$\dfrac{1}{g_{ds1}+g_{ds2}}$	$\dfrac{g_{ds1}+g_{ds2}}{C_L}$

In principle we can see that in a single stage amplifier the DC gain can approximately be expressed as $g_{m,in}/g_{out} = g_{m,in}r_{out}$ and the bandwidth is $g_{out}/C_L = 1/(r_{out}C_L)$.

d) The highest gain is obtained in a CMOS inverter. The circuit with highest bandwidth is the common-drain amplifier.

8. Current mirrors.

a) The ESSS of the simple current mirror is shown in Figure 36a.

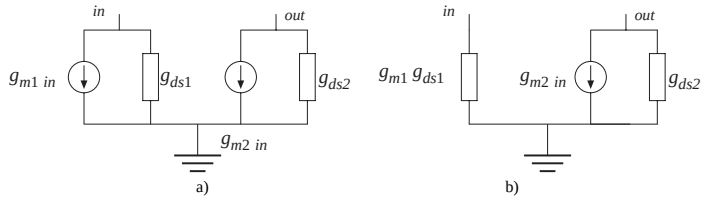


Figure 36: a) The ESSS for the simple current mirror. b) Simplified ESSS for the simple current mirror.

The input resistance is computed by adding a input voltage source to V_{in} and computing the current delivered by the source. The output should be terminated by the resistive load R_{load}.

$$I_{in} = g_{m1}V_{in} + V_{in}g_{ds1} = V_{in}(g_{ds1}+g_{m1}) \tag{8.1}$$

We see that if a transistor has a connection between its drain and gate, called diode-connected, the small-signal model will be a resistor with the value $g_{m1}+g_{ds1}$ as shown in Figure 36b. The input resistance is

$$r_{in} = \frac{V_{in}}{I_{in}} = \frac{1}{g_{m1}+g_{ds1}} \tag{8.2}$$

The output resistance is computed by adding a voltage source at the output and computing the current it delivers. This will give the output resistance equal to

$$r_{out} = \left.\frac{V_{out}}{I_{out}}\right|_{I_{in}=0} = \frac{1}{g_{ds2}} \tag{8.3}$$

The ESSS of the cascode current mirror is shown in Figure 37.

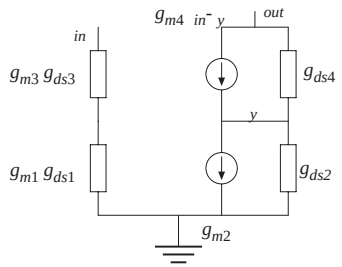


Figure 37: The ESSS of a cascode current mirror.

The input current is given by $I_{in} = (V_{in} - V_x)(g_{m3} + g_{ds3}) = V_x(g_{m1} + g_{ds1})$. The node voltage V_x can be eliminated from the equations and the output resistance is given by

$$r_{in} = \frac{V_{in}}{I_{in}} = \frac{g_{m1} + g_{ds1} + g_{m3} + g_{ds3}}{(g_{m1} + g_{ds1})(g_{m3} + g_{ds3})} \approx \frac{g_{m1} + g_{m3}}{g_{m1}g_{m3}} = \frac{1}{g_{m1}} + \frac{1}{g_{m3}} \tag{8.4}$$

The output current is given by

$$I_{out} = g_{m4}(-V_y) + g_{ds4}(V_{out} - V_y) = g_{m2}0 + g_{ds2}V_y \tag{8.5}$$

since $I_{in} = 0$ and thereby is $V_x = 0$. The output resistance is given by

$$r_{out} = \frac{V_{out}}{I_{out}} = \frac{g_{ds2} + g_{ds4} + g_{m4}}{g_{ds2}g_{ds4}} \approx \frac{g_{m4}}{g_{ds2}g_{ds4}} \tag{8.6}$$

The ESSS of the wide-swing current mirror is shown in Figure 38.

The input current equals $I_{in} = g_{m3}(-V_x) + (V_{in} - V_x)g_{ds3} = V_{in}g_{m1} + V_x g_{ds1}$. The input resistance is

$$r_{in} = \frac{V_{in}}{I_{in}} = \frac{g_{ds1} + g_{ds3} + g_{m3}}{g_{m1}(g_{ds3} + g_{m3}) + g_{ds1}g_{ds3}} \approx \frac{g_{m3}}{g_{m1}(g_{ds3} + g_{m3})} = \frac{1}{g_{m1}} \tag{8.7}$$

The output current is given by

$$I_{out} = g_{m4}(-V_y) + g_{ds4}(V_{out} - V_y) = g_{m2}0 + g_{ds2}V_y \tag{8.8}$$

The output resistance is

$$r_{out} = \frac{V_{out}}{I_{out}} = \frac{g_{ds2} + g_{ds4} + g_{m4}}{g_{ds2}g_{ds4}} \approx \frac{g_{m4}}{g_{ds2}g_{ds4}} \tag{8.9}$$

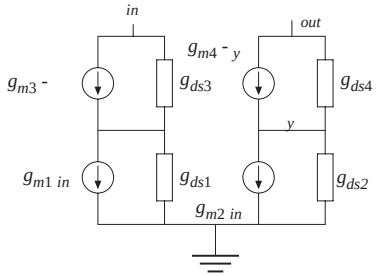


Figure 38: The ESSS of a wide-swing current mirror.

b) The lowest possible V_{ds} of a transistor in the saturation region, V_{dssat}, is $V_{dssat} = V_{gs} - V_T$. The V_{dssat} is expressed as a function of the drain current in a transistor in the following way.

$$I_D = \alpha(V_{gs} - V_T)^2 = \alpha V_{dssat}^2 \tag{8.10}$$

Solving for V_{dssat} gives

$$V_{dssat} = \sqrt{\frac{I_D}{\alpha}} \tag{8.11}$$

The minimum gate source voltage for a transistor that is operating in the saturation region is

$$V_{gsmin} = V_{dssat} + V_T = \sqrt{\frac{I_D}{\alpha}} + V_T \tag{8.12}$$

The minimum voltage is derived by determining the minimum voltage required to ensure that all transistors are operating in the saturation region for each possible way from ground to the node of interest, not passing directly between the gate to the drain.

The lowest possible input/output voltage of the simple current mirror is

$$V_{inmin} = max\{V_{gsmin1}, V_{dssat1}\} = V_{gsmin1} = \sqrt{\frac{I_{in}}{\alpha_1}} + V_{T1} \tag{8.13}$$

$$V_{outmin} = V_{dssat2} = \sqrt{\frac{I_{out}}{\alpha_2}} \tag{8.14}$$

The lowest possible input/output voltage for the cascode current mirror is

$$V_{inmin} = V_{gsmin1} + V_{gsmin3} = \sqrt{\frac{I_{in}}{\alpha_1}} + V_{T1} + \sqrt{\frac{I_{in}}{\alpha_3}} + V_{T3} \tag{8.15}$$

$$V_{outmin} = max\{V_{dssat2} + V_{dssat4}, V_{gsmin1} + V_{gsmin3} - V_{gsmin4} + V_{dssat4}\} = \sqrt{\frac{I_{in}}{\alpha_1}} + V_{T1} + \sqrt{\frac{I_{in}}{\alpha_3}} + V_{T3} - \sqrt{\frac{I_{out}}{\alpha_4}} - V_{T4} + \sqrt{\frac{I_{out}}{\alpha_4}} = \sqrt{\frac{I_{in}}{\alpha_1}} + V_{T1} + \sqrt{\frac{I_{in}}{\alpha_3}} + V_{T3} - V_{T4} \quad (8.16)$$

The lowest possible input/output/bias voltage for the wide-swing current mirror is.

$$V_{inmin} = max\{V_{gsmin1}, V_{dssat1} + V_{dssat3}\} = \sqrt{\frac{I_{in}}{\alpha_1}} + V_{T1} \quad (8.17)$$

$$V_{outmin} = max\{V_{dssat2} + V_{dssat4}, V_{dssat1} + V_{gsmin3} - V_{gsmin4} + V_{dssat4}\} = \sqrt{\frac{I_{in}}{\alpha_1}} + \sqrt{\frac{I_{in}}{\alpha_3}} + V_{T3} - V_{T4} \quad (8.18)$$

$$V_{biasmin} = max\{V_{dssat1} + V_{gsmin3}, V_{dssat2} + V_{gsmin4}\} = max\left\{\sqrt{\frac{I_{in}}{\alpha_1}} + \sqrt{\frac{I_{in}}{\alpha_3}} + V_{T3}, \sqrt{\frac{I_{out}}{\alpha_2}} + \sqrt{\frac{I_{out}}{\alpha_3}} + V_{T4}\right\} \quad (8.19)$$

Summary:

	Simple	Cascode	Wide-Swing
Input impedance	$\frac{1}{g_{m1} + g_{ds1}}$	$\frac{1}{g_{m1}} + \frac{1}{g_{m3}}$	$\frac{1}{g_{m1}}$
Output impedance	$\frac{1}{g_{ds2}}$	$\frac{g_{m4}}{g_{ds2}g_{ds4}}$	$\frac{g_{m4}}{g_{ds2}g_{ds4}}$
Lowest input voltage	$\sqrt{\frac{I_{in}}{\alpha_1}} + V_{T1}$	$\sqrt{\frac{I_{in}}{\alpha_1}} + V_{T1} + \sqrt{\frac{I_{in}}{\alpha_3}} + V_{T3}$	$\sqrt{\frac{I_{in}}{\alpha_1}} + V_{T1}$
Lowest output voltage	$\sqrt{\frac{I_{out}}{\alpha_2}}$	$\sqrt{\frac{I_{in}}{\alpha_1}} + V_{T1} + \sqrt{\frac{I_{in}}{\alpha_3}} + V_{T3} - V_{T4}$	$\sqrt{\frac{I_{in}}{\alpha_1}} + \sqrt{\frac{I_{in}}{\alpha_3}} + V_{T3} - V_{T4}$
Lowest bias voltage	-	-	See above

c) The current mirror that is most ideal is the wide swing and cascode current mirror since they have the lowest input resistance and the highest output resistance. But by looking at the possible input/output voltage the wide-swing current mirror is best. If the chip area is of concern then the simplest current mirror is the one to

choose. Depending on the application each of these current mirrors can be the best choice.

9. Gain stages with cascodes.

a) A gain-boosted common-source amplifier.

b) We first compute the output impedance of a cascode as shown in Figure 39a

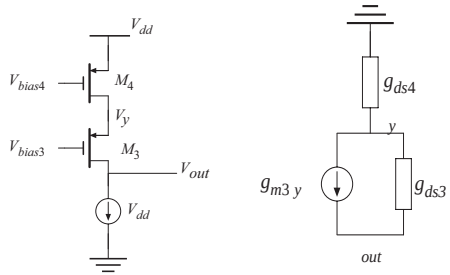


Figure 39: a) A cascode transistor. b) The ESSS of the circuit.

with the ESSS as shown in Figure 39b. The current I_{out} is

$$I_{out} = V_y g_{ds4} = -g_{m3}V_y - g_{ds3}(V_y - V_{out}) \quad (9.1)$$

The output resistance is

$$r_{out} = \frac{V_{out}}{I_{out}} = \frac{g_{m3} + g_{ds3} + g_{ds4}}{g_{ds3}g_{ds4}} \approx \frac{g_{m3}}{g_{ds3}g_{ds4}} = \frac{A_3}{g_{ds4}} \quad (9.2)$$

where A_3 is the gain of the transistor M_3. The two transistors above can be replaced by a resistor with the values of A_3/g_{ds4} when we are computing the small-signal characteristics.

The simplified ESSS of the amplifier is shown in Figure 40. The DC gain can be computed using the following equations.

$$g_{m1}V_{in} + V_x g_{ds1} + g_{m2}V_x + (V_x - V_{out})g_{ds2} = 0 \quad (9.3)$$

$$(-g_{m2})V_x + (V_{out} - V_x)g_{ds2} + V_{out}G = 0 \quad (9.4)$$

Solving for V_{out} gives the following DC gain.

$$\frac{V_{out}}{V_{in}} = -\frac{g_{m1}(g_{m2} + g_{ds2})}{g_{ds1}g_{ds2} + G(g_{ds1} + g_{ds2} + g_{m2})} \approx -\frac{g_{m1}}{\frac{g_{ds1}g_{ds2}}{g_{m2}} + G} = -\frac{g_{m1}}{\frac{g_{ds1}g_{ds2}}{g_{m2}} + \frac{g_{ds3}g_{ds4}}{g_{m3}}} \quad (9.5)$$

The DC gain can be expressed as g_{m1}/g_{out} where the output conductance is the sum of the conductances seen from the output to ground and from the output to

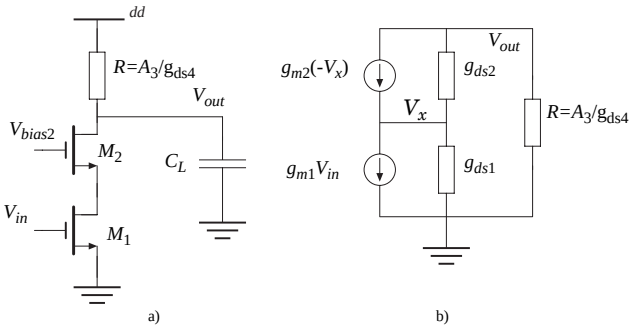


Figure 40: a) Equivalent low frequency folded cascode amplifier. b) ESSS of the simplified amplifier.

the positive supply voltage (the parallel connection of the two output resistances seen up and down from the output). The cascode transistors are used to enhance the output resistance by the gain of the cascode transistors, i.e. g_{m2}/g_{ds2} and g_{m3}/g_{ds3} respectively.

The DC gain of the gain-boosted amplifier can be calculated in the same way as the cascode transistors. The upper part of the transistor together with its small-signal equivalent is shown in Figure 41

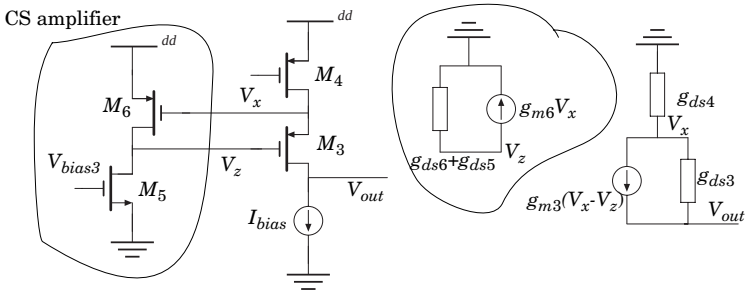


Figure 41: A part of the gain-boosted cascode transistor.

We start to calculate the DC gain of the common-source amplifier to

$$\frac{V_z}{V_x} = -\frac{g_{m6}}{g_{ds5} + g_{ds6}} = A_{cs} \tag{9.6}$$

Continuing to derive the output resistance by setting up the current delivered by the output source.

$$I_{out} = -g_{m3}(V_x - V_z) + (V_{out} - V_x)g_{ds3} = V_x g_{ds4} \tag{9.7}$$

Solving for V_{out} and eliminating V_x gives

$$r_{out} = \frac{V_{out}}{I_{out}} = \frac{g_{ds3} + g_{ds3} + g_{m3} - A_{cs}g_{m3}}{g_{ds3}g_{ds4}} \approx \frac{A_{cs}g_{m3}}{g_{ds3}g_{ds4}} = \frac{g_{m5}}{g_{ds5} + g_{ds6}}\frac{g_{m3}}{g_{ds3}g_{ds4}} \tag{9.8}$$

The output impedance is increased by the gain of the common-source amplifier, A_{cs}.

The same type of computation as the one above will give the output DC gain of the whole circuit. The simplified small-signal schematic for the gain-boosted amplifier is shown in Figure 42.

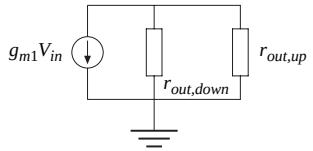


Figure 42: A simplified ESSS of the gain-boosted amplifier.

The output resistance

$$r_{out,\,up} = \frac{g_{m5}}{g_{ds5} + g_{ds6}}\frac{g_{m3}}{g_{ds3}g_{ds4}} \tag{9.9}$$

and

$$r_{out,\,down} = \frac{g_{m8}}{g_{ds8} + g_{ds7}}\frac{g_{m2}}{g_{ds2}g_{ds1}} \tag{9.10}$$

The DC gain is given by

$$\frac{V_{out}}{V_{in}} \approx \frac{g_{m1}}{g_{out}} \approx \frac{g_{m1}}{\frac{1}{r_{out,\,up}} + \frac{1}{r_{out,\,down}}} \tag{9.11}$$

c) The parasitic capacitance in the signal path for the amplifier with cascodes is much lower since we do not have the C_{gs8} in the signal path compared with the amplifier using gain boosting.

The bandwidth is g_{out}/C_L for a single stage amplifier. The output conductance of the gain boosted amplifier is much less than the one width cascodes. Hence, the bandwidth of the gain boosted amplifier is much lower than the amplifier with cascodes.

Summary:

	DC gain	First pole (bandwidth)
Common source	$-\frac{g_{m1}}{g_{ds1}+g_{ds2}}$	$\frac{g_{ds1}+g_{ds2}}{C_L}$
Common source with cascodes	$-\frac{g_{m1}}{\frac{g_{ds1}g_{ds2}}{g_{m2}}+\frac{g_{ds3}g_{ds4}}{g_{m3}}}$	$\frac{\frac{g_{ds1}g_{ds2}}{g_{m2}}+\frac{g_{ds3}g_{ds4}}{g_{m3}}}{C_L}$
Gain-boosted common-source amplifier	$-\frac{g_{m1}}{g_{out}}$	$\frac{g_{out}}{C_L}$

where $g_{out} = \frac{g_{ds1}g_{ds2}}{g_{m2}}\frac{g_{ds8}+g_{ds7}}{g_{m8}} + \frac{g_{ds3}g_{ds4}}{g_{m3}}\frac{g_{ds5}+g_{ds6}}{g_{m5}}$.

3.3 — Differential gain stage

10. A single-ended differential gain stage.

a) The OR (output range) is the possible swing at the output so that all transistors are operating in the saturation region.

$$V_{out,max} = V_{dd} - V_{sdsat4} = V_{dd} - \sqrt{\frac{I_{D4}}{\alpha_4}} = V_{dd} - \sqrt{\frac{I_{D5}}{2\alpha_4}} \tag{10.1}$$

$$V_{out,min} = V_{dssat5} + V_{dssat2} = \sqrt{\frac{I_{D5}}{\alpha_5}} + \sqrt{\frac{I_{D2}}{\alpha_2}} = \sqrt{\frac{I_{D5}}{\alpha_5}} + \sqrt{\frac{I_{D5}}{2\alpha_2}} \tag{10.2}$$

The output range is also dependent on the input voltage which results that

$$V_{out,min} = V_{in} - V_{gs2} + V_{ds2} = V_{in} - V_{T2} \tag{10.3}$$

which results in a minimum output voltage for all transistors operating in the saturation region equal to

$$V_{out,min} = max\left\{\sqrt{\frac{I_{D5}}{\alpha_5}} + \sqrt{\frac{I_{D5}}{2\alpha_2}}, V_{in} - V_{T2}\right\} \tag{10.4}$$

The common-mode range is the possible input swing.

$$V_{in,min} = V_{dssat5} + V_{gs1} = \sqrt{\frac{I_{D5}}{\alpha_5}} + \sqrt{\frac{I_{D5}}{2\alpha_1}} + V_{T1} \tag{10.5}$$

$$V_{in,max} = V_{DD} - V_{gs3} - V_{dssat1} + V_{gs1} =$$
$$V_{DD} - \sqrt{\frac{I_{D3}}{\alpha_3}} - V_{T3} + V_{T1} = V_{DD} - \sqrt{\frac{I_{D5}}{2\alpha_3}} - V_{T3} + V_{T1} \tag{10.6}$$

The ESSS of the differential gain stage is shown in Figure 43.

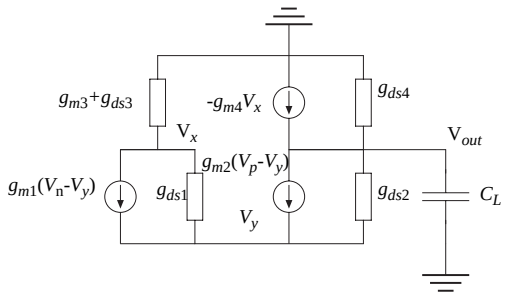


Figure 43: The ESSS of a single-ended differential gain stage.

It is assumed that transistors M_1 and M_2 are equally sized, as well as transistors M_3 and M_4. If the currents in both branches of the differential gain stage are equal, then $g_{m1} \approx g_{m2}$, $g_{ds1} \approx g_{ds2}$,$g_{m3} \approx g_{m4}$, and $g_{ds3} \approx g_{ds4}$. The following expressions hold for the circuit in Figure 43:

$$(g_{m3} + g_{ds3})V_x + g_{m1}(V_n - V_y) + g_{ds1}(V_x - V_y) = 0, \tag{10.7}$$

$$g_{m1}(V_n - V_y) + g_{ds1}(V_x - V_y) + g_{m1}(V_p - V_y) + g_{ds1}(V_{out} - V_y) = 0, \tag{10.8}$$

and

$$g_{m1}(V_p - V_y) + g_{ds1}(V_{out} - V_y) + g_{m3}V_x + V_{out}(sC_L + g_{ds3}) = 0. \tag{10.9}$$

Solving for V_{out} yields

$$V_{out} = \frac{(g_{ds3} + 2g_{m3})g_{m1}(V_p - V_n)}{2(g_{ds1} + g_{ds3})(g_{ds3} + g_{m3}) + sC_L(g_{ds1} + 2(g_{ds3} + g_{m3}))}. \tag{10.10}$$

Assuming that $g_{m3} \gg g_{ds3}$, g_{ds1} and dividing both the numerator and denominator of Eq. (10.10) with $2g_{m3}$ yields

$$V_{out} \approx \frac{g_{m1}(V_p - V_n)}{g_{ds1} + g_{ds3} + sC_L} \tag{10.11}$$

To compute the output resistance, r_{out}, we connect an AC voltage source, V_{out}, to the output node and set $V_p = V_n = 0$ (and, of course, neglect C_L). The current delivered by V_{out} is denoted I_{out}. The following equations hold:

$$I_{out} - g_{m3}V_x - g_{ds3}V_{out} + g_{m1}V_y - g_{ds1}(V_{out} - V_y) = 0, \tag{10.12}$$

$$-2g_{m1}V_y + g_{ds1}(V_x - 2V_y + V_{out}) = 0, \tag{10.13}$$

and

$$-g_{m1}V_y + g_{ds1}(V_x - V_y) + (g_{m3} + g_{ds})V_x = 0. \tag{10.14}$$

Solving for I_{out} yields

$$I_{out} = \frac{2(g_{ds1} + g_{ds3})(g_{ds3} + g_{m3})}{g_{ds1} + 2(g_{ds3} + g_{m3})}V_{out} \approx (g_{ds1} + g_{ds3})V_{out}, \tag{10.15}$$

under the assumption that $g_{ds1} \ll 2(g_{m3} + g_{ds3})$. Hence, the output resistance is

$$r_{out} = \frac{V_{out}}{I_{out}} \approx \frac{1}{g_{ds1} + g_{ds3}} \tag{10.16}$$

and the output impedance is

$$z_{out} \approx \frac{1}{g_{ds1} + g_{ds3} + sC_L}. \tag{10.17}$$

b) The maximum current that can be delivered to the load capacitor is I_{bias}. Hence,

$$SR \approx \frac{I_{bias}}{C_L}. \tag{10.18}$$

11. Differential stage with passive load.

Here we would like to derive the differential and common-mode gain. The small-signal schemes are a little bit different.

a) The circuit is fully differential and thereby it is sufficient to compute the differential gain for half the circuit shown in Figure 44a. The differential gain is then

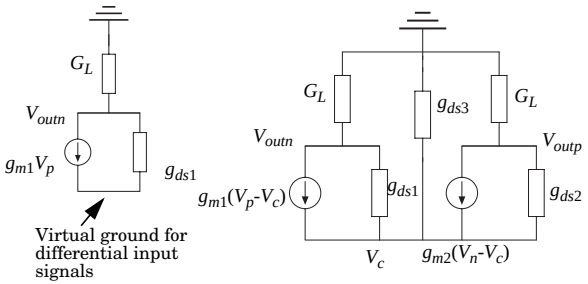


Figure 44: The ESSS of a differential gain stage for computing a) the differential gain (half circuit) and b) the gain from the common-mode input to the common-mode output voltage.

$$A_{diff} = \frac{V_{outp} - V_{outn}}{V_p - V_n} = -\frac{V_{outn}}{V_p} = \frac{g_{m1}}{g_{ds1} + G_L} \tag{11.1}$$

The second equality comes from the fact that $V_{outp} = -V_{outn}$ and $V_p = -V_n$ and

we have a fully differential gain stage. Nearly the same computation as in Exercise 10.

b) The gain from the common-mode input voltage to the common-mode output voltage is computed using nodal analysis in the ESSS shown in Figure 44b. The nodal analysis is performed in nodes V_{outn}, V_{outp} and gnd.

$$V_{outn}G_L + (V_{outn} - V_c)g_{ds1} + g_{m1}(V_p - V_c) = 0 \tag{11.2}$$

$$V_{outp}G_L + (V_{outp} - V_c)g_{ds2} + g_{m2}(V_n - V_c) = 0 \tag{11.3}$$

$$V_{outn}G_L + V_{outp}G_L + V_c g_{ds3} = 0 \tag{11.4}$$

Solving for V_c in Eq. (11.4) gives

$$V_c = -\frac{G_L}{g_{ds3}}(V_{outp} + V_{outn}) \tag{11.5}$$

Adding the Eq. (11.2) and Eq. (11.3) gives

$$\begin{aligned}(V_{outp} + V_{outn})G_L + V_{outp}g_{ds2} + V_{outn}g_{ds1} + V_p g_{m1} + V_n g_{m2} = \\ (g_{ds1} + g_{ds2} + g_{m1} + g_{m2})V_c\end{aligned} \tag{11.6}$$

The design is fully symmetrical (i.e. transistor M_1 is equal to M_2 yielding the same transconductances, g_m, and output conductances, g_{ds}). The Eq. (11.6) is then simplified to

$$(V_{outp} + V_{outn})(g_{ds} + G_L) + (V_p + V_n)g_m = 2(g_{ds} + g_m)V_c \tag{11.7}$$

Combining Eq. (11.5) and Eq. (11.7) gives the gain

$$A_{cm,cm} = \frac{\frac{V_{outp} + V_{outn}}{2}}{\frac{V_p + V_n}{2}} = -\frac{g_{ds3}g_m}{g_{ds3}(g_{ds} + G_L) + 2G_L(g_{ds} + g_m)} \tag{11.8}$$

c) The power supply rejection ration (PSRR) from the negative supply is defined as

$$PSRR_n = A_{diff} \Big/ \left(\frac{(V_{outp} - V_{outn})/2}{V_{gnd}}\right) \tag{11.9}$$

The differential gain is already computed so it is just the differential output variations due to a noisy ground line that is of interest. The small-signal model is

shown in Figure 45. The small-signal source is V_n. Nodal analysis in nodes V_n, V_p,

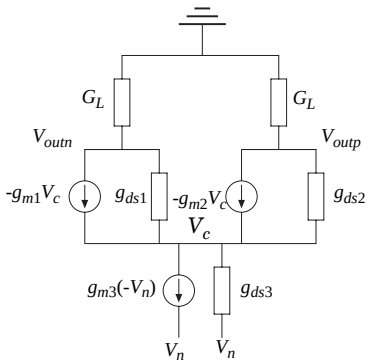


Figure 45: The ESSS for computing the negative power supply noise gain to the differential output.

and V_c gives the following equations.

$$V_{outn}G_L + (V_{outn} - V_c)g_{ds1} + g_{m1}(-V_c) = 0 \tag{11.10}$$

$$V_{outp}G_L + (V_{outp} - V_c)g_{ds2} + g_{m2}(-V_c) = 0 \tag{11.11}$$

$$-V_c g_{m1} - V_c g_{m2} + (V_{outn} - V_c)g_{ds1} + (V_{outp} - V_c)g_{ds2} + (V_n - V_c)g_{ds3} + V_n g_{m3} = 0$$

We take the difference between Eq. (11.10) and Eq. (11.11) and assuming that transistor M_1 is matched to M_2.

$$(V_{outn} - V_{outp})(G_L + g_{ds}) = 0 \tag{11.12}$$

This yields that the gain from the negative supply to the differential output is zero and thereby the negative PSRR is infinite.

3.4 — OTAs and OPs

12. OP and OTA.

An operational amplifier (OP) has ideally zero output impedance and is thus suitable for driving resistive loads, since in this way there is no voltage division between the output impedance and the load resistance. Resistive loads are most often used off-chip, but also on-chip in, e.g., active RC filters.

The operational transconductance amplifier (OTA), however, has ideally infinite output impedance and is thus suitable for driving capacitive loads, as is often the case in “on-chip” situations, such as Gm-C filters or sample-and-hold circuits.

13. Current mirror OTA.

We start by some useful relations

$$g_m \approx 2\alpha V_{eff} \approx \sqrt{4\alpha I_D} = \sqrt{2\mu C_{ox}\frac{W}{L}I_D} \tag{13.1}$$

Which gives

$$W \approx \frac{g_m^2 L}{2\mu C_{ox} I_D} \tag{13.2}$$

Furthermore,

$$g_{ds} \approx \lambda I_D \tag{13.3}$$

The total power dissipation is

$$P_{diss} = V_{dd}I_{tot} = V_{dd}I_b\left(\frac{3}{2} + \frac{K}{2}\right) \tag{13.4}$$

Where K is the current-mirror gain. Solving for I_b gives

$$I_b = \frac{2}{3+K}\frac{P_{diss}}{V_{dd}} \tag{13.5}$$

From Johns&Martin (pages 273 -)

$$SR = \frac{KI_b}{C_L} = 2\frac{P_{diss}}{C_L V_{dd}}\frac{K}{3+K} \tag{13.6}$$

$$\omega_u \approx \frac{Kg_{m1}}{C_L} \Rightarrow g_{m1} \approx \frac{C_L}{K}\omega_u \tag{13.7}$$

$$A_0 = Kg_{m1}r_{out} \Rightarrow r_{out} = \frac{A_0}{Kg_{m1}} \tag{13.8}$$

Solution:

We start with the slew-rate specification to determine the K value. Solving for K in Eq. (13.6) gives

$$K = \frac{3SR}{\frac{2P_{diss}}{V_{dd}C_L} - SR} \approx 2.36 \tag{13.9}$$

When K is chosen we get $I_b \approx 170\mu A$ and we determine W_1 by combining Eq. (13.7) and Eq. (13.2) yielding

$$W_1 = \frac{C_L^2\omega_u^2 L}{2\mu K^2 C_{ox} I_{D1}} = \frac{C_L^2\omega_u^2 L}{K^2\mu C_{ox} I_b} \approx 58\mu m \tag{13.10}$$

From Eq. (13.8) we get the required output resistance $r_{out} \approx 3.18\text{M}\Omega$.

The output stage is a common-source amplifier with cascodes like the one in the Ex. 9. The output conductance is given by the parallel combination of the nmos and pmos resistances. Here we have chosen the size of the output resistances of the nmos and pmos transistors equal to $r_p = r_n = 2r_{out}$. The pmos resistance is given by

$$r_p = \frac{1}{g_{ds8}}\frac{g_{m10}}{g_{ds10}} = \frac{g_{mp}}{g_{dsp}^2} \Rightarrow g_{mp} = r_p g_{dsp}^2 \tag{13.11}$$

Similarly

$$r_n = \frac{1}{g_{ds14}}\frac{g_{m12}}{g_{ds12}} = \frac{g_{mn}}{g_{dsn}^2} \Rightarrow g_{mn} = r_n g_{dsn}^2 \tag{13.12}$$

Here we have assumed that the size of transistors M_8 is equal to M_{10} and M_{12} is equal to M_{14} and thereby they will have the same small-signal parameters.

The DC current through the output stage is given by $I_D = I_b K/2$ and we know that $g_{ds} = \lambda I_D$. These two expression together with Eq. (13.11) and Eq. (13.12) gives

$$g_{mp} = 2r_{out}(\lambda_p I_b K/2)^2 \approx 1.5mS \tag{13.13}$$

$$g_{mn} = 2r_{out}(\lambda_n I_b K/2)^2 \approx 0.544\mu S \tag{13.14}$$

Solving for the widths by using Eq. (13.1) gives

$$W_8 = W_{10} = \frac{g_{mp}^2 L}{2\mu_p C_{ox} I_D} \approx 113\mu m \tag{13.15}$$

$$W_{12} = W_{14} = \frac{g_{mn}^2 L}{2\mu_n C_{ox} I_D} \approx 4.8\mu m \tag{13.16}$$

$$W_3 = W_4 = W_5 = W_6 = W_7 = W_9 = \frac{W_8}{K} \approx 48\mu m \tag{13.17}$$

$$W_{11} = W_{13} = \frac{W_{12}}{K} \approx 2\mu m \tag{13.18}$$

14. A simplified model of a two-stage operational transconductance amplifier.

a) A compensation circuit can for example consist of a capacitor, or a capacitor and a resistor. For a useful compensation circuit there can not be a DC path between the nodes of the compensation circuit. We use the approximation $g_m \gg g_{ds}$ and assume that M_1 and M_2 are equally sized, and that M_3 and M_4 are equally sized. Further, the bulk effect is neglected.

$$g_I = g_{ds2} + g_{ds4} \tag{14.1}$$

$$g_{II} = g_{ds6} + g_{ds7} \tag{14.2}$$

$$g_{mI} = g_{m1} = g_{m2} \tag{14.3}$$

$$g_{mII} = g_{m7} \tag{14.4}$$

$$C_I = C_{gs7} + C_{ds4} + C_{db4} + C_{ds2} + C_{db2} + C_{gb7} \tag{14.5}$$

$$C_{II} = C_L + C_{ds7} + C_{db7} + C_{ds6} + C_{db6} \tag{14.6}$$

b) The small-signal properties are calculated using nodal analysis in the nodes V_x

and V_{out}.

$$g_{mI}V_{in} + V_x(g_I + sC_I) + (V_x - V_{out})sC_c = 0 \tag{14.7}$$

$$g_{mII}V_x + V_{out}(g_{II} + sC_{II}) + (V_{out} - V_x)sC_c = 0 \tag{14.8}$$

Solving for V_x in Eq. (14.8) and inserting it into Eq. (14.7) gives

$$\frac{V_{out}}{V_{in}} = \frac{g_{mI}(g_{mII} - sC_c)}{g_I g_{II} + s((C_{II} + C_c)g_I + (C_I + C_c)g_{II} + C_c g_{mII}) + s^2(C_I C_{II} + C_c(C_I + C_{II}))}$$

We simplify the expression above by assuming that $g_{mII} \gg g_I, g_{II}$ and $C_c, C_{II} \gg C_I$, yielding

$$\frac{V_{out}}{V_{in}} \approx \frac{g_{mI}(g_{mII} - sC_c)}{g_I g_{II} + sC_c g_{mII} + s^2 C_c C_{II}} \tag{14.9}$$

Eq. (14.9) can be used to get the DC gain, poles and zero.

$$A_0 = \frac{g_{mI}}{g_I}\frac{g_{mII}}{g_{II}} \tag{14.10}$$

$$p_1 \approx \frac{g_I g_{II}}{g_{mII} C_c} \tag{14.11}$$

$$p_2 \approx \frac{g_I g_{II}}{C_c C_{II}}\frac{1}{p_1} = \frac{g_{mII}}{C_{II}} \tag{14.12}$$

$$z_1 = -\frac{g_{mII}}{C_c} \tag{14.13}$$

The zero is located in the right half plane (RHP).

The unity-gain frequency is approximately given by the expression $\omega_u \approx A_0 p_1$ if the poles are well separated.

$$\omega_u \approx \frac{g_{mI}}{g_I}\frac{g_{mII}}{g_{II}}\frac{g_I g_{II}}{g_{mII} C_c} = \frac{g_{mI}}{C_c} \tag{14.14}$$

Q.E.D.

c, d, and e) Recall that $g_m \propto \sqrt{W(I_D/L)}$ and $g_{ds} \propto I_D/L$. The DC gain, unity-gain frequency and the first pole can be expressed as

$$A_0 = \frac{g_{m2}g_{m7}}{(g_{ds2}+g_{ds4})(g_{ds6}+g_{ds7})} \propto \frac{\sqrt{\frac{W_2}{2L_2}I_{D5}}\sqrt{\frac{W_7}{L_7}I_{D6}}}{\left(\frac{1}{L_2}+\frac{1}{L_4}\right)\frac{I_{D5}}{2}\left(\frac{1}{L_6}+\frac{1}{L_7}\right)I_{D6}} = \frac{L_4\sqrt{2W_2L_2}}{(L_2+L_4)\sqrt{I_{D5}}}\frac{L_6\sqrt{W_7L_7}}{(L_6+L_7)\sqrt{I_{D6}}} \tag{14.15}$$

$$\omega_u \approx \frac{g_{mI}}{C_c} \propto \sqrt{\frac{W_2}{2L_2}I_{D5}} \tag{14.16}$$

$$p_1 \approx \frac{(g_{ds2}+g_{ds4})(g_{ds6}+g_{ds7})}{g_{m7}C_c} \propto \frac{\left(\frac{1}{L_2}+\frac{1}{L_4}\right)\frac{I_{D5}}{2}\left(\frac{1}{L_6}+\frac{1}{L_7}\right)\frac{I_{D6}}{2}}{\sqrt{\frac{W_7}{L_7}I_{D6}}C_c} = \frac{1}{4}\left(\frac{1}{L_2}+\frac{1}{L_4}\right)\frac{(L_6+L_7)}{L_6\sqrt{W_7L_7}}I_{D5}\sqrt{I_{D6}} \tag{14.17}$$

$$\frac{1}{4}\left(\frac{1}{L_2}+\frac{1}{L_4}\right)\frac{(L_6+L_7)}{L_6\sqrt{W_7L_7}}I_{D5}\sqrt{I_{D6}} \tag{14.18}$$

	DC gain	**unity-gain frequency**	**bandwidth**
W_2 **increased**	Increased	Increased	-
I_{bias} **increased**	Decreased	Increased	Increased
W_4 **increased**	-	-	-

15. A two-stage OTA without compensation circuit.

The ESSS of the two-stage amplifier is shown in Figure 46. The following assumption has been used, $g_m \gg g_{ds}$ and no bulk effect.

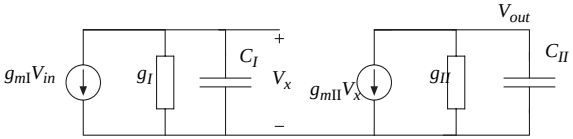


Figure 46: The ESSS of an ordinary two-stage amplifier with no compensation.

Since there is no connection between the first stage and the second stage, i.e. no

component between the node V_x and V_{out}, the transfer function can be computed directly by the following expression

$$A(s) = \frac{V_{out}}{V_{in}} = \frac{V_{out}}{V_x}\frac{V_x}{V_{in}} = \frac{g_{mII}}{g_{II}+sC_{II}}\frac{g_{mI}}{g_I+sC_I} \tag{15.1}$$

where $g_{mII} = g_{m7}$, $g_{mI} = g_{m1} = g_{m2}$, $g_{II} = g_{ds6}+g_{ds7}$, $g_I = g_{ds2}+g_{ds4}$, $C_I = C_{gs7}$, and $C_{II} = C_L$.

The DC gain is

$$A_0 = \frac{g_{m2}g_{m7}}{(g_{ds2}+g_{ds4})(g_{ds6}+g_{ds7})} \propto \frac{L_4\sqrt{2W_2L_2}}{(L_2+L_4)\sqrt{I_{D5}}}\frac{L_6\sqrt{W_7L_7}}{(L_6+L_7)\sqrt{I_{D6}}} \tag{15.2}$$

which gives that

$$A_0 \propto \frac{1}{\sqrt{I_{D5}I_{D6}}} \tag{15.3}$$

b) The dominant pole is located at

$$p_1 = \frac{g_{ds6}+g_{ds7}}{C_L} \tag{15.4}$$

if the load capacitor is assumed to be much larger than the capacitive parasitics. The non dominant pole is located at

$$p_2 = \frac{g_{ds2}+g_{ds4}}{C_{gs7}} \tag{15.5}$$

c) The unity-gain frequency

$$\omega_u \approx A_0 p_1 = \frac{g_{m2}g_{m7}}{(g_{ds2}+g_{ds4})C_L} \tag{15.6}$$

The phase margin is defined as $\phi_m = \pi + \arg A(j\omega_u)$.

$$\phi_m = \pi - \operatorname{atan}\frac{\omega_u}{p_1} - \operatorname{atan}\frac{\omega_u}{p_2} \tag{15.7}$$

d) An ideal operational amplifier has zero output impedance. To decrease the output impedance we have to compute the output resistance of the amplifier. Adding a voltage source at the output and calculating the current delivered by the source according to the following

$$I_{out} = V_{out}(g_{ds6}+g_{ds7}) \tag{15.8}$$

The output resistance is, thus,

$$r_{out} = \frac{V_{out}}{I_{out}} = \frac{1}{g_{ds6}+g_{ds7}} \approx \frac{1}{\left(\frac{1}{L_6}+\frac{1}{L_7}\right)I_{D6}} \tag{15.9}$$

The output resistance is decreased if the current through the output stage is increased. Another way to decrease the output resistance is to add a buffer stage, for example a common-drain amplifier, at the output of the circuit.

16. Compensation of a two-stage OTA.

a) The resistor value can be choose so that the compensation zero is located at infinity, nulling resistor. The other way is to use the lead compensation method where the zero is placed slightly higher in frequency than the unity-gain frequency.

b) Starting with the *Miller capacitor* compensation:

The simplified ESSS is shown in Figure 47. The transfer function is calculated us-

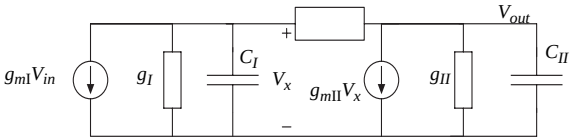


Figure 47: The ESSS of an ordinary two-stage amplifier with compensation.

ing nodal analysis in the nodes V_x and V_{out}.

$$g_{m1}V_{in} + V_x(g_I + sC_I) + (V_x - V_{out})sC_c = 0 \tag{16.1}$$

$$g_{mII}V_x + V_{out}(g_{II} + sC_{II}) + (V_{out} - V_x)sC_c = 0 \tag{16.2}$$

Solving for V_x in Eq. (16.2) and inserting it into Eq. (16.1) gives

$$\frac{V_{out}}{V_{in}} = \frac{g_{mI}(g_{mII} - sC_c)}{g_I g_{II} + s((C_{II} + C_c)g_I + (C_I + C_c)g_{II} + C_c g_{mII}) + s^2(C_I C_{II} + C_c(C_I + C_{II}))}$$

Some simplification can be in place. $g_m \gg g$, $C_c \gg C_I$, $C_c \approx C_{II}$.

$$\frac{V_{out}}{V_{in}} \approx \frac{g_{mI}(g_{mII} - sC_c)}{g_I g_{II} + sC_c g_{mII} + s^2 C_c C_{II}} \tag{16.3}$$

The above equation can be used to get the DC gain, poles and zero.

$$A_0 = \frac{g_{mI}}{g_I}\frac{g_{mII}}{g_{II}} \tag{16.4}$$

$$p_1 \approx \frac{g_I g_{II}}{g_{mII} C_c} \tag{16.5}$$

$$p_2 \approx \frac{g_I g_{II}}{C_c C_{II}}\frac{1}{p_1} = \frac{g_{mII}}{C_{II}} \tag{16.6}$$

$$z_1 = -\frac{g_{mII}}{C_c} \tag{16.7}$$

The zero is located in the right hand plane (RHP).

The unity-gain frequency is approximately give by the expression $\omega_u \approx A_0 p_1$ if the poles are well separated.

$$\omega_u \approx \frac{g_{mI}}{g_I}\frac{g_{mII}}{g_{II}}\frac{g_I g_{II}}{g_{mII} C_c} = \frac{g_{mI}}{C_c} \tag{16.8}$$

The *resistor and capacitor (lead) compensation* is shown in Figure 48. Nodal

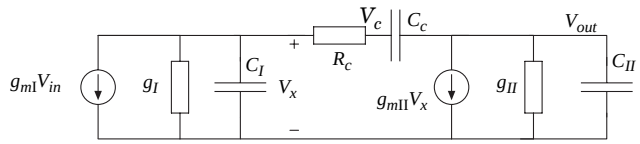


Figure 48: The ESSS of a two-stage amplifier compensated with a resistor and a capacitor.

analysis in the nodes V_x, V_c and V_{out} gives the following equations.

$$g_{mI}V_{in} + V_x(g_I + sC_I) + (V_x - V_c)G_c = 0 \tag{16.9}$$

$$(V_x - V_c)G_c + (V_{out} - V_c)sC_c = 0 \tag{16.10}$$

$$g_{mII}V_x + V_{out}(g_{II} + sC_{II}) + (V_{out} - V_c)sC_c = 0 \tag{16.11}$$

Solving this system of equations gives

$$\frac{V_{out}}{V_{in}} = \frac{g_{mI}(G_c g_{mII} + C_c(-G_c + g_{mII}))s}{a + bs + cs^2 + ds^3} \tag{16.12}$$

where

$$a = g_I g_{II} G_c \tag{16.13}$$

$$b = (C_{II}g_I + C_I g_{II})G_c + C_c(g_I g_{II} + G_c(g_I + g_{II} + g_{mII})) \tag{16.14}$$

$$c = C_I C_{II} G_c + C_c(C_{II}g_I + C_I g_{II} + (C_I + C_{II})G_c) \tag{16.15}$$

$$d = C_I C_{II} C_c \tag{16.16}$$

The above expressions can be simplified by $C_I \ll C_{II}$, $C_I \ll C_c$, $g \ll g_m$, and $g \ll G_c$

$$b \approx C_{II}g_I G_c + C_c G_c g_{mII} \tag{16.17}$$

$$c \approx C_c C_{II} G_c \tag{16.18}$$

The DC gain is

$$A_0 = \frac{g_{mI}g_{mII}G_c}{g_I g_{II} G_c} = \frac{g_{mI}g_{mII}}{g_I g_{II}} \tag{16.19}$$

The first pole is well separated from the other ones.

$$p_1 \approx \frac{a}{b} \approx \frac{g_I g_{II} G_c}{C_{II}g_I G_c + C_c G_c g_{mII}} = \frac{g_I g_{II}}{C_{II}g_I + C_c g_{mII}} \approx \frac{g_I g_{II}}{C_c g_{mII}} \tag{16.20}$$

The zero is located at

$$z_1 = \frac{G_c g_{mII}}{C_c(-G_c + g_{mII})} = -\frac{1}{C_c\left(\frac{1}{g_{mII}} - \frac{1}{G_c}\right)} \tag{16.21}$$

The unity-gain frequency is

$$\omega_u \approx A_0 p_1 \approx \frac{g_{mI}}{C_c} \tag{16.22}$$

When the compensation circuit is inserted the first pole will decrease in frequency at the same time as the DC gain is not changed. This will result in a decreased unity-gain frequency and a more stable amplifier.

c) To increase the phase margin of the system we need to place the compensation zero of the circuit at a frequency higher than the unity-gain frequency. $|z_1| > \omega_u$ gives

$$-\frac{1}{C_c\left(\frac{1}{g_{mII}} - \frac{1}{G_c}\right)} > \frac{g_{mI}}{C_c} \tag{16.23}$$

which can be rearranged according to

$$R_c > \frac{1}{g_{mI}} + \frac{1}{g_{mII}} \tag{16.24}$$

If $R_c > 1/g_{mII}$ then we will have a zero in the left hand plane.

17. A folded-cascode OTA.

For symmetrical fully differential circuits with only a differential input signal, the node at the source of M_5 is small-signal ground. Further, the circuit is a fully differential gain stage and thereby it is sufficient to compute the small-signal transfer function of half the circuit.

The equivalent small-signal model is shown in Figure 49.

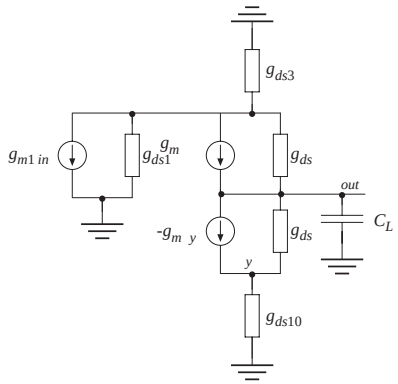


Figure 49: ESSS for the folded-cascode amplifier.

Performing nodal analysis in the nodes V_x, V_y, and V_{out} results in the following equations

$$\begin{aligned} g_{m1}V_{in} + V_x g_{ds1} + V_x g_{ds1} + g_{m7}V_x + (V_x - V_{out})g_{ds7} &= 0 \\ g_{m8}V_y + (V_y - V_{out})g_{ds8} + V_y g_{ds10} &= 0 \\ g_{m7}V_x + (V_x - V_{out})g_{ds7} - V_{out}sC_L + g_{m8}V_y + (V_y - V_{out})g_{ds8} &= 0 \end{aligned} \tag{17.1}$$

Solving for V_{out} in the system of equations gives

$$\frac{V_{out}}{V_{in}} = \frac{-g_{m1}(g_{m7} + g_{ds7})(g_{m8} + g_{ds8} + g_{ds10})}{(g_{ds1} + g_{ds3})g_{ds7}(g_{m8} + g_{ds8} + g_{ds10}) + (g_{ds1} + g_{ds3} + g_{ds7} + g_{m7})(g_{ds8} + g_{ds10}) + sC_L} \tag{17.2}$$

dividing by the two expressions within the parenthesis in the numerator and assuming that $g_m \gg g_{ds}$ gives the following expression

$$\frac{V_{out}}{V_{in}} = \frac{-g_{m1}}{\frac{(g_{ds1} + g_{ds3})g_{ds7}}{g_{m7}} + \frac{g_{ds8}g_{ds10}}{g_{m8}} + sC_L} \tag{17.3}$$

The DC gain is extracted from Eq. (17.3).

$$A_0 = \frac{-g_{m1}}{\frac{(g_{ds1} + g_{ds3})g_{ds7}}{g_{m7}} + \frac{g_{ds8}g_{ds10}}{g_{m8}}} = \frac{-g_{m1}}{g_{out}} \tag{17.4}$$

and the first pole is given by

$$p_1 = \frac{g_{out}}{C_L} \tag{17.5}$$

b) The phase margin is increased if the ratio between the second pole and the unity-gain frequency is increased. The unity-gain frequency can be expressed as

$$\omega_u \approx A_o p_1 \approx \frac{g_{m1}}{C_L} \approx \frac{\sqrt{2\mu_n C_{ox}\frac{W_1}{L_1}I_{diff}}}{C_L} \tag{17.6}$$

where I_{diff} is the current through transistor M_1. The second pole is given in the exercise to be

$$p_2 \approx \frac{g_{m7}}{C_x} \approx \frac{g_{m7}}{C_{gs7}} \approx \frac{\sqrt{2\mu_p C_{ox}\frac{W_7}{L_7}I_{casc}}}{\frac{2}{3}C_{ox}W_7L_7} = \frac{\sqrt{2\mu_p}}{\frac{2}{3}\sqrt{C_{ox}}}\frac{\sqrt{I_{casc}}}{L_7\sqrt{W_7L_7}} \tag{17.7}$$

where I_{casc} is the current through transistors M_7, M_8 and M_{10}. The expression for the ratio between the second pole and the unity-gain frequency is given by

$$\frac{p_2}{\omega_u} \approx \frac{\frac{\sqrt{2\mu_p}}{\frac{2}{3}\sqrt{C_{ox}}}\frac{\sqrt{I_{casc}}}{L_7\sqrt{W_7L_7}}}{\frac{\sqrt{2\mu_n C_{ox}\frac{W_1}{L_1}I_{diff}}}{C_L}} = \frac{3}{2}\sqrt{\frac{\mu_p}{\mu_n}}\frac{\sqrt{L_1}C_L}{C_{ox}L_7\sqrt{W_7L_7W_1}}\sqrt{\frac{I_{casc}}{I_{diff}}} \tag{17.8}$$

Further, the DC gain can be expressed as

$$\begin{aligned} A_0 &\approx \frac{-g_{m1}}{\frac{(g_{ds1}+g_{ds3})g_{ds7}}{g_{m7}} + \frac{g_{ds8}g_{ds10}}{g_{m8}}} \approx \\ &\frac{\sqrt{2\mu_n C_{ox}\frac{W_1}{L_1}I_{diff}}}{\frac{(\lambda_1 I_{diff}+\lambda_3(I_{diff}+I_{casc}))\lambda_7 I_{casc}}{\sqrt{2\mu_p C_{ox}\frac{W_7}{L_7}I_{casc}}} + \frac{\lambda_8\lambda_{10}I_{casc}^2}{\sqrt{2\mu_n C_{ox}\frac{W_8}{L_8}I_{casc}}}} \approx \\ &\sqrt{2\mu_n C_{ox}}\frac{\sqrt{\frac{W_1}{L_1}I_{diff}}}{\frac{\left(\frac{1}{L_1}I_{diff}+\frac{1}{L_3}(I_{diff}+I_{casc})\right)\sqrt{I_{casc}}}{\sqrt{W_7L_7}} + \frac{I_{casc}^{3/2}}{\sqrt{2\mu_n C_{ox}}\sqrt{W_8L_8}L_{10}}} \end{aligned} \tag{17.9}$$

From Eq. (17.8) and Eq. (17.9) the solution can be computed.

The phase margin can be increased if the area is limited by for example:

- Increasing I_{casc} the drawbacks will be higher power consumption and lower DC gain.

The phase margin can be increased if the power is critical by for example:

- Increasing C_L, the drawbacks is decreased slew rate and unity-gain frequency, but the DC gain will not be changed.
- Decrease W_7, the drawback is decreased DC gain, no changes to the unity-gain frequency or the slew rate.

The phase margin can be increased if the unity-gain frequency and the power consumption is critical for example by:

- Decrease W_7, the drawback is decreased DC gain, no changes to the unity-gain frequency or the slew rate.

3.5 — Noise in CMOS circuits

18. Noise in a multi-stage amplifier.

a) In Figure 50(b) the small-signal equivalent for the circuit is shown. Further,

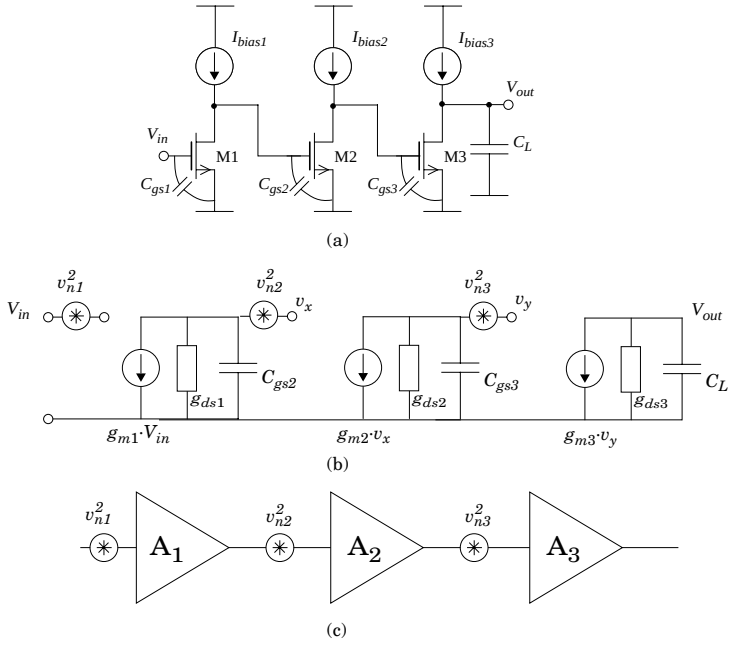


Figure 50: (a) Multi-stage circuit, (b) small-signal equivalent and (c) superposition principle.

the gain for each gain stage is computed to

$$A_1 = \frac{-g_{m1}}{g_{ds1} + sC_{gs2}};\ A_2 = \frac{-g_{m2}}{g_{ds2} + sC_{gs3}} \text{ and } A_3 = \frac{-g_{m3}}{g_{ds3} + sC_L} \tag{18.1}$$

The total output noise is now given by superpositioning the different noise contributions according to

$$V_{N,TOT}^2 = v_{n1}^2\left|A_1A_2A_3\right|^2 + v_{n2}^2\left|A_2A_3\right|^2 + v_{n3}^2\left|A_3\right|^2 \tag{18.2}$$

where

$$v_{ni}^2 = \frac{8kT}{3}\frac{1}{g_{mi}} \tag{18.3}$$

By combining Eq. (18.1), Eq. (18.2) and Eq. (18.3) we get

$$V_{N,TOT}^2 = \frac{8kT}{3}\frac{1}{g_{m1}}\frac{g_{m1}^2g_{m2}^2g_{m3}^2}{|g_{ds1} + j2\pi fC_{gs2}|^2|g_{ds2} + j2\pi fC_{gs3}|^2|g_{ds3} + j2\pi fC_L|^2} +$$
$$+\frac{8kT}{3}\frac{1}{g_{m2}}\frac{g_{m2}^2g_{m3}^2}{|g_{ds2} + j2\pi fC_{gs3}|^2|g_{ds3} + j2\pi fC_L|^2} + \frac{8kT}{3}\frac{1}{g_{m3}}\frac{g_{m3}^2}{|g_{ds3} + j2\pi fC_L|^2} \tag{18.4}$$

and with all I_{bias} equal and all transistors equally sized -> equal g_m, g_{ds}, and C_{gs} we get

$$V_{N,TOT}^2 = \frac{8kT}{3}\frac{g_m}{|g_{ds} + j2\pi fC_L|^2}\left(\frac{g_m^4}{|g_{ds} + j2\pi fC_{gs}|^4} + \frac{g_m^2}{|g_{ds} + j2\pi fC_{gs}|^2} + 1\right) \tag{18.5}$$

The equivalent output noise power is computed as the integral of the spectral density over the frequency spectrum. This is here approximated using the noise bandwidth concept. Hence, the output noise power is

$$P_{out} = V_{N,TOT}^2\frac{p_1}{4} = \frac{2kT}{3}\frac{g_m}{g_{ds}^2}\left(\frac{g_m^4}{g_{ds}^4} + \frac{g_m^2}{g_{ds}^2} + 1\right)\frac{g_{ds}}{C_L} =$$
$$\frac{2kT}{3C_L}\frac{g_m}{g_{ds}}\left(\frac{g_m^4}{g_{ds}^4} + \frac{g_m^2}{g_{ds}^2} + 1\right) \tag{18.6}$$

b) The total output noise scales with I_D as

$$V_{N,TOT}^2 \sim \frac{g_m}{g_{ds}}\left(\frac{g_m^4}{g_{ds}^4} + \frac{g_m^2}{g_{ds}^2} + 1\right) \sim \frac{1}{\sqrt{I_D}}\left(\frac{1}{I_D^2} + \frac{1}{I_D} + 1\right);(g_m \approx 2\sqrt{\alpha I_D},$$
$$g_{ds} \approx \lambda I_D), \tag{18.7}$$

i.e., increasing I_D decreases the equivalent output noise power.

The DC gain of the circuit is given by

$$A_{TOT} = A_1A_2A_3 = \frac{g_{m1}g_{m2}g_{m3}}{g_{ds1}g_{ds2}g_{ds3}} \sim \left(\frac{1}{I_D}\right)^{3/2}, \tag{18.8}$$

i.e., the DC gain will be lower for a larger I_D.

The bandwidth of the circuit is approximately given by the dominating pole because $C_L \gg C_{gs}$. This pole is computed from

$$A_3 = \frac{g_{m3}}{(g_{ds3} + sC_L)} = \frac{g_{m3}/g_{ds3}}{\left(1 + \frac{sC_L}{g_{ds3}}\right)}, \tag{18.9}$$

i.e., the pole is given by

$$p_1 = \frac{g_{ds}}{C_L}. \tag{18.10}$$

Hence, the bandwidth scales as $p_1 \sim \lambda I_D$ -> larger bandwidth for a larger I_D.

c) From Eq. (18.2) we can see that A_3 amplifies all noise sources, i.e., this stage should have the smallest gain. A_1 on the other hand only amplifies the first noise source and should therefore have the largest gain.

19. Noise in CMOS circuits.

a) The equivalent small-signal model for the circuit is shown in Figure 51.

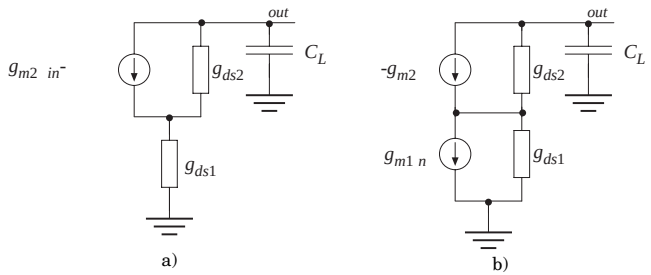


Figure 51: ESSS for the source-degenerated CS stage. a) Input to output. b) bias to output.

To compute the equivalent output noise power the transfer function from V_{in} to V_{out} and from V_b to V_{out} is computed. We start by setting up the equations required to compute the transfer function from the input to the output.

$$g_{m1}(V_{in} - V_x) - g_{mbs1}V_x + (V_{out} - V_x)g_{ds1} - V_xg_{ds2} = 0 \tag{19.1}$$

$$g_{m1}(V_{in} - V_x) - g_{mbs1}V_x + (V_{out} - V_x)g_{ds1} + V_{out}sC_L = 0 \tag{19.2}$$

Solving for V_{out} by eliminating V_x gives the following transfer function

$$H_1 = \frac{V_{out}}{V_{in}} = \frac{g_{m1}}{g_{ds1}}\frac{1}{1 + \frac{s}{\frac{g_{ds1}g_{ds2}}{C_L(g_{m1} + g_{mbs1} + g_{ds1} + g_{ds2})}}} \tag{19.3}$$

The equations for the transfer function between V_b and V_{out} is given by

$$g_{m2}V_n + g_{ds2}V_x + g_{m1}V_x + g_{mbs1}V_x + (V_x - V_{out})g_{ds1} = 0 \quad (19.4)$$

$$g_{m1}V_x + g_{mbs1}V_x + (V_x - V_{out})g_{ds1} - V_{out}sC_L = 0 \quad (19.5)$$

Solving for V_{out} by eliminating V_x results in

$$H_2 = \frac{V_{out}}{V_b} = \frac{(g_{m1}+g_{mbs1}+g_{ds1})g_{m2}}{g_{ds1}g_{ds2}} \frac{1}{1+\frac{s}{\frac{g_{ds1}g_{ds2}}{C_L(g_{m1}+g_{mbs1}+g_{ds1}+g_{ds2})}}}$$

$$\approx \frac{(g_{m1}+g_{mbs1})g_{m2}}{g_{ds1}g_{ds2}} \frac{1}{1+\frac{s}{\frac{g_{ds1}g_{ds2}}{C_L(g_{m1}+g_{mbs1}+g_{ds1}+g_{ds2})}}} \quad (19.6)$$

The rms output noise is given by

$$V_{no}^2 = \int |H_1|^2 V_{in}^2 df + \int |H_2|^2 V_b^2 df \quad (19.7)$$

where

$$V_{in}^2 = \frac{8kT}{3}\frac{1}{g_{m1}} \quad (19.8)$$

and

$$V_b^2 = \frac{8kT}{3}\frac{1}{g_{m2}} \quad (19.9)$$

The last two equations comes from the fact that the thermal noise power of a transistor is modelled as a gaussian white noise source.

The two integrals in Eq. (19.7) can be calculated using the concept of noise bandwidth which results in the following computation.

$$V_{no}^2 = \left(\frac{g_{m1}}{g_{ds1}}\right)^2 \frac{p_1}{4} V_{in}^2 + \left(\frac{(g_{m1}+g_{mbs1})g_{m2}}{g_{ds1}g_{ds2}}\right)^2 \frac{p_1}{4} V_b^2 \quad (19.10)$$

$$V_{no}^2 = \frac{2kT}{3C_L}\left(\frac{g_{m1}}{g_{ds1}}g_{ds2} + \frac{(g_{m1}+g_{mbs1})^2 g_{m2}}{g_{ds1}g_{ds2}}\right)\frac{1}{g_{m1}+g_{mbs1}+g_{ds1}+g_{ds2}} \approx$$

$$\approx \frac{2kT}{3C_L}\left(\frac{g_{m1}}{g_{ds1}(g_{m1}+g_{mbs1})}g_{ds2} + \frac{(g_{m1}+g_{mbs1})g_{m2}}{g_{ds1}g_{ds2}}\right)$$

$$\approx \frac{2kT}{3C_L}\left(\frac{g_{ds2}}{g_{ds1}} + \frac{g_{m1}g_{m2}}{g_{ds1}g_{ds2}}\right) \quad (19.11)$$

b) Relevant design parameters are for example the current through the circuit and the size of the transistor.

Rewriting the Eq. (19.11) with the design parameters yields

$$V_{no}^2 = \frac{2kT}{3}\frac{1}{C_L}\left(\frac{L_2}{L_1} + \frac{\sqrt{2\mu_n C_{ox} W_1 L_1}\sqrt{2\mu_n C_{ox} W_2 L_2}}{I_{bias}}\right) \quad (19.12)$$

The DC gain from the input to the output is given by

$$A_0 = \frac{g_{m1}}{g_{ds1}} \approx \sqrt{\frac{2\mu_n C_{ox} W_1 L_1}{I_{bias}}} \quad (19.13)$$

and the unity-gain frequency is given by

$$\omega_u \approx A_0 p_1 \approx \frac{g_{ds2}g_{m1}}{(g_{m1}+g_{mbs1}+g_{ds1}+g_{ds2})C_L} \approx \frac{g_{ds2}}{C_L} \approx \frac{I_{bias}}{L_2 C_L} \quad (19.14)$$

The equivalent output noise power can be reduced by:

- Increase the bias current -> Decreased DC gain, Increased unity-gain frequency, and Increased slew rate.
- Decreased W_2 -> No change to the DC gain, unity-gain frequency or slew rate.
- Decrease L_2 -> No change to the DC gain, increased unity-gain frequency and no change to the slew rate.

20. Noise in an amplifier.

a) The ESSS is shown in Figure 52.

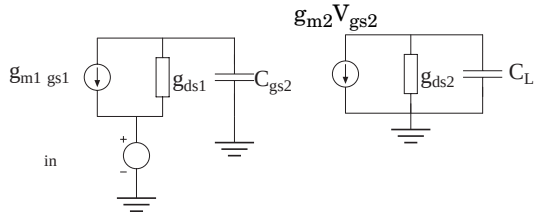


Figure 52: The ESSS of the noisy circuit

We have to calculate the transfer function from the gate of transistor M1 to the output, $H1$, from transistor M2 to the output, $H2$, and from the V_{in} to the output, H.

$$H1 = \frac{g_{m1}g_{m2}}{g_{ds1}g_{ds2} + s(g_{ds1}C_L + g_{ds2}C_{gs2}) + s^2 C_L C_{gs2}} \quad (20.1)$$

According to exercise 2 the poles of the transfer function can be extracted directly.

$$p_{11} \approx \frac{g_{ds2}}{C_L} \quad (20.2)$$

and

$$p_{12} \approx \frac{g_{ds1}}{C_{gs2}} \quad (20.3)$$

Continuing with the transfer function from the gate of M2 to the output.

$$H2 = -\frac{g_{m2}}{g_{ds2} + sC_L} \tag{20.4}$$

The transfer function from V_{in} to the output is

$$H = \frac{(g_{m1} + g_{ds1})g_{m2}}{g_{ds1}g_{ds2} + s(g_{ds1}C_L + g_{ds2}C_{gs2}) + s^2C_LC_{gs2}} \tag{20.5}$$

The spectral density of the output can be calculated as

$$S_{out}(f) = |H_1(f)|^2V_{n1} + |H_2(f)|^2V_{n2} \tag{20.6}$$

where

$$V_{ni} = \frac{8kT}{3}\frac{1}{g_{mi}} \tag{20.7}$$

The noise power at the output can now be calculated according to the equation below.

$$V_{out}^2 = \int_0^\infty S_{out}(f)df \tag{20.8}$$

If we do not like to perform the integration we can use the concept of noise bandwidth (see chapter 4 in Johns&Martin). The integral of a one pole system (or a system with well separated poles) is equivalent to the integral of a rectangle with the width of the dominant pole divided by four.

$$V_{out}^2 = \frac{2kT}{3}\frac{g_{m2}}{g_{ds2}}\frac{1}{C_L}\left(\frac{g_{m1}g_{m2}}{g_{ds1}^2} + 1\right) \tag{20.9}$$

b) Derive the noise voltage that can be referred to the input.

The input referred noise voltage can be obtain by dividing the output referred noise voltage by $|H_1|^2$.

$$S_{in}(f) = S_{out}(f)/|H_1|^2 \tag{20.10}$$

This gives the answer

$$S_{in}(f) = \frac{8kT}{3}\frac{g_{ds2}}{g_{m1}}\left(1 + \frac{g_{ds1}}{g_{m1}g_{m2}}^2\right) \tag{20.11}$$

c) Propose one way to increase the maximum signal-to-noise ratio, SNR in the circuit. What will happen to the DC gain, unity-gain frequency, bandwidth and the phase margin of the circuit?

The gain, p1, p2, ω_u of the circuit are already derived. Assume that the input voltage source is white.

$$V_{in}^2 = S_{in}(f) = \frac{2kT}{3}\frac{1}{g_{m1}}\left(1 + \frac{g_{ds1}^2}{g_{m1}g_{m2}}\right)\frac{g_{ds2}}{C_L} \tag{20.12}$$

$$\propto \frac{2kT}{3}\frac{g_{ds2}}{g_{m1}}\frac{1}{C_L}\left(1 + \frac{g_{ds1}^2}{g_{m1}g_{m2}}\right) \tag{20.13}$$

$$\propto \frac{I_2}{L_2}\sqrt{\frac{L_1}{W_1I_1}}\left(1 + \frac{I_1^2}{L_1^2}\sqrt{\frac{L_1L_2I_1I_2}{W_1W_2}}\right) \tag{20.14}$$

$$A_0 = \frac{g_{m1}g_{m2}}{g_{ds1}g_{ds2}} \propto \sqrt{\frac{W_1L_1W_2L_2}{I_{bias1}I_{bias2}}} \tag{20.15}$$

$$p1 = \frac{g_{ds2}}{C_L} \propto \frac{I_2}{L_2C_L} \tag{20.16}$$

$$p_2 \approx \frac{g_{ds1}}{C_{gs2}} \propto \frac{I_1}{W_2L_1L_2} \tag{20.17}$$

$$\omega_u \approx A_0p_1 = \frac{g_{m1}g_{m2}}{g_{ds1}C_L} \propto \sqrt{\frac{W_1L_1W_2I_{bias2}}{L_2I_{bias1}C_L}} \tag{20.18}$$

The above five equations shows that will happen if a parameter is changed. Remember that

$$1 \gg \frac{g_{ds1}}{g_{m1}g_{m2}}^2 \tag{20.19}$$

Change	noise	A0	p1	unity-gain	phase margin
Increase W1	decreases	Increases	no change	increases	decreases
increase I1	decreases	decreases	no change	decreases	increases
Increase W2	decreases	increases	no change	increases	decreases
decrease I2	decreases	increases	decreases	decreases	increases

21. Noise in a common-source amplifier biased by a current mirror.

a) The spectral density function of for the resistor is given by

$$V_R^2(f) = 4kTR \tag{21.1}$$

The ESSS is shown in Figure 53.

We have to calculate the transfer function from the drain of transistor M1 to the output, H1, from transistor M2 to the output, H2, from transistor M3 to the output, H3, and from the resistor to the output, H4.

Consider a current source at in parallel with transistor M1 this will give a transfer function from that current source to the output according to

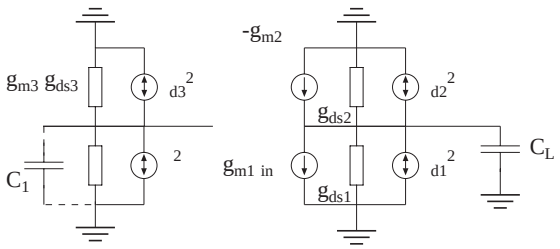


Figure 53: The ESSS of the noisy circuit.

$$H1 = -\frac{1}{g_{ds1} + g_{ds2} + sC_L} \tag{21.2}$$

the pole is located in

$$p_1 = \frac{g_{ds1} + g_{ds2}}{C_L} \tag{21.3}$$

Continuing with the transfer function from the noise current source in transistor M2 to the output. This gives that $H2 = H1$.

The transfer function from M3 to the output is given by

$$H_3 = \frac{V_{out}}{V_x}\frac{V_x}{I_{nM3}} = -\frac{g_{m2}}{g_{ds1} + g_{ds2} + sC_L}\frac{1}{g_{ds3} + g_{m3} + \frac{1}{R}} \tag{21.4}$$

The transfer function from the resistor to the output is given by

$$H_4 = \frac{V_{out}}{V_x}\frac{V_x}{I_R} = -\frac{g_{m2}}{g_{ds1} + g_{ds2} + sC_L}\frac{1}{g_{ds3} + g_{m3} + \frac{1}{R}} \tag{21.5}$$

The spectral density function of the output can be calculated as

$$S_{out}(f) = |H_1(f)|^2 I^2_{n1} + |H_2(f)|^2 I^2_{n2} + |H_3(f)|^2 I^2_{n3} + |H_4(f)|^2 I^2_1 \tag{21.6}$$

where

$$I_{ni} = \frac{8kT}{3} g_{mi} \tag{21.7}$$

The noise power at the output can now be calculated according to

$$V^2_{out} = \int_0^\infty S_{out}(f)df \tag{21.8}$$

If we do not like to perform the integration we can use the concept of noise bandwidth (see chapter 4 in Johns&Martin). The integral of a one pole system (or a system with well separated poles) is equivalent to the integral of a rectangle with the width of the dominant pole divided by four.

$$V^2_{out} = \frac{2kT}{g_{ds2} + g_{ds1}}\frac{1}{C_L}\left(\frac{g_{m1}}{3} + \frac{g_{m2}}{3} + \frac{g^2_{m2}}{\left(\frac{1}{R} + g_{m3} + g_{ds3}\right)^2}\left(\frac{g_{m3}}{3} + \frac{1}{2R}\right)\right) \tag{21.9}$$

b)

- Increase the load capacitor. This will decrease the unity-gain frequency of the amplifier, but the gain will not change.
- Decrease the resistance R. This will increase the current through transistor M3 and thereby through all transistors. The output noise voltage is approximately proportional to the inverse of the square root of the current through transistor M1. $g_{m3} \gg 1/R$ is assumed. Increasing the current will decrease the DC gain of the circuit but increase the unity-gain frequency.
- Decrease the size of M1. Decreases the DC gain and the unity-gain frequency.
- Decrease the size of both M2 and M3 => approximately constant current. No change will happen to neither the DC gain nor the unity-gain frequency.

c) The ESSS is the same as in Figure 53. The transfer function H1 and H2 will not be affected, but H3 and H4 will be changed.

$$H_3 = \frac{g_{m2}}{g_{ds1} + g_{ds2} + sC_L}\frac{1}{\frac{1}{R} + g_{m3} + g_{ds3} + sC_1} \tag{21.10}$$

$$H_4 = \frac{g_{m2}}{g_{ds1} + g_{ds2} + sC_L}\frac{1}{\frac{1}{R} + g_{m3} + g_{ds3} + sC_1} \tag{21.11}$$

The dominating pole of both H3 and H4 are approximately

$$p = \frac{\frac{1}{R} + g_{m3} + g_{ds3}}{C_1} \tag{21.12}$$

Using the same way to calculate the output noise as in 3a) gives

$$V^2_{out} = \frac{2kT}{g_{ds2} + g_{ds1}}\left(\frac{1}{3C_L}(g_{m1} + g_{m2}) + \frac{g^2_{m2}}{g_{ds2} + g_{ds1}}\frac{1}{\frac{1}{R} + g_{m3} + g_{ds3}}\left(\frac{g_{m3}}{3C_1} + \frac{1}{2R}\right)\right)$$

3.6 — Continuous-time filters

22. Butterworth LP-filter.

From the specification we get that $A_{max} = 3\,\text{dB}$ at $\omega_c = 2\pi \cdot 3.5 \cdot 10^3 \approx 22\,\text{krad/s}$ and that $A_{min} = 25\,\text{dB}$ at $\omega_s = 2\pi \cdot 10 \cdot 10^3 \approx 63$ krad/s.

Nomogram and formulas gives us a filter order of $N = 3$ (page 27 and 25).

According to the “Tabell och Formelsamlingen” at page 23 the in-resistance for the voltage supply is normalized to $1/R_i$. This gives us the refection factor $r = R_L/R_i = 600/1200 = 0.5$.

From the table at page 28 ($r = 0.5$) we get the normalized values:

$L_{1n} = 3.2612$, $C_{2n} = 0.7789$, $L_{3n} = 1.1811$

Which are de normalized according to $L = \frac{R_0 L_n}{\omega_0}$ and $C = \frac{C_n}{\omega_0 R_0}$ which finally gets us:

$L_1 = 88.9mH$, $C_2 = 59nF$, $L_3 = 49mH$

23. Chebychev LP filter.

The specification is given as:

$\omega_c = 1000$ rad/s, $\omega_s = 2000$ rad/s, $Z_L = 1k\Omega$, $Z_i = 125\Omega$.

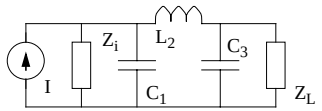
A filter of Chebyshev I type shall be implemented, with lowest possible order that meets the specification above. The transfer curve is normalized giving us the maximal value $H_0 = 1$. By using that and the information given by the specification we get:

$$A_{max} = 20\log 1.2 \approx 1.58\,\text{dB and } A_{min} = 20\log(1/0.1) = 20\,\text{dB} \qquad (23.1)$$

By using a nomogram we can derive the filter order but it can also be calculated as

$$N = \left\lceil \operatorname{acosh}\sqrt{\frac{10^{0.1A_{min}}-1}{10^{0.1A_{max}}-1}} / \operatorname{acosh}\left(\frac{\omega_s}{\omega_c}\right) \right\rceil \approx \lceil 2.58 \rceil = 3 \qquad (23.2)$$

We also know that we shall implement a current-mode filter and that $r = |Z_i/Z_L| = 1/8$. The ripple can be derived to be approximately 1.6 dB. This means that we shall use the closest lower value given by the table (= 1dB, page 36). We read the component values – and since we have a current mode filter and we have an odd filter order ($N = 3$) the first component must be a capacitance (page 23).



$C_{1n} = 12.5563$

$L_{2n} = 0.1657$

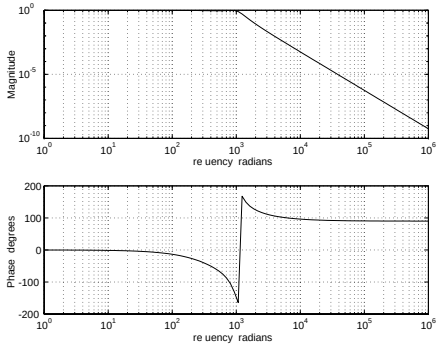
$C_{3n} = 8.8038$

The values are de normalized, which gives us:

$$C_1 = \frac{C_{1n}}{\omega_0 Z_L} = \frac{12.5563}{1000 \cdot 1000} = 12.5563\mu F \qquad (23.3)$$

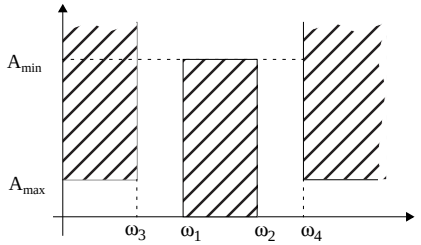
$$L_2 = \frac{Z_L L_{2n}}{\omega_0} = \frac{1000 \cdot 0.1657}{1000} = 0.1657H \qquad (23.4)$$

$$C_3 = \frac{C_{3n}}{\omega_0 Z_L} = 8.8038\mu F \qquad (23.5)$$



24. Butterworth BS-filter.

From the text we get the following specification.



$$\begin{cases} \omega_1 = 1600\ [\text{rad/s}] \\ \omega_2 = 2000\ [\text{rad/s}] \\ \omega_3 = 800\ [\text{rad/s}] \\ \omega_4 = 4000\ [\text{rad/s}] \\ A_{min} = 50\ [\text{dB}] \\ A_{max} = 3\ [\text{dB}] \end{cases}$$

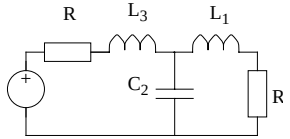
First we transform the BS-specification to an LP-specification. According to page 67 in "Tabell och Formelsamlingen" we get:

$$\begin{cases} \omega_I^2 = \omega_1\omega_2 = \omega_3\omega_4 = 1600 \cdot 2000 = 32 \cdot 10^6 \\ \Omega_2 = \dfrac{\omega_I^2}{\omega_4 - \omega_3} = \dfrac{32 \cdot 10^5}{3200} = 1 \cdot 10^3\ [\text{rad/s}] \\ \Omega_3 = \dfrac{\omega_I^2}{\omega_2 - \omega_1} = \dfrac{32 \cdot 10^5}{400} = 8 \cdot 10^3\ [\text{rad/s}] \end{cases}$$

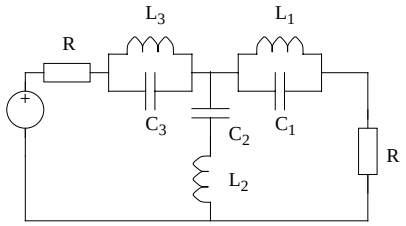
Nomogram, (the requirement on the attenuation is the same as for the BS specification) and the transformed frequencies gives the filter order N=3. We now get the normalized element values from table (r=1) and we de normalized them ac-

cording to page 22 in "Tabell och Formelsamlingen" ($R_0 = 100$, $\omega_0 = \Omega_2$):

$$\begin{cases} R = 1 \\ L_1 = 1 \\ L_3 = 1 \\ C_2 = 2 \end{cases} \quad \text{denormalization} \quad \begin{cases} R = 100\Omega \\ L_1 = 0.1\text{H} \\ L_3 = 0.1\text{H} \\ C_2 = 20\mu\text{F} \end{cases}$$



Now we can transform our LP-filter back to the specified BP-filter according to page 67 in "T&F", which gives us the final BS-filer:



$$\begin{cases} R = 100\Omega \\ L_1 = L_3 = 100\text{mH} \\ C_1 = C_3 = 3.13\mu\text{F} \\ C_2 = 20\mu\text{F} \\ L_2 = 15.6\text{mH} \end{cases}$$

25. A doubly resistive terminated ladder network.

The solution is much the same as for Exercise 1.3, but since it is not specified which filter type to use it could be interesting to se how the filter order differs between the different filter types. First we transform the BS-specification to an LP-specification according to:

$$\begin{cases} \omega_I^2 = 4\pi^2 \cdot 0.9 \cdot 9 \cdot 10^6 \\ \Omega_2 = 2\pi \cdot 10^3 \text{ [rad/s]} \\ \Omega_3 = 2\pi \cdot 3 \cdot 10^3 \text{ [rad/s]} \end{cases}$$

Now we can use either a nomogram or some computer based program, e.g, Matlab to derive the different filter orders.

The following Matlab code can be used to derive the filter orders for a Butterworth-, Chebyshev I-, and a Cauer-type filter.

```
% Filter specification
Wc = 2*pi*1e3;
Ws = 6*pi*1e3;
Amax = 1;
Amin = 40;
% Filter order for a Butterworth-type filter
NBW = buttord(Wc, Ws, Amax, Amin,'s')
> NBW = 5
% Filter order for a Chebyshev I-type filter
NCI = cheb1ord(Wc, Ws, Amax, Amin,'s')
> NCI = 4
% Filter order for a Cauer-type filter
NCA = ellipord(Wc, Ws, Amax, Amin,'s')
> NCA = 3
```

Here we can see that for the given specification the Cauer-type filter gives the lowest filter order (N=3) followed by the Chebyshev I-type filter (N=4) and finally the Butterworth-type filter (N=5).

3.7 — Switched Capacitor Circuits

26. Switched capacitor circuit.

a) Here we use the charge analysis. The SC circuit is shown for both clock phases in Figure 54.

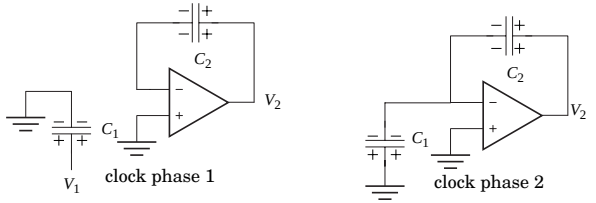


Figure 54: The SC circuit in both clock phases.

Using the charge analysis in the circuit starting at time t *(clock phase 1)*

$$q_1(t) = (V_1(t) - 0)C_1 \tag{26.1}$$

$$q_2(t) = (V_2(t) - 0)C_2 \tag{26.2}$$

At time $t + \tau$ *(clock phase 2)*

$$q_1(t + \tau) = (0 - 0)C_1 \tag{26.3}$$

$$q_2(t + \tau) = (V_2(t + \tau) - 0)C_2 \tag{26.4}$$

At time $t + 2\tau$ *(clock phase 1)*

$$q_1(t + 2\tau) = (V_1(t + 2\tau) - 0)C_1 \tag{26.5}$$

$$q_2(t + 2\tau) = (V_2(t + 2\tau) - 0)C_2 \tag{26.6}$$

Another equation is required to be able to compute the transfer function. This equation comes from the charge conservation. In clock phase 2 the charge of the two capacitors can not disappear since the charge can not be discharged through the opamp input terminals. This means that the charge on the capacitors at the end of clock phase 1 is equal to the charge of the capacitors during the whole clock phase 2.

$$q_1(t) + q_2(t) = q_1(t + \tau) + q_2(t + \tau) \tag{26.7}$$

The charge of C_2 at the time $t + \tau$ is equal to the charge of C_2 at time $t + 2\tau$ since no charge can be given by the opamp input.

$$q_2(t + \tau) = q_2(t + 2\tau) \tag{26.8}$$

Inserting the above equations into Eq. (26.7) gives

$$V_1(t)C_1 + V_2(t)C_2 = V_2(t+\tau)C_2 = V_2(t+2\tau)C_2 \tag{26.9}$$

To compute the transfer function we have to take the Z-transform of both sides.

$$V_1(z)C_1 + V_2(z)C_2 = V_2(z)zC_2 \tag{26.10}$$

Solving for $V_2(z)/V_1(z)$ gives

$$\frac{V_2(z)}{V_1(z)} = \frac{C_1}{C_2}\frac{1}{z-1} = \frac{C_1}{C_2}\frac{z^{-1}}{1-z^{-1}} \tag{26.11}$$

This is a non inverting discrete-time accumulator (compare continuous-time integrator) with a delay of one clock period $T = 2\tau$.

b) Each switch and capacitor has parasitic capacitances connected to ground. In Figure 55 the parasitics are shown.

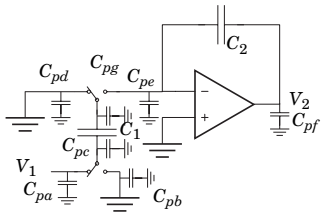


Figure 55: A non inverting accumulator with parasitics.

C_{pa} is connected between the ideal input and ground and will not change the transfer function.

C_{pb} is connected between ground and ground and thereby not change the transfer function.

C_{pc} is connected between the ideal input and ground or shorted to ground. No effect on the transfer function.

C_{pd} Connected to ground. No effect on the transfer function.

C_{pe} is connected between ground and virtual ground thereby not changing the transfer function.

C_{pf} is connected to the ideal operational amplifier and ground not changing the transfer function.

C_{pg} is connected to either ground or virtual ground and thereby not changing the transfer function.

The transfer function is not sensitive to parasitics.

27. Switched capacitor circuit.

a) Here we use the charge analysis. The SC circuit is shown for both clock phases in Figure 56.

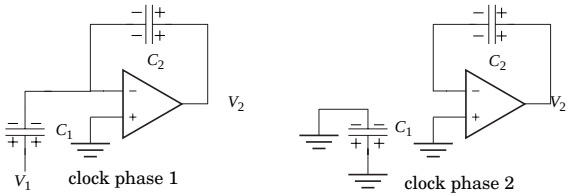


Figure 56: The SC circuit in both clock phases.o

Using the charge analysis in the circuit starting at time t *(clock phase 1)*

$$q_1(t) = (V_1(t)-0)C_1 \tag{27.1}$$

$$q_2(t) = (V_2(t)-0)C_2 \tag{27.2}$$

At time $t+\tau$ *(clock phase 2)*

$$q_1(t+\tau) = (0-0)C_1 \tag{27.3}$$

$$q_2(t+\tau) = (V_2(t+\tau)-0)C_2 \tag{27.4}$$

At time $t+2\tau$ *(clock phase 1)*

$$q_1(t+2\tau) = (V_1(t+2\tau)-0)C_1 \tag{27.5}$$

$$q_2(t+2\tau) = (V_2(t+2\tau)-0)C_2 \tag{27.6}$$

Another equation is required to be able to compute the transfer function. This equation comes from the charge conservation. In clock phase 1, $t+2\tau$, the charge of the two capacitors can not disappear since the charge can not be discharged through the opamp input terminals. This means that the charge on the capacitors at the end of clock phase 2, $t+\tau$, is equal to the charge of the capacitors during the whole clock phase 1, $t+2\tau$.

$$q_1(t+\tau) + q_2(t+\tau) = q_1(t+2\tau) + q_2(t+2\tau) \tag{27.7}$$

The charge of C_2 at the time t is equal to the charge of C_2 at time $t+\tau$ since no charge can be given by the opamp input.

$$q_2(t) = q_2(t+\tau) \tag{27.8}$$

Inserting the above equations into Eq. (27.7) gives

$$V_2(t+\tau)C_2 = V_2(t+2\tau)C_2 + V_1(t+2\tau)C_1 \tag{27.9}$$

and

$$V_2(t) = V_2(t+\tau) \tag{27.10}$$

To compute the transfer function we have to take the Z-transform of both sides.

$$V_2(z)C_2 = V_2(z)zC_2 + V_1(z)zC_1 \tag{27.11}$$

Solving for $V_2(z)/V_1(z)$ gives

$$\frac{V_2(z)}{V_1(z)} = -\frac{C_1}{C_2}\frac{z}{z-1} = -\frac{C_1}{C_2}\frac{1}{1-z^{-1}} \tag{27.12}$$

This is an inverting discrete-time accumulator (compare continuous-time integrator) with no delay.

b) Each switch and capacitor has parasitic capacitances connected to ground. In Figure 57 the parasitics are shown.

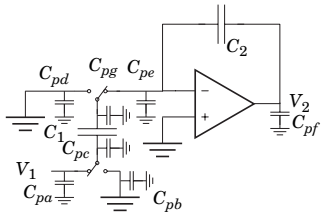


Figure 57: An inverting accumulator with parasitics.

C_{pa} is connected between the ideal input and ground and will not change the transfer function.

C_{pb} is connected between ground and ground and thereby not change the transfer function.

C_{pc} is connected between the ideal input and ground or shorted to ground. No effect on the transfer function.

C_{pd} Connected to ground. No effect on the transfer function.

C_{pe} is connected between ground and virtual ground thereby not changing the transfer function.

C_{pf} is connected to the ideal operational amplifier and ground not changing the transfer function.

C_{pg} is either connected to the virtual ground, ground or ground and ground. Hence, the transfer function of the circuit is not changed.

The transfer function is not sensitive to parasitics.

28. Switched capacitor circuit.

a) Here we use the charge analysis. The SC circuit is shown for both clock phases in Figure 58.

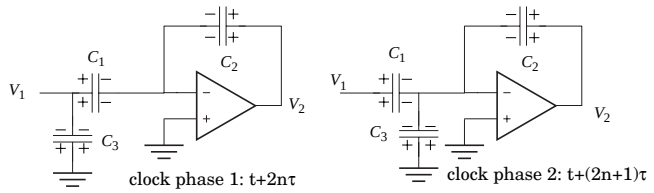


Figure 58: The SC circuit in both clock phases.

Using the charge analysis in the circuit starting at time t *(clock phase 1)*

$$q_1(t) = (V_1(t) - 0)C_1 \tag{28.1}$$

$$q_2(t) = (V_2(t) - 0)C_2 \tag{28.2}$$

$$q_3(t) = (0 - V_1(t))C_3 \tag{28.3}$$

At time $t + \tau$ *(clock phase 2)*

$$q_1(t+\tau) = (V_1(t+\tau) - 0)C_1 \tag{28.4}$$

$$q_2(t+\tau) = (V_2(t+\tau) - 0)C_2 \tag{28.5}$$

$$q_3(t+\tau) = (0 - 0)C_3 \tag{28.6}$$

At time $t + 2\tau$ *(clock phase 1)*

$$q_1(t+2\tau) = (V_1(t+2\tau) - 0)C_1 \tag{28.7}$$

$$q_2(t+2\tau) = (V_2(t+2\tau) - 0)C_2 \tag{28.8}$$

$$q_3(t+2\tau) = (0 - V_1(t+2\tau))C_3 \tag{28.9}$$

Other equations are required to be able to compute the transfer function. These equations come from the charge conservation. In clock phase 2 the charge of the three capacitors can not disappear since the charge can not be discharged through the opamp input terminals. This means that the charge on the capacitors at the end of clock phase 1 is equal to the charge of the capacitors during the whole clock phase 2.

$$q_1(t) + q_2(t) + q_3(t) = q_1(t+\tau) + q_2(t+\tau) + q_3(t+\tau) \tag{28.10}$$

The charge of C_1 and C_2 at the time $t + \tau$ are equal to the charge of C_1 and C_2 at time $t + 2\tau$ since no charge can be given by the opamp input.

$$q_1(t+\tau) + q_2(t+\tau) = q_1(t+2\tau) + q_2(t+2\tau) \tag{28.11}$$

Inserting the above equations into Eq. (28.10) gives

$$V_1(t)C_1 + V_2(t)C_2 - V_1(t)C_3 = V_1(t+\tau)C_1 + V_2(t+\tau)C_2 \tag{28.12}$$

Inserting equation Eq. (28.11) into Eq. (28.12) gives

$$V_1(t)C_1 + V_2(t)C_2 - V_1(t)C_3 = V_1(t+2\tau)C_1 + V_2(t+2\tau)C_2 \tag{28.13}$$

To compute the transfer function we make a Z-transformation of both sides.

$$V_1(z)(C_1 - C_3 - zC_1) = V_2(z)(zC_2 - C_2) \tag{28.14}$$

Solving for $V_2(z)/V_1(z)$ gives

$$\frac{V_2(z)}{V_1(z)} = \frac{C_1 - C_3 - zC_1}{zC_2 - C_2} = -\frac{C_1}{C_2}\frac{1+z}{z-1} = -\frac{C_1}{C_2}\frac{1+z^{-1}}{1-z^{-1}} \tag{28.15}$$

This is a bilinear inverting discrete-time accumulator (compare continuous-time integrator).

b) Each switch and capacitor has parasitic capacitances connected to ground. In Figure 59 the parasitics are shown.

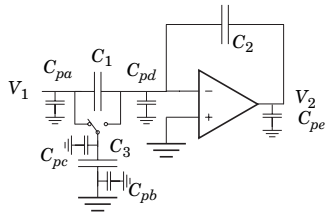


Figure 59: A bilinear inverting accumulator with parasitics.

C_{pa} is connected between the ideal input and ground and will not change the transfer function.

C_{pb} is connected between ground and ground and thereby not change the transfer function.

C_{pc} The parasitic capacitor is in parallel with C_3 and thereby it will change the transfer function according to

$$\frac{V_2(z)}{V_1(z)} = \frac{C_1 - C_3 - C_{pc} - zC_1}{zC_2 - C_2} = -\frac{C_1}{C_2}\frac{1+z}{z-1} - \frac{C_{pc}}{C_2}\frac{1}{z-1} = -\frac{C_1}{C_2}\frac{1+z^{-1}}{1-z^{-1}} - \frac{C_{pc}}{C_2}\frac{z^{-1}}{1-z^{-1}}$$

C_{pd} is connected between ground and virtual ground thereby not changing the transfer function.

C_{pe} is connected to the ideal operational amplifier and ground not changing the transfer function.

The transfer function is sensitive to parasitics.

29. Switched capacitor circuit.

a) The the two different clock phases of the circuit is shown Figure 60.

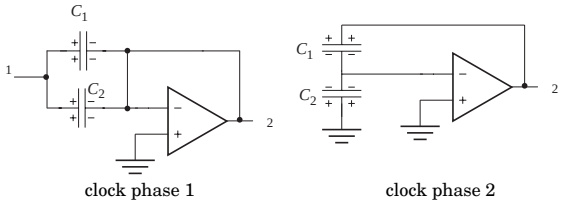


Figure 60: The circuit in the two different clock phases.

Starting in the clock phase 1 at time t:

$$q_1(t) = (V_1(t) - 0)C_1 \tag{29.1}$$

$$q_2(t) = (V_1(t) - 0)C_2 \tag{29.2}$$

At time $t + \tau$

$$q_1(t+\tau) = V_2(t+\tau)C_1 \tag{29.3}$$

$$q_2(t+\tau) = 0 \tag{29.4}$$

At time $t + 2\tau$

$$q_2(t+2\tau) = (V_1(t+2\tau) - 0)C_1 \tag{29.5}$$

$$q_2(t+2\tau) = (V_1(t+2\tau) - 0)C_2 \tag{29.6}$$

The last equation comes from the charge conservation. The charge at the end of clock phase t is equal to the charge during clock phase $t + \tau$ since no charge can vanish into the operational amplifier.

$$q_1(t) + q_2(t) = q_1(t+\tau) + q_2(t+\tau) \tag{29.7}$$

Inserting the above equations into Eq. (29.7) gives.

$$V_1(t)C_1 + V_1(t)C_2 = V_2(t+\tau)C_1 + 0 \tag{29.8}$$

performing z-transformation on both sides gives

$$V_1(z)(C_1 + C_2) = z^{1/2}V_2(z)C_1 \tag{29.9}$$

which gives the following transfer function

$$\frac{V_2(z)}{V_z(z)} = z^{-1/2}\frac{C_1 + C_2}{C_1} = z^{-1/2}\left(1 + \frac{C_2}{C_1}\right) \tag{29.10}$$

The factor $z^{-1/2}$ is just a time delay from the input to the output, it means that when the input is sampled at time t, the output will not be available until the time $t + \tau$.

b) There will be parasitic capacitances at both sides of each switch and the input and output of the operational amplifier as shown in Figure 61.

C_{pa} is connected between the ideal input and ground. Not changing the transfer function

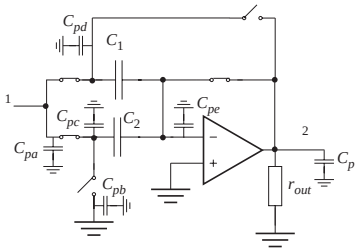


Figure 61: The SC-circuit with all parasitic capacitances.

C_{pb} is always connected to ground. Will not change the transfer function.

C_{pc} is connected between the ideal input and ground or between ground and ground and thereby not interacting with the transfer function.

C_{pd} is connected between ideal input and ground or the ideal output of the opamp and ground and thereby no change in the transfer function will appear.

C_{pe} is connected between the virtual ground and ground not causing any change in the transfer function.

C_{pf} is connected between the ideal output of the opamp and ground and thereby not changing the transfer function.

Hence, the circuit is insensitive of capacitive parasitics with respect to the transfer function.

c) To handle the offset voltage it is assumed to be a function of time with the properties, $V_{os}(t + n \cdot \tau) = V_{os}(t) \forall n$ and the Z-transform of $V_{os}(t)$ equals $V_{os}(z)$.

At time t, $t + 2\tau$, $t + 4\tau$ and so on, the potential at the negative input of the operational amplifier, V_x, will be equal to

$$V_x(t + n\tau) = \frac{A}{1 + A} V_{os}(t). \tag{29.11}$$

At time $t + \tau$, $t + 3\tau$, $t + 5\tau$ and so on, the potential at the negative input of the operational amplifier will be equal to

$$V_x(t + (n + 1)\tau) = V_{os}(t) - \frac{V_2(t + (n + 1)\tau)}{A}. \tag{29.12}$$

Using charge analysis gives:

$$q_1(t) = \left(V_1(t) - \frac{A}{1 + A} V_{os}(t)\right) C_1 \tag{29.13}$$

$$q_2(t) = \left(V_1(t) - \frac{A}{1 + A} V_{os}(t)\right) C_2 \tag{29.14}$$

$$q_1(t + \tau) = (V_2(t + \tau) - V_x(t + \tau)) C_1 =$$

$$= \left(V_2(t + \tau)\left(1 + \frac{1}{A}\right) - V_{os}(t)\right) C_1 \tag{29.15}$$

$$q_2(t + \tau) = -V_x(t + \tau) C_2 = \left(V_2(t + \tau)\frac{1}{A} - V_{os}(t)\right) C_2 \tag{29.16}$$

$$q_1(t + 2\tau) = \left(V_1(t + 2\tau) - \frac{A}{1 + A} V_{os}(t)\right) C_1 \tag{29.17}$$

$$q_2(t + 2\tau) = \left(V_1(t + 2\tau) - \frac{A}{1 + A} V_{os}(t)\right) C_2 \tag{29.18}$$

The charge conservation gives

$$q_1(t) + q_2(t) = q_1(t + \tau) + q_2(t + \tau) \tag{29.19}$$

Some manipulation gives

$$V_2(z) = z^{-1/2} \frac{1}{\left(1 + \frac{1}{A}\right) C_1 + \frac{C_2}{A}} (C_1 + C_2)\left(V_1(z) + \frac{1}{1 + A} V_{os}(z)\right)$$

$$= z^{-1/2}\left(1 + \frac{C_2}{C_1}\right) \frac{1}{1 + \frac{1}{A}\left(1 + \frac{C_2}{C_1}\right)} \left(V_1(z) + \frac{1}{1 + A} V_{os}(z)\right) \tag{29.20}$$

We can from this equation see that A goes to infinity we will return to the same answer as in a). Further, the circuit is insensitive to offset in the operational amplifier and we can get a design specification of the DC gain of operational amplifier to meet a certain specification of the whole system.

30. Switched capacitor circuit.

The circuit is shown in Figure 62.

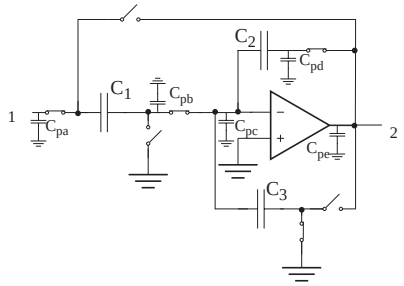


Figure 62: The SC circuit with parasitic capacitances

V_n is the input voltage of the amplifier. The transfer function can be derived by using charge analysis.

t:

$$q_1(t) = C_1(V_1(t) - V_n(t)) \tag{30.1}$$

$$q_2(t) = C_2(V_2(t) - V_n(t)) \tag{30.2}$$

$$q_3(t) = C_3(-V_n(t)) \tag{30.3}$$

t+τ:

$$q_1(t+\tau) = C_1 V_2(t+\tau) \tag{30.4}$$

$$q_2(t+\tau) = q_2(t) \tag{30.5}$$

$$q_3(t+\tau) = C_3(V_2(t+\tau) - V_n(t+\tau)) \tag{30.6}$$

t+2τ:

$$q_1(t+2\tau) = C_1(V_1(t+2\tau) - V_n(t+2\tau)) \tag{30.7}$$

$$q_2(t+2\tau) = C_2(V_2(t+2\tau) - V_n(t+2\tau)) \tag{30.8}$$

$$q_3(t+2\tau) = -C_3 V_n(t+2\tau) \tag{30.9}$$

Charge redistribution

$$q_2(t) + q_3(t) = q_2(t+\tau) + q_3(t+\tau) \tag{30.10}$$

$$q_1(t+2\tau) + q_2(t+2\tau) + q_3(t+2\tau) = q_1(t+\tau) + q_2(t+\tau) + q_3(t+\tau) \tag{30.11}$$

We also know that $V_2 = A(V_p - V_n)$ where V_p and V_n is the positive and negative input node of the OTA respectively. An offset voltage of the OTA is modelled by a voltage source at the positive input. Solve for V_n.

$$V_n(t) = -\frac{V_2}{A} + V_{os}(t), \text{ where } V_{os}(t+n\cdot\tau) = V_{os}(t) \forall n \tag{30.12}$$

Eq. (30.10) gives that

$$-C_3 V_n(t) = C_3(V_2(t+\tau) - V_n(t+\tau)) \tag{30.13}$$

Solving this equation gives

$$V_2(t+\tau) = \frac{V_2(t)}{(A+1)} \tag{30.14}$$

Inserting all necessary equations in Eq. (30.11) gives the following transfer function:

$$V_2(z) = -\frac{C_1}{C_2 + \frac{1}{A}(C_1 + C_2 + C_3)} \frac{(zV_1(z) - V_{os}(z))}{z - 1 + \frac{\frac{C_1}{A+1}}{C_2(A+1) + C_1 + C_3}} \tag{30.15}$$

b) Yes it is insensitive to parasitics.

Parasitics:

C_{pa} is connected to an ideal voltage source is will not affect the transfer function.

C_{pb} is connected between ground and virtual ground or ground and ground so it will not affect the transfer function.

C_{pc} is connected between ground and virtual ground so it will not affect the transfer function

C_{pd} is either connected to the output of the OTA or it will not be connected so it will not affect the transfer function.

C_{pe} is connected to the output of the OTA and thereby not change the transfer function.

31. Switched capacitor circuit.

a) See solution e)

b) Yes it is insensitive to parasitics. All parasitics are shown in Figure 63.

Parasitics:

C_{pa} are connected to an ideal voltage source is will not be affected.

C_{pb} are connected between ground and virtual ground so it will not be affected.

C_{pc} are connected to the output of the ideal OTA, so it will not be affected.

C_{pd} are either connected to the output of the OTA or a node which has a constant voltage. Hence, it will not affect the transfer function.

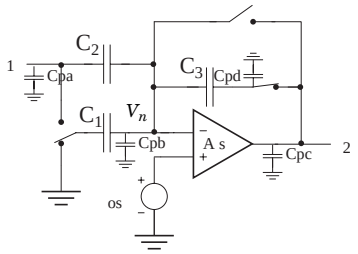


Figure 63: The SC circuit with parasitics.

c) The output from the SC-circuit is shown in Figure 64. Every other output

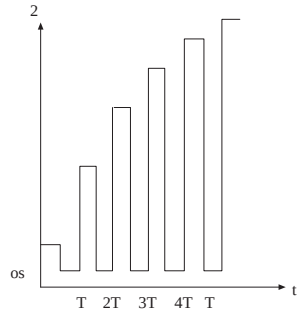


Figure 64: The output voltage as a function of the time.

(T/2) the output voltage will be V_{os}.

d) The circuit is insensitive to parasitics so the transfer function will not change. The speed of the circuit will decrease since a larger load is applied to the output of the amplifier.

e) Assume that at time t the circuit is in the state as shown in Figure 65.

During time t, t+2τ, t+4τ and so on, vi see that

$$V_2(t+2n\tau) = (V_{os}(t) - V_n(t+2n\tau))A \tag{31.1}$$

$$V_2(t+(2n+1)\tau) = (V_{os}(t) - V_2(t+(2n+1)\tau))A \tag{31.2}$$

Eq. (31.1) gives

$$V_n(t+2n\tau) = V_{os}(t) - \frac{V_2(t+2n\tau)}{A} \tag{31.3}$$

Eq. (31.2) gives

$$V_n(t+(2n+1)\tau) = \frac{V_{os}(t)}{1+\frac{1}{A}} \tag{31.4}$$

Use charge redistribution analysis

During time t:

$$q_1(t) = C_1\left(0 - V_{os}(t) + \frac{V_2(t)}{A}\right) \tag{31.5}$$

$$q_2(t) = C_2\left(V_1(t) - V_{os}(t) + \frac{V_2(t)}{A}\right) \tag{31.6}$$

$$q_3(t) = C_3\left(V_2(t) - V_{os}(t) + \frac{V_2(t)}{A}\right) \tag{31.7}$$

During time $t+\tau$ ($V_{os}(t+\tau) = V_{os}(t)$):

$$q_1(t+\tau) = C_1\left(V_1(t+\tau) - \frac{V_{os}(t)}{1+\frac{1}{A}}\right) \tag{31.8}$$

$$q_2(t+\tau) = C_2\left(V_1(t+\tau) - \frac{V_{os}(t)}{1+\frac{1}{A}}\right) \tag{31.9}$$

$$q_3(t+\tau) = q_3(t) \tag{31.10}$$

The charge across capacitor 3 is constant from time t to t+τ since it is not connected anywhere.

During time $t+2\tau$ ($V_{os}(t+2\tau) = V_{os}(t)$):

$$q_1(t+2\tau) = C_1\left(0 - V_{os}(t) + \frac{V_2(t+2\tau)}{A}\right) \tag{31.11}$$

$$q_2(t+2\tau) = C_2\left(V_1(t+2\tau) - V_{os}(t) + \frac{V_2(t+2\tau)}{A}\right) \tag{31.12}$$

$$q_3(t+2\tau) = C_3\left(V_2(t+2\tau) - V_{os}(t) + \frac{V_2(t+2\tau)}{A}\right) \tag{31.13}$$

Charge conservation:

$q_1(t+\tau) + q_2(t+\tau) + q_3(t+\tau) = q_1(t+2\tau) + q_2(t+2\tau) + q_3(t+2\tau)$

Inserting the above equations in the charge conservation equation and then a Z-transformation gives the transfer function (Z-transform of $V_{os}(t) = V_{os}(z)$)

$$V_2(z) = \frac{1}{C_3\left(1+\frac{1}{A}\right) + \frac{C_1+C_2}{A}} \cdot \frac{\left((C_1+C_2)z^{\frac{1}{2}} - C_2 z\right)V_1(z) + V_{os}(z)\frac{C_1+C_2}{1+A}}{z - \frac{C_3\left(1+\frac{1}{A}\right)}{C_3\left(1+\frac{1}{A}\right) + \frac{C_1+C_2}{A}}} \tag{31.14}$$

The solution for exercise a) is obtained by letting $A \to \infty$

$$V_2(z) = \frac{1}{C_3}\frac{(C_1+C_2)z^{\frac{1}{2}} - C_2 z}{z-1}V_1(z) \tag{31.15}$$

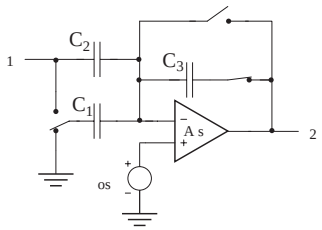


Figure 65: The switched capacitor circuit.

32. Switched capacitor circuit.

a) The SC circuit in the different clock phases are shown in Figure 66. We do a

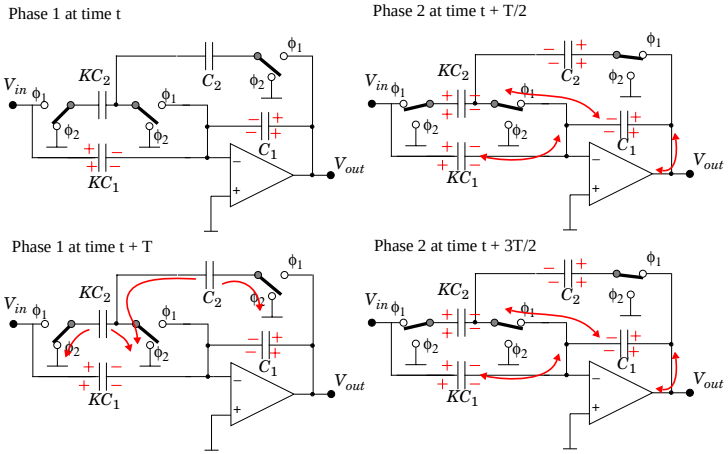


Figure 66: Switched capacitor circuit in different phases

charge redistribution analysis. First we state the initial conditions of the circuit.

Phase 1 at time t

$$q_1(t) = v_{out}(t) \cdot C_1; \tag{32.1}$$

$$q_2(t) = 0 \tag{32.2}$$

$$q_{2K}(t) = 0 \tag{32.3}$$

$$q_{1K}(t) = v_{in}(t) \cdot K \cdot C_1 \tag{32.4}$$

Phase 2 at time $t + T/2$

$$q_1(t+T/2) = v_{out}(t+T/2) \cdot C_1 \tag{32.5}$$

$$q_2(t+T/2) = v_{out}(t+T/2) \cdot C_2 \tag{32.6}$$

$$q_{2K}(t+T/2) = v_{in}(t+T/2) \cdot K \cdot C_2; \tag{32.7}$$

$$q_{1K}(t+T/2) = v_{in}(t+T/2) \cdot K \cdot C_1 \tag{32.8}$$

The charge on the negative input node of the OP $(q_1(t) + q_{1K}(t))$ is distributed between all four capacitances, i.e,

$$q_1(t) + q_{1K}(t) = q_1(t+T/2) + q_2(t+T/2) + \ldots \\ \ldots + q_{1K}(t+T/2) + q_{2K}(t+T/2) \tag{32.9}$$

Phase 1 at time $t + T$

$$q_1(t+T) = v_{out}(t+T) \cdot C_1; \; q_2(t+T) = 0; \tag{32.10}$$

$$q_{1K}(t+T) = v_{in}(t+T) \cdot C_1 \cdot K; \; q_{2K}(t+T) = 0 \tag{32.11}$$

and we get a charge conservation because no charge can leave the negative input node of the OP.

$$q_1(t+T) + q_{1K}(t+T) = q_1(t+T/2) + q_{1K}(t+T/2) \tag{32.12}$$

Phase 2 at time $t + 3T/2$

$$q_1(t+3T/2) = v_{out}(t+3T/2) \cdot C_1; \\ q_2(t+3T/2) = v_{out}(t+3T/2) \cdot C_2 \tag{32.13}$$

$$q_{2K}(t+3T/2) = v_{in}(t+3T/2) \cdot K \cdot C_2; \\ q_{1K}(t+3T/2) = v_{in}(t+3T/2) \cdot K \cdot C_1 \tag{32.14}$$

The charge on the negative input node of the OP is distributed between all four capacitances, i.e,

$$q_1(t+T) + q_{1K}(t+T) = q_1(t+3T/2) + q_2(t+3T/2) + \ldots \\ \ldots + q_{1K}(t+3T/2) + q_{2K}(t+3T/2) \tag{32.15}$$

By combining Eq. (32.12) with Eq. (32.15) we get

$$q_1(t+T/2) + q_{1K}(t+T/2) = q_1(t+3T/2) + q_2(t+3T/2) + \ldots \\ \ldots + q_{1K}(t+3T/2) + q_{2K}(t+3T/2) \tag{32.16}$$

which is equal to

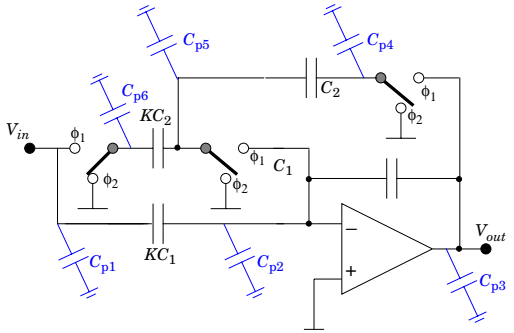
$$v_{out}(t+T/2) \cdot C_1 + v_{in}(t+T/2) \cdot C_1 \cdot K = v_{out}(t+3T/2) \cdot C_1 + \\ (v_{out}(t+3T/2) \cdot C_2 + v_{in}(t+T/2) \cdot C_2 \cdot K + v_{in}(t+T/2) \cdot C_1 \cdot K) \tag{32.17}$$

by using the z-transform we finally get the transfer function

$$\frac{V_{out}(z)}{V_{in}(z)} = \frac{K(z(C_2+C_1)-C_1)}{-(z(C_2+C_1)-C_1)} = -K \tag{32.18}$$

, i.e., an inverting amplifier.

b) To see if the circuit is sensitive to parasitics we examine all the parasitic capacitances and check whether they can destroy the operation.



C_{p1}... will not affect the transfer function because it is always connected to the input node.

C_{p2}... is shorted between ground a virtual ground.

C_{p3}... will not affect the transfer function because it is always connected to the output node.

C_{p4}... is either shorted or connected to the output node and will never contribute to the output.

C_{p5}... is either shorted to ground or virtual ground.

C_{p6}... is either shorted or connected to the input node and will never contribute to the output.

, i.e., the circuit is insensitive to parasitics.

c) If the switch transistors would have a non-negligible on-resistance the charging/discharging through them would not be instantaneously. This affects the speed of the circuit and not the transfer function. To compensate for this problem one have to make sure that we are using non-overlapping switching signals and that they are slow enough so that the circuit has time to settle properly.