ANTIK Exercises 2014

General information

Welcome to the 2012 versions of the ATIK and ANIK courses. Jointly referred to as the ANTIK courses. This is your exercise manual for this year and more information is found at:

http://www.es.isy.liu.se/courses/A*IK/lessons.html

We are currently compiling most of our material in a more handy format and you now find the new generation of our exercises manual. Unfortunately this (this year) implies that some of the solutions are found in multiple other sources. We have however indicated where to find the solutions in the exercises of this document.

K -- Kompedium

J&M - Johns & Martin

S - Schaumann

The teaching assistant can guide you through how to find the answers to the questions.

> ✗ As usual it is suggested to not print the whole document. Keep your laptop next to you... save some trees.

Exercises

Document history

Rev	Date	Comment	Issued/Created by
0,1	the old days.	Creation.	Anton Blad, Erik Säll, Robert Hägglund, K Ola Andersson, Niklas U Andersson, J Jacob Wikner, etc., etc.
...			
P2A	2012-01-13	Hard-core copy-paste from previous manual (framemaker).	Niklas U Andersson
P3A	2012-01-14	Cleaned up a bit to make it a bit shorter.	J Jacob Wikner
P4A	2012-01-26	Added dummy section, Niklas added some missed answers	Prakash Harikumar
P5A	2012-02-29	Added some more answers.	J Jacob Wikner
P6A	2014-02-07	Aligned with the exercise manual	J Jacob Wikner

EXERCISE SECTION 1: INTRODUCTION

1.1. Definitions of voltages and currents

As a quick reference, we have pasted the directions, and indicators to ports, currents, voltages, etc., for the NMOS and PMOS transistors in Figure 1.1.1.

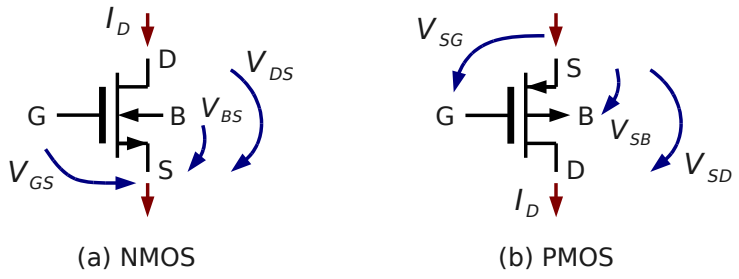


Figure 1.1.1: Schematic symbols of (a) NMOS and (b) PMOS transistors with voltages and currents indicated.

1.2. (Approximate) Device equations

General

For convenience we use a couple of 'abbreviations' and shorter forms, as:

$v_{eff} = V_{GS} - V_T$ (and $v_{eff} = V_{SG} - V_T$ for PMOS) is the effective gate voltage. (1)

$\alpha = \frac{\mu_0 C_{ox}}{2} \cdot \frac{W}{L}$, $K = \mu_0 C_{ox}$, $\beta = K \cdot \frac{W}{L}$, $S = \frac{W}{L}$ (2)

$\lambda = \frac{1}{V_\theta}$ is the channel length modulation. (3)

(Notice the deliberately "sloppy" notation with lower and upper cases.)

NMOS transistors

Cut-off region (subtreshold):

$V_{GS} < V_T$ or $v_{eff} < 0$ (4)

$I_D \approx 0$ (5)

✗ The current is considered to be more or less 0 for hand calculations. It should however be mentioned that nowadays one should not be too afraid to use the transistors in the sub-threshold region. As we get close to the threshold the gain of the transistor is comparatively

Linear region:

$V_{GS} \geq V_T$, or $v_{eff} > 0$
$V_{DS} < V_{GS} - V_T$, or $V_{DS} < v_{eff}$ (6)

$I_D \approx \frac{\mu_0 \cdot C_{ox}}{2} \cdot \frac{W}{L} \cdot \left(2(V_{GS} - V_T) \cdot V_{DS} - V_{DS}^2\right) = \alpha \cdot \left(2 v_{eff} V_{DS} - V_{DS}^2\right)$ (7)

Saturated region:

$V_{GS} \geq V_T$, or $v_{eff} > 0$
$V_{DS} \geq V_{GS} - V_T$, or $V_{DS} \geq v_{eff}$ (8)

$$I_D \approx \frac{\mu_0 \cdot C_{ox}}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_T)^2 \cdot \left(1 + \frac{V_{DS}}{V_\theta}\right) \approx \alpha \cdot v_{eff}^2 \quad (9)$$

Threshold voltage:

$$V_T \approx V_{T,0} + \gamma \cdot \left(\sqrt{2\Phi_F - V_{BS}} - \sqrt{2\Phi_F}\right) \quad (10)$$

✗ The higher source-bulk voltage the higher the threshold voltage, i.e., bad.

PMOS transistors

Cut-off region (subtreshold):

$V_{SG} < V_T$ or $v_{eff} < 0$ (11)

$I_D \approx 0$ (12)

Linear region:

$V_{SG} \geq V_T$, or $v_{eff} > 0$
$V_{SD} < V_{SG} - V_T$, or $V_{SD} < v_{eff}$ (13)

$$I_D \approx \frac{\mu_0 \cdot C_{ox}}{2} \cdot \frac{W}{L} \cdot \left(2(V_{SG} - V_T) \cdot V_{SD} - V_{SD}^2\right) = \alpha \cdot \left(2 v_{eff} V_{SD} - V_{SD}^2\right) \quad (14)$$

Saturated region:

$V_{SG} \geq V_T$, or $v_{eff} > 0$
$V_{SD} \geq V_{SG} - V_T$, or $V_{SD} \geq v_{eff}$ (15)

$$I_D \approx \frac{\mu_0 \cdot C_{ox}}{2} \cdot \frac{W}{L} \cdot (V_{SG} - V_T)^2 \cdot \left(1 + \frac{V_{SD}}{V_\theta}\right) \approx \alpha \cdot v_{eff}^2 \quad (16)$$

Threshold voltage:

$$V_T \approx V_{T,0} + \gamma \cdot \left(\sqrt{2\Phi_F - V_{SB}} - \sqrt{2\Phi_F}\right) \quad (17)$$

1.3. Circuit noise

Thermal noise

The thermal noise spectral density at the gate of a CMOS transistor is

$$v_t^2(f)=\frac{4kT\cdot\gamma}{g_m} \tag{18}$$

where γ traditionally was 2/3, but nowadays it can be higher than 1.

Flicker noise

The flicker noise spectral density at the gate of a CMOS transistor is

$$v_f^2(f)=\frac{K}{WLC_{ox}f} \tag{19}$$

where K is a constant.

> ✗ Integrating the noise spectral density over a certain frequency band gives you the noise power. Notice that, in both cases, an infinite noise power is obtained if integrating over all frequencies.

Approximate parameters for a 0.35-micron process

In Table 1.1 we have compiled some "older" process parameters for hand calculations that are also used throughout the exercises.

> ✗ Notice that more modern processes will have quite different values, but it is also more difficult to perform the hand calculations in the same way.

Param.	Unit	NMOS	PMOS	Comment
μ_0	$\mathrm{cm}^2/V\,s$	400	130	Charge mobility, "holes are slower than electrons".
C_{ox}	nF/cm^2	450	450	
V_θ	V	33	20	$L=1\,\mu m$
V_θ	V	100	50	$L=5\,\mu m$
$V_{T,0}$	V	0.47	0.62	The PMOS typically has higher threshold voltage ...
γ	$\sqrt{V}$	0.62	0.41	... but is less sensitive to bulk variations.
$2\Phi_F$	V	0.86	0.82	

Table 1.1: Some typical values for handcalculations.

EXERCISE SECTION 2: DC ANALYSIS

2.1. DC analysis on a common-source gain stage with cascodes

1. DC analysis on a common-source gain stage with cascodes.

We neglect the body effect and channel-length modulation in the DC calculations (AC analysis is performed in Ex. 9).

We define the effective gate-source voltage of an NMOS transistor as

$$V_{eff,n} = V_{GS} - V_T \tag{1.1}$$

and, similarly, the effective source-gate voltage of a PMOS transistor as

$V_{eff,p} = V_{SG} - V_T$ (different V_T for NMOS and PMOS transistors!)

We have the simplified current equation for a saturated transistor

$$I_D \approx \alpha \cdot V_{eff}^2 \tag{1.2}$$

Since the transistor sizes are equal for $M1$ and $M2$, and they have the same drain current, they will also have the same V_{eff}. Similarly, $M3$ and $M4$ will have the same V_{eff}.

For NMOS transistors ($M1$ and $M2$)

$$V_{eff,n} = \sqrt{\frac{I_D}{\alpha}} \approx 0{,}105 \text{ V} \tag{1.3}$$

and for PMOS transistors

$$V_{eff,p} = \sqrt{\frac{I_D}{\alpha}} \approx 0{,}185 \text{ V} \tag{1.4}$$

(α different for NMOS and PMOS transistors!)

Thus, $V_{in,DC} = V_{eff,n} + V_T = 0{,}105 + 0{,}47 \approx 0{,}58$ V. $V_{bias,2}$ is not determined by the current alone, we also need to know V_{DS} for $M1$. We have

$$V_{bias,2} = V_{DS,1} + V_{GS,2} = V_{DS,1} + V_{eff,n} + V_T \tag{1.5}$$

To ensure that $M1$ is properly saturated we choose

$$V_{DS,1} = V_{eff,n} + 0{,}2 \text{ V} \tag{1.6}$$

and thus

$$V_{bias,2} = 2 \cdot V_{eff,n} + V_T + 0{,}2 \text{ V} \approx 0.88 \text{ V} \tag{1.7}$$

We make a similar analysis for the PMOS part and find that

$$V_{bias,4} = V_{DD} - (V_{eff,p} + V_T) = 3{,}3 - (0{,}185 + 0{,}62) \approx 2{,}50 \text{ V} \tag{1.8}$$

To ensure that $M4$ is properly saturated we set

$V_{SD,4} = V_{eff,p} + 0{,}2$ V and find that

$V_{bias,3} = V_{DD} - (2 \cdot V_{eff,p} + V_T + 0{,}2) \approx 3{,}3 - (2 \cdot 0{,}185 + 0{,}62 + 0{,}2) = 2{,}11$ V

The output range is now given by the following relations

$$V_{out} \geq V_{DS,1} + V_{eff,n} = 2 \cdot V_{eff,n} + 0{,}2 \approx 0{,}41 \text{ V} \tag{1.9}$$

and

$$V_{out} \leq V_{DD} - (V_{SD,4} + V_{eff,p}) = V_{DD} - (2 \cdot V_{eff,p} + 0{,}2) \approx 2{,}73 \text{ V} \tag{1.10}$$

2.2. DC analysis of a bias circuit

2. DC analysis on a bias circuit.

Here we assume that all transistors are operating in the saturation region and that the channel-length modulation is neglected. Choose a suitable value of V_x, e.g., $V_x = 2V$. The maximum current through the circuit is

$$I_D \leq \frac{P_{diss}}{V_{DD}} = 5\mu A \tag{2.1}$$

The current through all the transistors is equal and

$$I_D = \frac{K_1}{2}\frac{W_1}{L_1}(V_{DD} - V_x - V_{T1})^2 \tag{2.2}$$

$$I_D = \frac{K_2}{2}\frac{W_2}{L_2}(V_x - V_{bias} - V_{T2})^2 \tag{2.3}$$

$$I_D = \frac{K_3}{2}\frac{W_3}{L_3}(V_{bias} - V_{T3})^2 \ . \tag{2.4}$$

Moreover,

$$V_{T2} = V_{T0} + \gamma(\sqrt{2\Phi_F - V_{SB}} - \sqrt{2\Phi_F}) \ . \tag{2.5}$$

Eq. (2.1) and Eq. (2.4) gives

$$\frac{W_3}{L_3} = \frac{2I_D}{K_3(V_{bias} - V_{T3})^2} \approx 3{,}3 \ . \tag{2.6}$$

Eq. (2.1) and Eq. (2.2) gives

$$\frac{W_1}{L_1} = \frac{2I_D}{K_1(V_{DD} - V_x - V_{T1})^2} \approx 0{,}37 \ . \tag{2.7}$$

Eq. (2.5) yields

$$V_{T2} = 0{,}846V \ , \tag{2.8}$$

and from Eq. (2.1) and Eq. (2.3) we obtain

$$\frac{W_2}{L_2} = \frac{2I_D}{K_2(V_x - V_{bias} - V_{T2})^2} \approx 0{,}56 \ . \tag{2.9}$$

2.3. DC analysis of a common-gate amplifier

3. DC analysis on a common-gate amplifier.

a) The transistor M_1 is in the cut-off regime as long as $V_{b1} - V_{T1} < V_1$ no (very small) current will flow through transistor M_1 so the output voltage will be equal to V_{dd}.

When the input voltage is lower than, but close to, $V_{b1} - V_{T1}$ the transistor will be saturated since $V_{DS} = V_{out} - V_1 > V_{b1} - V_1 - V_T > 0$, and V_{out} is close to $V_{dd} \geq V_{b1}$. The input voltage for which the transistor M_1 enters the linear region is depending on the value of V_{b1}, and can be computed as follows.

b) The current through transistor M_1 in saturation is

$$I_{D1} = \alpha(V_{b1} - V_1 - V_{T1})^2(1 + \lambda(V_{out} - V_1)) \tag{3.1}$$

In saturation the current through transistor M_1 must equal I_{bias}.

$$I_{bias} = \alpha(V_{b1} - V_1 - V_{T1})^2(1 + \lambda(V_{out} - V_1)) \tag{3.2}$$

Solving for $V_{out} - V_1$ gives the following expression.

$$V_{out} - V_1 = \frac{1}{\lambda}\frac{I_{bias}}{\alpha(V_{b1} - V_1 - V_{T1})} - \frac{1}{\lambda} \tag{3.3}$$

The transistor operates in the saturation region when $V_{out} - V_1 = V_{b1} - V_1 - V_{T1}$. Inserting Eq. (3.3) into previous equation and solving for V_1 gives the input voltage where the transition between the saturation and linear operation appears.

2.4. Simple gain stages with passive load

5. Simple gain stages with resistive load.

First considering the common-source stage.

a) The ESSS is shown in Figure 30. Where $R = 1/G$.

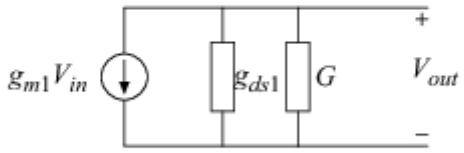


Figure 30: The ESSS of a common-source gain stage with resistive load.

b) The transfer function can be computed by using nodal analysis in the output node.

$$g_{m1}V_{in} + V_{out}(g_{ds1} + G) = 0 \tag{5.1}$$

The transfer function is

$$\frac{V_{out}}{V_{in}} = -\frac{g_{m1}}{g_{ds1} + G} \tag{5.2}$$

The output resistance can be computed by adding a voltage source V_x between the output node and ground. Then compute the current delivered by that voltage source when the input source/sources is zero (V_{in} equals zero).

$$\left.\frac{V_x}{I_x}\right|_{V_{in}=0} = \frac{1}{g_{ds1} + G} = R \parallel \frac{1}{g_{ds1}} \tag{5.3}$$

c) The transistor M_1 is in the cut-off regime when V_{in} is below V_T, yielding the output voltage equal to V_{DD}. Increasing the input voltage will give the $V_{ds1} > V_{gs1} - V_{T1} > 0$ and the transistor will operate in the saturation region and the output voltage will decrease quadratically with the input voltage. Increasing the voltage further will result in a transistor operating in the linear region and the output voltage will then decrease linearly with the input voltage.

d) Obviously, $V_{in} > V_T$. In the saturation region it holds that

$$V_{out} \approx V_{DD} - R\alpha(V_{in} - V_T)^2 \,. \tag{5.4}$$

For saturation it is required that

$$V_{out} \geq V_{in} - V_T \,. \tag{5.5}$$

Combining Eq. (5.4) and Eq. (5.5) yields

$$(V_{in} - V_T)^2 + \frac{(V_{in} - V_T)}{R\alpha} - \frac{V_{DD}}{R\alpha} \leq 0 \,. \tag{5.6}$$

The maximum input voltage is computed with equality in Eq. (5.6), hence

$$V_{in,\,max} = V_T - \frac{1}{2R\alpha} + \sqrt{\frac{1}{4R^2\alpha^2} + \frac{V_{DD}}{R\alpha}} \tag{5.7}$$

(The solution $\ldots - \sqrt{\ldots}$ is obviously false, since it yields $V_{in,\,max} < V_T$)

a) The ESSS of the common drain, common gate, and CMOS inverter is shown in Figure 31.

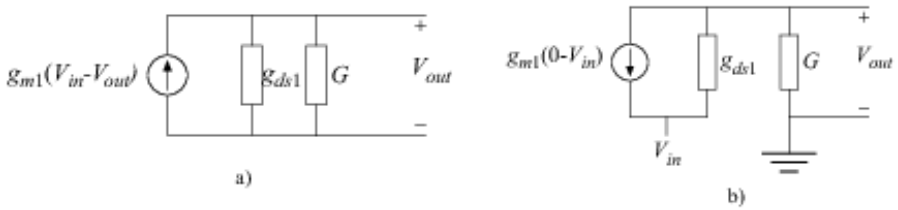


Figure 31: The ESSS for the a) common drain and b) common gate

b) Using nodal analysis at the output node gives the following DC gain and output resistance.

	CS	CD	CG
DC gain	$-\frac{g_{m1}}{g_{ds1}+G}$	$\frac{g_{m1}}{g_{m1}+g_{ds1}+G}$	$\frac{g_{m1}}{g_{ds1}+G}$
Output resistance	$\frac{1}{g_{ds1}+G}$	$\frac{1}{g_{m1}+g_{ds1}+G}$	$\frac{1}{g_{ds1}+G}$

c) Common-drain amplifier: The transistor M_1 is cut off until $V_{in} < V_{out} + V_T$. Then will it be in the saturation region.

Common-gate amplifier: The transistor will be in the linear or saturation region when the input voltage is low. An increased voltage will result that the transistor will be cut off.

d)

e) The ESSS of the common-drain circuit with the bulk effect is shown in Figure 32.

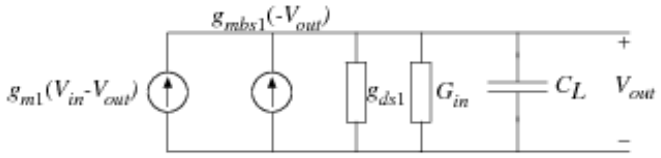


Figure 32: The ESSS of the common-drain circuit including the bulk effect.

The transfer function is given by

$$\frac{V_{out}}{V_{in}} = \frac{g_{m1}}{g_{m1}+g_{mbs1}+g_{ds1}+G_{in}} \tag{5.8}$$

The ESSS of the common-gate amplifier when the bulk effect is considered is shown in

Figure 33.

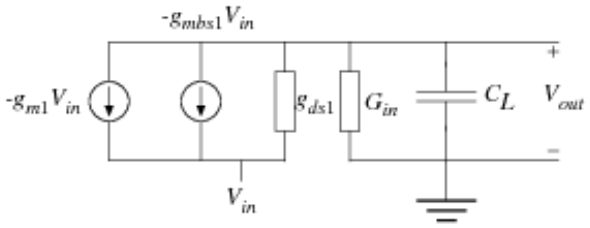


Figure 33: The ESSS of a common-gate amplifier when the bulk effect is considered.

The transfer function is

$$\frac{V_{out}}{V_{in}} = \frac{g_{ds1} + g_{m1} + g_{mbs1}}{g_{ds1} + G_{in}} \tag{5.9}$$

EXERCISE SECTION 3: AC ANALYSIS

3.1. Derivation of small-signal parameters 1

4. Derivation of small-signal parameters.

a) In the linear region we have the following expression for the current I_D.

$$I_D \approx \mu_0 \cdot C_{ox} \cdot \frac{W}{L} \cdot \left((V_{GS} - V_T) \cdot V_{DS} - \frac{V_{DS}^2}{2} \right) \tag{4.1}$$

Further we have

$$g_m = \frac{dI_D}{dV_{GS}} = \mu_0 \cdot C_{ox} \cdot \frac{W}{L} \cdot V_{DS} \tag{4.2}$$

$$g_{ds} = \frac{dI_D}{dV_{DS}} = \mu_0 \cdot C_{ox} \cdot \frac{W}{L} \cdot (V_{GS} - V_T - V_{DS}) \tag{4.3}$$

I_D is affected by the bulk-source voltage through variations in the threshold voltage, i.e.,

$$g_{mbs} = \frac{dI_D}{dV_{BS}} = \frac{\partial I_D}{\partial V_T} \cdot \frac{\partial V_T}{\partial V_{BS}} = -g_m \cdot \frac{\partial V_T}{\partial V_{BS}} \tag{4.4}$$

We have the following relation for the threshold voltage

$$V_T \approx V_{T,0} + \gamma(\sqrt{2\Phi_F - V_{BS}} - \sqrt{2\Phi_F}) \tag{4.5}$$

yielding

$$\frac{\partial V_T}{\partial V_{BS}} = -\frac{\gamma}{2 \cdot \sqrt{2\Phi_F - V_{BS}}} \tag{4.6}$$

and thus

$$g_{mbs} = \frac{\gamma}{2 \cdot \sqrt{2\Phi_F - V_{BS}}} \cdot g_m \tag{4.7}$$

This relation is also valid in the saturated region.

b) In the saturated region we have the following expression for I_D

$$I_D \approx \frac{\mu_0 \cdot C_{ox}}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_T)^2 \cdot (1 + \lambda \cdot V_{DS}) \tag{4.8}$$

Thus

$$g_m = \frac{dI_D}{dV_{GS}} \approx \mu_0 \cdot C_{ox} \cdot \frac{W}{L} \cdot (V_{GS} - V_T) = \sqrt{\left(\mu_0 \cdot C_{ox} \cdot \frac{W}{L} \cdot (V_{GS} - V_T) \right)^2}$$

$$\approx \sqrt{2 \cdot \mu_0 \cdot C_{ox} \cdot \frac{W}{L} \cdot I_D} \tag{4.9}$$

and

$$g_{ds} = \frac{dI_D}{dV_{DS}} = \frac{\mu_0 \cdot C_{ox}}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_T)^2 \cdot \lambda \approx \lambda \cdot I_D \tag{4.10}$$

3.2. Derivation of small-signal parameters 2 (K7)

TBD Solution to be added.

a)

b)

3.3. Small-signal parameters (K8)

TBD Solution to be added.

a)

Linear region.

b)

With higher gate voltage the resistance decreases.

3.4. Common-gate amplifier with non ideal input source

6. Common-gate amplifier with non ideal input source.
The small-signal equivalent is shown in Figure 34 where $R_{in} = 1/G_{in}$.

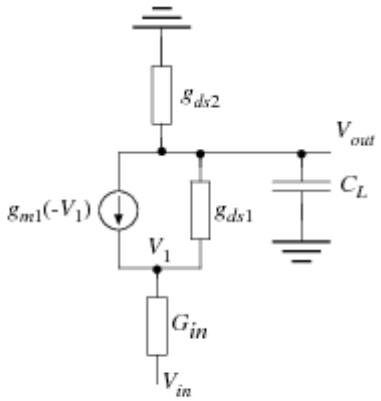


Figure 34: ESSS for the common-gate amplifier valid for low frequencies.

Using nodal analysis in the nodes V_1 and V_{out} gives the following equations

$$-g_{m1}V_1 + (V_{out} - V_1)g_{ds1} + (V_{in} - V_1)G_{in} = 0 \tag{6.1}$$

$$-g_{m1}V_1 + (V_{out} - V_1)g_{ds1} + V_{out}(g_{ds2} + sC_L) = 0 \tag{6.2}$$

Solving for V_1 in Eq. (6.1) and inserting it into Eq. (6.2) results in

$$\frac{V_{out}}{V_{in}} = \frac{G_{in}(g_{m1} + g_{ds1})}{g_{ds1}G_{in} + g_{ds2}(G_{in} + g_{m1} + g_{ds1}) + sC_L(g_{m1} + G_{in} + g_{ds1})} \approx \frac{G_{in}g_{m1}}{g_{ds1}G_{in} + g_{ds2}(G_{in} + g_{m1}) + sC_L(g_{m1} + G_{in})} \tag{6.3}$$

where $g_{m1} \gg g_{ds1}$ is assumed.

The DC gain is computed by setting $s = 0$ and the location of the first pole is computed from Eq. (6.3) by comparing with the transfer function

$$\frac{V_{out}}{V_{in}} = \frac{A_0}{1 + \frac{s}{p_1}} \tag{6.4}$$

The DC gain and the first pole can then be expressed as

$$A_0 \approx \frac{G_{in}g_{m1}}{g_{ds2}(g_{m1} + G_{in}) + g_{ds1}G_{in}} \tag{6.5}$$

$$p_1 = \frac{g_{ds2}(g_{m1} + G_{in}) + g_{ds1}G_{in}}{(g_{m1} + G_{in})C_L} \tag{6.6}$$

b) C_{gs1} is connected from node V_1 to ground. The nodal analysis in node V_1 and V_{out} gives:

$$-g_{m1}V_1 + (V_{out} - V_1)g_{ds1} + (V_{in} - V_1)G_{in} - V_1 sC_{gs1} = 0 \tag{6.7}$$

$$g_{m1}V_1 + (V_{out} - V_1)g_{ds1} + V_{out}(g_{ds2} + sC_L) = 0 \tag{6.8}$$

Solving for V_1 in Eq. (6.8)

$$\frac{V_1}{V_{out}} = \frac{g_{ds1} + g_{ds2} + sC_L}{g_{m1} + g_{ds1}} \tag{6.9}$$

Inserting into Eq. (6.7) gives

$$\frac{V_{out}}{V_{in}} = \frac{G_{in}(g_{m1} + g_{ds1})}{a + bs + cs^2} \tag{6.10}$$

where

$$a = g_{ds1}G_{in} + g_{ds2}(G_{in} + g_{m1} + g_{ds1}) \tag{6.11}$$

$$b = C_{gs1}(g_{ds1} + g_{ds2}) + C_L(g_{ds1} + G_{in} + g_{m1}) \tag{6.12}$$

$$c = C_{gs1}C_L \tag{6.13}$$

The load capacitance is often much larger than the parasitic capacitances. This results in that the load capacitor will be give rise to the dominant pole and the parasitic capacitances will contribute to the pole located much higher in frequency. When it is a large difference between the capacitances, the poles will be well separated. For well separated poles the following approximation holds.

$$\left(1 + \frac{s}{p_1}\right)\left(1 + \frac{s}{p_2}\right) = 1 + s\left(\frac{1}{p_1} + \frac{1}{p_2}\right) + \frac{s^2}{p_1 p_2} \approx 1 + \frac{s}{p_1} + \frac{s^2}{p_1 p_2} \tag{6.14}$$

Comparing Eq. (6.14) and Eq. (6.10) gives the following poles.

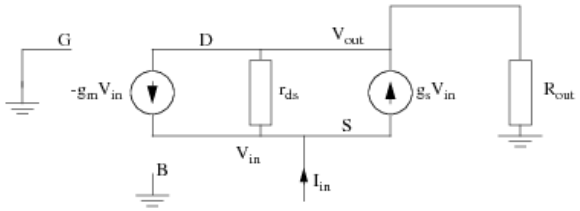
$$p_1 \approx \frac{a}{b} = \frac{g_{ds1}G_{in} + g_{ds2}(G_{in} + g_{m1} + g_{ds1})}{C_{gs1}(g_{ds1} + g_{ds2}) + C_L(g_{ds1} + G_{in} + g_{m1})} \approx \frac{g_{ds1}G_{in} + g_{ds2}(G_{in} + g_{m1})}{C_L(G_{in} + g_{m1})} \tag{6.15}$$

$$p_2 \approx \frac{a}{cp_1} = \frac{b}{c} \approx \frac{g_{ds1} + G_{in} + g_{m1}}{C_{gs1}} \tag{6.16}$$

3.5. Common-gate amplifier input impedance (K3)

Exercise K3

Small Signal Model:



When using y- or z- parameters to derive the input impedance, either the output current or the output voltage should be set to zero. When analysing circuits where the input resistance depends on the load impedance (the CG stage is such a circuit) it is more convenient to include the load in the analysis and leaving the output open. This has be done in the above small signal model and gives the following nodal equations:

$$\begin{cases} I_{in} = V_{in}g_m + (V_{in} - V_{out})g_{ds} + g_sV_{in} \\ V_{in}g_m + (V_{in} - V_{out})g_{ds} + g_sV_{in} = V_{out}G_{out} \end{cases} \Rightarrow r_{in} = \frac{V_{in}}{I_{in}} =$$

$$= \frac{\left(1 + \frac{g_{ds}}{G_{out}}\right)}{g_{ds} + g_s + g_m} \approx \frac{1}{g_m}\left(1 + \frac{R_{out}}{r_{ds}}\right)$$

3.6. Amplifier stages with active load

7. Amplifier stages with active load.

a) The ESSS of the four amplifier stages is shown in Figure 35.

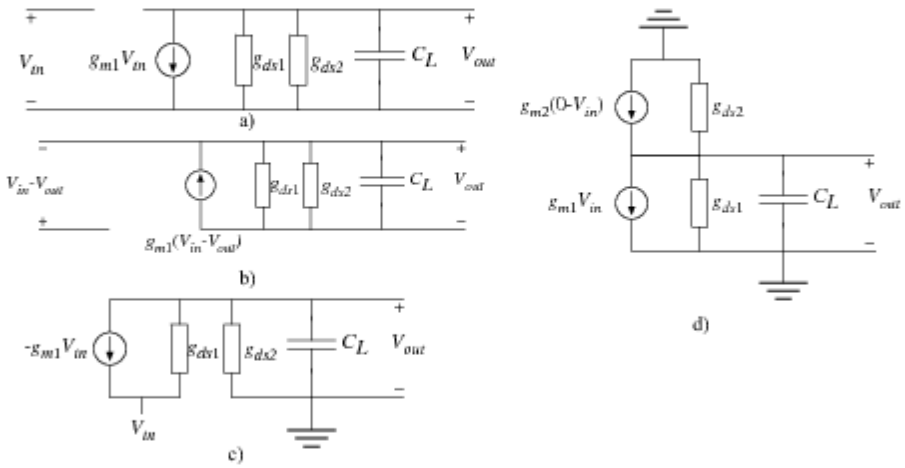


Figure 35: The ESSS of the amplifiers with active load. a) Common source, b) common drain, c) common gate, and d) CMOS inverter

The bulk effect is neglected.

b and c) To calculate the DC gain and the dominating pole only the capacitance C_L needs to be considered.

Nodal analysis of the *common-source* amplifier

$$g_{m1}V_{in} + V_{out}(g_{ds1} + g_{ds2} + sC_L) = 0 \tag{7.1}$$

gives the transfer function

$$\frac{V_{out}}{V_{in}} = -\frac{g_{m1}}{g_{ds1} + g_{ds2} + sC_L} = -\frac{g_{m1}}{g_{ds1} + g_{ds2}} \frac{1}{1 + \dfrac{s}{\dfrac{g_{ds1} + g_{ds2}}{C_L}}} = -\frac{A_0}{1 + \dfrac{s}{p_1}} \tag{7.2}$$

where A_0 is the DC gain and p_1 is the dominating pole.

The output resistance is compute by adding a voltage source at the output, V_x, and compute the current delivered from the source when the input source is zeroed. This gives $I_x = V_x(g_{ds1} + g_{ds2})$ and the output resistance

$$r_{out} = \frac{V_x}{I_x} = \frac{1}{g_{ds1} + g_{ds2}} \tag{7.3}$$

Nodal analysis for the *common-drain* amplifier

$$-g_{m1}(V_{in} - V_{out}) + V_{out}(g_{ds1} + g_{ds2} + sC_L) = 0 \tag{7.4}$$

gives the transfer function

$$\frac{V_{out}}{V_{in}} = \frac{g_{m1}}{g_{m1} + g_{ds1} + g_{ds2}} \frac{1}{1 + \dfrac{s}{\dfrac{g_{m1} + g_{ds1} + g_{ds2}}{C_L}}} \tag{7.5}$$

The output current through the output source equals $I_x = V_x(g_{ds1} + g_{ds1} + g_{m1})$ and the output resistance

$$r_{out} = \frac{V_x}{I_x} = \frac{1}{g_{ds1} + g_{ds2} + g_{m1}} \tag{7.6}$$

The *common-gate* amplifier:

$$-g_{m1}V_{in} + (V_{out} - V_{in})g_{ds1} + V_{out}(g_{ds2} + sC_L) = 0 \tag{7.7}$$

gives the transfer function

$$\frac{V_{out}}{V_{in}} = \frac{g_{m1} + g_{ds1}}{g_{ds1} + g_{ds2}} \frac{1}{1 + \dfrac{s}{\dfrac{g_{ds1} + g_{ds2}}{C_L}}} \tag{7.8}$$

The output current through the output source equals $I_x = V_x(g_{ds1} + g_{ds2})$ an the output resistance

$$r_{out} = \frac{V_x}{I_x} = \frac{1}{g_{ds1} + g_{ds2}} \tag{7.9}$$

The *CMOS inverter*

$$(g_{m1} + g_{m2})V_{in} + (g_{ds1} + g_{ds2} + sC_L)V_{out} = 0 \tag{7.10}$$

giving the transfer function

$$\frac{V_{out}}{V_{in}} = -\frac{g_{m1} + g_{m2}}{g_{ds1} + g_{ds2}} \frac{1}{1 + \dfrac{s}{\dfrac{g_{ds1} + g_{ds2}}{C_L}}} \tag{7.11}$$

The output resistance is given by

$$r_{out} = \frac{V_x}{I_x} = \frac{1}{g_{ds1} + g_{ds2}} \tag{7.12}$$

Summary:

	DC gain	Output resistance	Bandwidth
Common source	$-\frac{g_{m1}}{g_{ds1}+g_{ds2}}$	$\frac{1}{g_{ds1}+g_{ds2}}$	$\frac{g_{ds1}+g_{ds2}}{C_L}$
Common drain	$\frac{g_{m1}}{g_{m1}+g_{ds1}+g_{ds2}}$	$\frac{1}{g_{m1}+g_{ds1}+g_{ds2}}$	$\frac{g_{m1}+g_{ds1}+g_{ds2}}{C_L}$
Common gate	$\frac{g_{m1}+g_{ds1}}{g_{ds1}+g_{ds2}}$	$\frac{1}{g_{ds1}+g_{ds2}}$	$\frac{g_{ds1}+g_{ds2}}{C_L}$
CMOS inverter	$-\frac{g_{m1}+g_{m2}}{g_{ds1}+g_{ds2}}$	$\frac{1}{g_{ds1}+g_{ds2}}$	$\frac{g_{ds1}+g_{ds2}}{C_L}$

In principle we can see that in a single stage amplifier the DC gain can approximately be expressed as $g_{m,in}/g_{out} = g_{m,in}r_{out}$ and the bandwidth is $g_{out}/C_L = 1/(r_{out}C_L)$.

d) The highest gain is obtained in a CMOS inverter. The circuit with highest bandwidth is the common-drain amplifier.

3.7. Current mirrors

8. Current mirrors.

a) The ESSS of the simple current mirror is shown in Figure 36a.

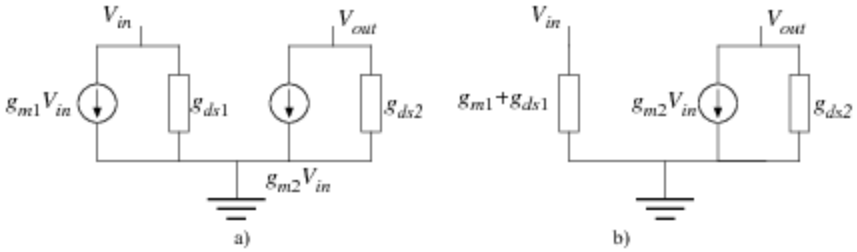


Figure 36: a) The ESSS for the simple current mirror. b) Simplified ESSS for the simple current mirror.

The input resistance is computed by adding a input voltage source to V_{in} and computing the current delivered by the source. The output should be terminated by the resistive load R_{load}.

$$I_{in} = g_{m1}V_{in} + V_{in}g_{ds1} = V_{in}(g_{ds1} + g_{m1}) \tag{8.1}$$

We see that if a transistor has a connection between its drain and gate, called diode-connected, the small-signal model will be a resistor with the value $g_{m1} + g_{ds1}$ as shown in Figure 36b. The input resistance is

$$r_{in} = \frac{V_{in}}{I_{in}} = \frac{1}{g_{m1} + g_{ds1}} \tag{8.2}$$

The output resistance is computed by adding a voltage source at the output and computing the current it delivers. This will give the output resistance equal to

$$r_{out} = \left.\frac{V_{out}}{I_{out}}\right|_{I_{in}=0} = \frac{1}{g_{ds2}} \tag{8.3}$$

The ESSS of the cascode current mirror is shown in Figure 37.

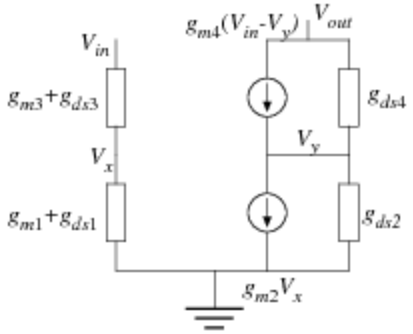


Figure 37: The ESSS of a cascode current mirror.

The input current is given by $I_{in} = (V_{in} - V_x)(g_{m3} + g_{ds3}) = V_x(g_{m1} + g_{ds1})$. The node voltage V_x can be eliminated from the equations and the output resistance is given by

$$r_{in} = \frac{V_{in}}{I_{in}} = \frac{g_{m1} + g_{ds1} + g_{m3} + g_{ds3}}{(g_{m1} + g_{ds1})(g_{m3} + g_{ds3})} \approx \frac{g_{m1} + g_{m3}}{g_{m1}g_{m3}} = \frac{1}{g_{m1}} + \frac{1}{g_{m3}} \tag{8.4}$$

The output current is given by

$$I_{out} = g_{m4}(-V_y) + g_{ds4}(V_{out} - V_y) = g_{m2}0 + g_{ds2}V_y \tag{8.5}$$

since $I_{in} = 0$ and thereby is $V_x = 0$. The output resistance is given by

$$r_{out} = \frac{V_{out}}{I_{out}} = \frac{g_{ds2} + g_{ds4} + g_{m4}}{g_{ds2}g_{ds4}} \approx \frac{g_{m4}}{g_{ds2}g_{ds4}} \tag{8.6}$$

The ESSS of the wide-swing current mirror is shown in Figure 38.

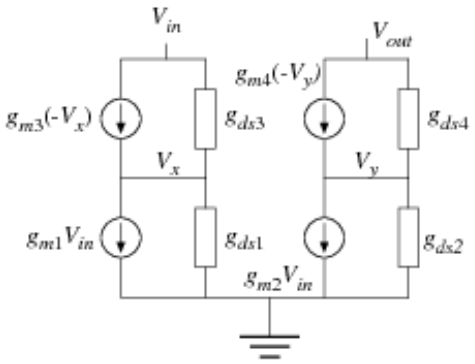


Figure 38: The ESSS of a wide-swing current mirror.

The input current equals $I_{in} = g_{m3}(-V_x) + (V_{in} - V_x)g_{ds3} = V_{in}g_{m1} + V_x g_{ds1}$. The input resistance is

$$r_{in} = \frac{V_{in}}{I_{in}} = \frac{g_{ds1} + g_{ds3} + g_{m3}}{g_{m1}(g_{ds3} + g_{m3}) + g_{ds1}g_{ds3}} \approx \frac{g_{m3}}{g_{m1}(g_{ds3} + g_{m3})} = \frac{1}{g_{m1}} \tag{8.7}$$

The output current is given by

$$I_{out} = g_{m4}(-V_y) + g_{ds4}(V_{out} - V_y) = g_{m2}0 + g_{ds2}V_y \tag{8.8}$$

The output resistance is

$$r_{out} = \frac{V_{out}}{I_{out}} = \frac{g_{ds2} + g_{ds4} + g_{m4}}{g_{ds2}g_{ds4}} \approx \frac{g_{m4}}{g_{ds2}g_{ds4}} \tag{8.9}$$

b) The lowest possible V_{ds} of a transistor in the saturation region, V_{dssat}, is $V_{dssat} = V_{gs} - V_T$. The V_{dssat} is expressed as a function of the drain current in a transistor in the following way.

$$I_D = \alpha(V_{gs} - V_T)^2 = \alpha V_{dssat}^2 \tag{8.10}$$

Solving for V_{dssat} gives

$$V_{dssat} = \sqrt{\frac{I_D}{\alpha}} \tag{8.11}$$

The minimum gate source voltage for a transistor that is operating in the saturation region is

$$V_{gsmin} = V_{dssat} + V_T = \sqrt{\frac{I_D}{\alpha}} + V_T \tag{8.12}$$

The minimum voltage is derived by determining the minimum voltage required to ensure that all transistors are operating in the saturation region for each possible way from ground to the node of interest, not passing directly between the gate to the drain.

The lowest possible input/output voltage of the simple current mirror is

$$V_{inmin} = max\{V_{gsmin1}, V_{dssat1}\} = V_{gsmin1} = \sqrt{\frac{I_{in}}{\alpha_1}} + V_{T1} \tag{8.13}$$

$$V_{outmin} = V_{dssat2} = \sqrt{\frac{I_{out}}{\alpha_2}} \tag{8.14}$$

The lowest possible input/output voltage for the cascode current mirror is

$$V_{inmin} = V_{gsmin1} + V_{gsmin3} = \sqrt{\frac{I_{in}}{\alpha_1}} + V_{T1} + \sqrt{\frac{I_{in}}{\alpha_3}} + V_{T3} \tag{8.15}$$

$$\begin{aligned} V_{outmin} &= max\{V_{dssat2} + V_{dssat4}, V_{gsmin1} + V_{gsmin3} - V_{gsmin4} + V_{dssat4}\} = \\ &\sqrt{\frac{I_{in}}{\alpha_1}} + V_{T1} + \sqrt{\frac{I_{in}}{\alpha_3}} + V_{T3} - \sqrt{\frac{I_{out}}{\alpha_4}} - V_{T4} + \sqrt{\frac{I_{out}}{\alpha_4}} = \\ &\sqrt{\frac{I_{in}}{\alpha_1}} + V_{T1} + \sqrt{\frac{I_{in}}{\alpha_3}} + V_{T3} - V_{T4} \end{aligned} \tag{8.16}$$

The lowest possible input/output/bias voltage for the wide-swing current mirror is.

$$V_{inmin} = max\{V_{gsmin1}, V_{dssat1} + V_{dssat3}\} = \sqrt{\frac{I_{in}}{\alpha_1}} + V_{T1} \tag{8.17}$$

$$\begin{aligned} V_{outmin} &= max\{V_{dssat2} + V_{dssat4}, V_{dssat1} + V_{gsmin3} - V_{gsmin4} + V_{dssat4}\} = \\ &\sqrt{\frac{I_{in}}{\alpha_1}} + \sqrt{\frac{I_{in}}{\alpha_3}} + V_{T3} - V_{T4} \end{aligned} \tag{8.18}$$

$$\begin{aligned} V_{biasmin} &= max\{V_{dssat1} + V_{gsmin3}, V_{dssat2} + V_{gsmin4}\} = \\ &max\left\{\sqrt{\frac{I_{in}}{\alpha_1}} + \sqrt{\frac{I_{in}}{\alpha_3}} + V_{T3}, \sqrt{\frac{I_{out}}{\alpha_2}} + \sqrt{\frac{I_{out}}{\alpha_3}} + V_{T4}\right\} \end{aligned} \tag{8.19}$$

Summary:

	Simple	Cascode	Wide-Swing
Input impedance	$\frac{1}{g_{m1}+g_{ds1}}$	$\frac{1}{g_{m1}}+\frac{1}{g_{m3}}$	$\frac{1}{g_{m1}}$
Output impedance	$\frac{1}{g_{ds2}}$	$\frac{g_{m4}}{g_{ds2}g_{ds4}}$	$\frac{g_{m4}}{g_{ds2}g_{ds4}}$
Lowest input voltage	$\sqrt{\frac{I_{in}}{\alpha_1}}+V_{T1}$	$\sqrt{\frac{I_{in}}{\alpha_1}}+V_{T1}+\sqrt{\frac{I_{in}}{\alpha_3}}+V_{T3}$	$\sqrt{\frac{I_{in}}{\alpha_1}}+V_{T1}$
Lowest output voltage	$\sqrt{\frac{I_{out}}{\alpha_2}}$	$\sqrt{\frac{I_{in}}{\alpha_1}}+V_{T1}+\sqrt{\frac{I_{in}}{\alpha_3}}+V_{T3}-V_{T4}$	$\sqrt{\frac{I_{in}}{\alpha_1}}+\sqrt{\frac{I_{in}}{\alpha_3}}+V_{T3}-V_{T4}$
Lowest bias voltage	-	-	See above

c) The current mirror that is most ideal is the wide swing and cascode current mirror since they have the lowest input resistance and the highest output resistance. But by looking at the possible input/output voltage the wide-swing current mirror is best. If the chip area is of concern then the simplest current mirror is the one to choose. Depending on the application each of these current mirrors can be the best choice.

3.8. Gain stages with cascodes

9. Gain stages with cascodes.

a) A gain-boosted common-source amplifier.

b) We first compute the output impedance of a cascode as shown in Figure 39a with the ESSS

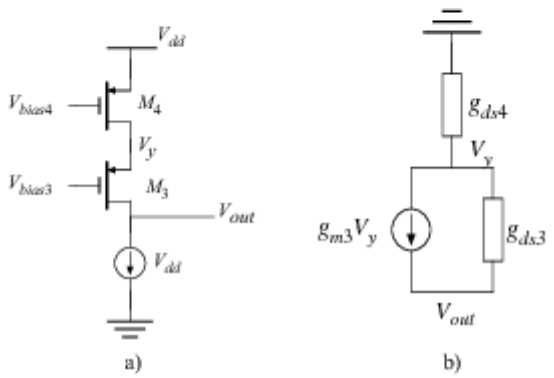


Figure 39: a) A cascode transistor. b) The ESSS of the circuit.

as shown in Figure 39b. The current I_{out} is

$$I_{out} = V_y g_{ds4} = -g_{m3}V_y - g_{ds3}(V_y - V_{out}) \tag{9.1}$$

The output resistance is

$$r_{out} = \frac{V_{out}}{I_{out}} = \frac{g_{m3} + g_{ds3} + g_{ds4}}{g_{ds3}g_{ds4}} \approx \frac{g_{m3}}{g_{ds3}g_{ds4}} = \frac{A_3}{g_{ds4}} \tag{9.2}$$

where A_3 is the gain of the transistor M_3. The two transistors above can be replaced by a resistor with the values of A_3/g_{ds4} when we are computing the small-signal characteristics.

The simplified ESSS of the amplifier is shown in Figure 40. The DC gain can be computed

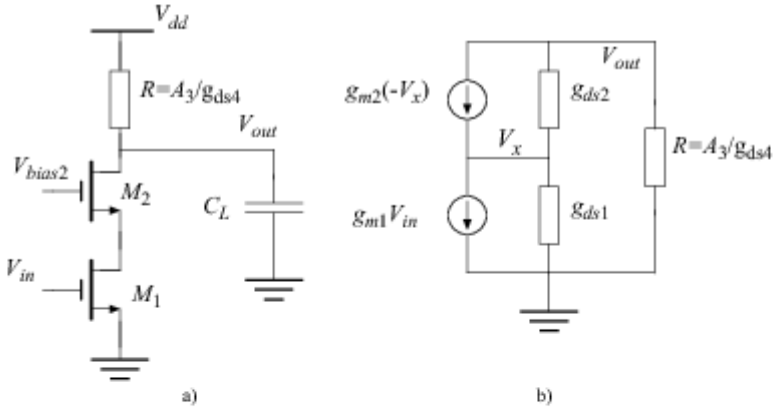


Figure 40: a) Equivalent low frequency folded cascode amplifier. b) ESSS of the simplified amplifier.

using the following equations.

$$g_{m1}V_{in} + V_x g_{ds1} + g_{m2}V_x + (V_x - V_{out})g_{ds2} = 0 \tag{9.3}$$

$$(-g_{m2})V_x + (V_{out} - V_x)g_{ds2} + V_{out}G = 0 \tag{9.4}$$

Solving for V_{out} gives the following DC gain.

$$\frac{V_{out}}{V_{in}} = -\frac{g_{m1}(g_{m2} + g_{ds2})}{g_{ds1}g_{ds2} + G(g_{ds1} + g_{ds2} + g_{m2})} \approx -\frac{g_{m1}}{\frac{g_{ds1}g_{ds2}}{g_{m2}} + G} = -\frac{g_{m1}}{\frac{g_{ds1}g_{ds2}}{g_{m2}} + \frac{g_{ds3}g_{ds4}}{g_{m3}}} \tag{9.5}$$

The DC gain can be expressed as g_{m1}/g_{out} where the output conductance is the sum of the conductances seen from the output to ground and from the output to the positive supply voltage (the parallel connection of the two output resistances seen up and down from the output). The cascode transistors are used to enhance the output resistance by the gain of the cascode transistors, i.e. g_{m2}/g_{ds2} and g_{m3}/g_{ds3} respectively.

The DC gain of the gain-boosted amplifier can be calculated in the same way as the cascode transistors. The upper part of the transistor together with its small-signal equivalent is shown in Figure 41

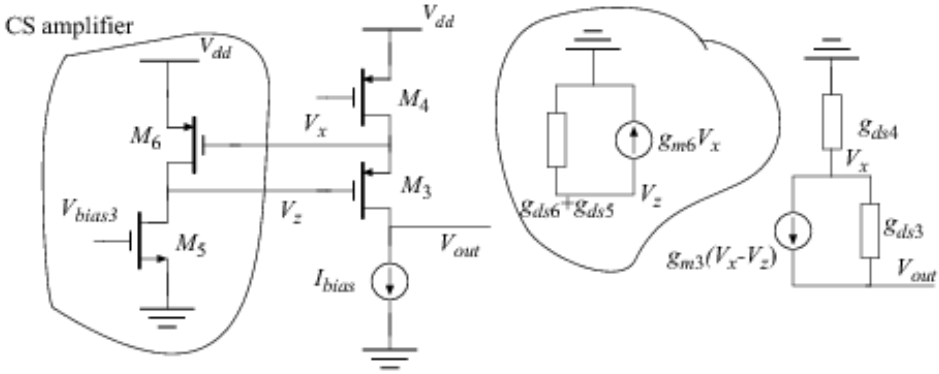


Figure 41: A part of the gain-boosted cascode transistor.

We start to calculate the DC gain of the common-source amplifier to

$$\frac{V_z}{V_x} = -\frac{g_{m6}}{g_{ds5} + g_{ds6}} = A_{cs} \tag{9.6}$$

Continuing to derive the output resistance by setting up the current delivered by the output source.

$$I_{out} = -g_{m3}(V_x - V_z) + (V_{out} - V_x)g_{ds3} = V_x g_{ds4} \tag{9.7}$$

Solving for V_{out} and eliminating V_x gives

$$r_{out} = \frac{V_{out}}{I_{out}} = \frac{g_{ds3} + g_{ds3} + g_{m3} - A_{cs}g_{m3}}{g_{ds3}g_{ds4}} \approx \frac{A_{cs}g_{m3}}{g_{ds3}g_{ds4}} = \frac{g_{m5}}{g_{ds5} + g_{ds6}g_{ds3}g_{ds4}} \frac{g_{m3}}{} \tag{9.8}$$

The output impedance is increased by the gain of the common-source amplifier, A_{cs}.

The same type of computation as the one above will give the output DC gain of the whole circuit. The simplified small-signal schematic for the gain-boosted amplifier is shown in

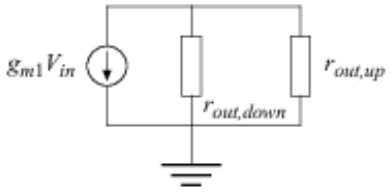


Figure 42: A simplified ESSS of the gain-boosted amplifier.

Figure 42.

The output resistance

$$r_{out,\,up} = \frac{g_{m5}}{g_{ds5} + g_{ds6}g_{ds3}g_{ds4}} \frac{g_{m3}}{} \tag{9.9}$$

and

$$r_{out,\,down} = \frac{g_{m8}}{g_{ds8} + g_{ds7}g_{ds2}g_{ds1}} \frac{g_{m2}}{} \tag{9.10}$$

The DC gain is given by

$$\frac{V_{out}}{V_{in}} \approx \frac{g_{m1}}{g_{out}} \approx \frac{g_{m1}}{\frac{1}{r_{out,\,up}} + \frac{1}{r_{out,\,down}}} \tag{9.11}$$

c) The parasitic capacitance in the signal path for the amplifier with cascodes is much lower since we do not have the C_{gs8} in the signal path compared with the amplifier using gain boosting.

The bandwidth is g_{out}/C_L for a single stage amplifier. The output conductance of the gain boosted amplifier is much less than the one width cascodes. Hence, the bandwidth of the gain boosted amplifier is much lower than the amplifier with cascodes.

Summary:

	DC gain	**First pole (bandwidth)**
Common source	$-\frac{g_{m1}}{g_{ds1} + g_{ds2}}$	$\frac{g_{ds1} + g_{ds2}}{C_L}$

Common source with cascodes	$-\dfrac{g_{m1}}{\dfrac{g_{ds1}g_{ds2}}{g_{m2}}+\dfrac{g_{ds3}g_{ds4}}{g_{m3}}}$	$\dfrac{\dfrac{g_{ds1}g_{ds2}}{g_{m2}}+\dfrac{g_{ds3}g_{ds4}}{g_{m3}}}{C_L}$
Gain-boosted common-source amplifier	$-\dfrac{g_{m1}}{g_{out}}$	$\dfrac{g_{out}}{C_L}$

where $g_{out} = \dfrac{g_{ds1}g_{ds2}}{g_{m2}}\dfrac{g_{ds8}+g_{ds7}}{g_{m8}} + \dfrac{g_{ds3}g_{ds4}}{g_{m3}}\dfrac{g_{ds5}+g_{ds6}}{g_{m5}}$.

EXERCISE SECTION 4: DIFFERENTIAL GAIN STAGES

4.1. A single-ended differential gain stage

10. A single-ended differential gain stage.

a) The OR (output range) is the possible swing at the output so that all transistors are operating in the saturation region.

$$V_{out,\,max} = V_{dd} - V_{sdsat4} = V_{dd} - \sqrt{\frac{I_{D4}}{\alpha_4}} = V_{dd} - \sqrt{\frac{I_{D5}}{2\alpha_4}} \tag{10.1}$$

$$V_{out,\,min} = V_{dssat5} + V_{dssat2} = \sqrt{\frac{I_{D5}}{\alpha_5}} + \sqrt{\frac{I_{D2}}{\alpha_2}} = \sqrt{\frac{I_{D5}}{\alpha_5}} + \sqrt{\frac{I_{D5}}{2\alpha_2}} \tag{10.2}$$

The output range is also dependent on the input voltage which results that

$$V_{out,\,min} = V_{in} - V_{gs2} + V_{ds2} = V_{in} - V_{T2} \tag{10.3}$$

which results in a minimum output voltage for all transistors operating in the saturation region equal to

$$V_{out,\,min} = max\left\{\sqrt{\frac{I_{D5}}{\alpha_5}} + \sqrt{\frac{I_{D5}}{2\alpha_2}},\, V_{in} - V_{T2}\right\} \tag{10.4}$$

The common-mode range is the possible input swing.

$$V_{in,\,min} = V_{dssat5} + V_{gs1} = \sqrt{\frac{I_{D5}}{\alpha_5}} + \sqrt{\frac{I_{D5}}{2\alpha_1}} + V_{T1} \tag{10.5}$$

$$V_{in,\,max} = V_{DD} - V_{gs3} - V_{dssat1} + V_{gs1} = V_{DD} - \sqrt{\frac{I_{D3}}{\alpha_3}} - V_{T3} + V_{T1} = V_{DD} - \sqrt{\frac{I_{D5}}{2\alpha_3}} - V_{T3} + V_{T1} \tag{10.6}$$

The ESSS of the differential gain stage is shown in Figure 43.

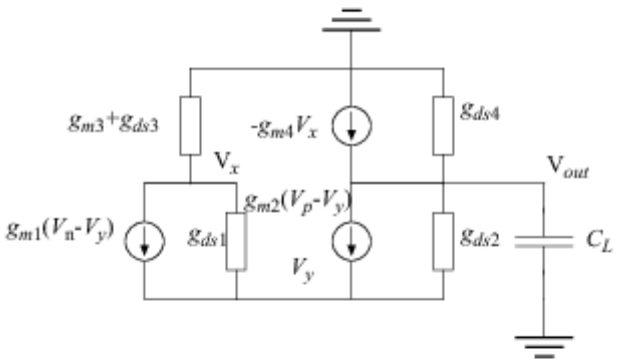


Figure 43: The ESSS of a single-ended differential gain stage.

It is assumed that transistors M_1 and M_2 are equally sized, as well as transistors M_3 and M_4. If the currents in both branches of the differential gain stage are equal, then $g_{m1} \approx g_{m2}$, $g_{ds1} \approx g_{ds2}$, $g_{m3} \approx g_{m4}$, and $g_{ds3} \approx g_{ds4}$. The following expressions hold for the circuit in Figure 43:

$$(g_{m3}+g_{ds3})V_x+g_{m1}(V_n-V_y)+g_{ds1}(V_x-V_y)=0\ , \tag{10.7}$$

$$g_{m1}(V_n-V_y)+g_{ds1}(V_x-V_y)+g_{m1}(V_p-V_y)+g_{ds1}(V_{out}-V_y)=0\ , \tag{10.8}$$

and

$$g_{m1}(V_p-V_y)+g_{ds1}(V_{out}-V_y)+g_{m3}V_x+V_{out}(sC_L+g_{ds3})=0\ . \tag{10.9}$$

Solving for V_{out} yields

$$V_{out}=\frac{(g_{ds3}+2g_{m3})g_{m1}(V_p-V_n)}{2(g_{ds1}+g_{ds3})(g_{ds3}+g_{m3})+sC_L(g_{ds1}+2(g_{ds3}+g_{m3}))}. \tag{10.10}$$

Assuming that $g_{m3}\gg g_{ds3}, g_{ds1}$ and dividing both the numerator and denominator of Eq. (10.10) with $2g_{m3}$ yields

$$V_{out}\approx\frac{g_{m1}(V_p-V_n)}{g_{ds1}+g_{ds3}+sC_L} \tag{10.11}$$

To compute the output resistance, r_{out}, we connect an AC voltage source, V_{out}, to the output node and set $V_p=V_n=0$ (and, of course, neglect C_L). The current delivered by V_{out} is denoted I_{out}. The following equations hold:

$$I_{out}-g_{m3}V_x-g_{ds3}V_{out}+g_{m1}V_y-g_{ds1}(V_{out}-V_y)=0\ , \tag{10.12}$$

$$-2g_{m1}V_y+g_{ds1}(V_x-2V_y+V_{out})=0\ , \tag{10.13}$$

and

$$-g_{m1}V_y+g_{ds1}(V_x-V_y)+(g_{m3}+g_{ds})V_x=0\ . \tag{10.14}$$

Solving for I_{out} yields

$$I_{out}=\frac{2(g_{ds1}+g_{ds3})(g_{ds3}+g_{m3})}{g_{ds1}+2(g_{ds3}+g_{m3})}V_{out}\approx(g_{ds1}+g_{ds3})V_{out}\ , \tag{10.15}$$

under the assumption that $g_{ds1}\ll 2(g_{m3}+g_{ds3})$. Hence, the output resistance is

$$r_{out}=\frac{V_{out}}{I_{out}}\approx\frac{1}{g_{ds1}+g_{ds3}} \tag{10.16}$$

and the output impedance is

$$z_{out}\approx\frac{1}{g_{ds1}+g_{ds3}+sC_L}. \tag{10.17}$$

b) The maximum current that can be delivered to the load capacitor is I_{bias}. Hence,

$$SR\approx\frac{I_{bias}}{C_L}. \tag{10.18}$$

4.2. Differential stage with passive load

11. Differential stage with passive load.

Here we would like to derive the differential and common-mode gain. The small-signal schemes are a little bit different.

a) The circuit is fully differential and thereby it is sufficient to compute the differential gain for half the circuit shown in Figure 44a. The differential gain is then

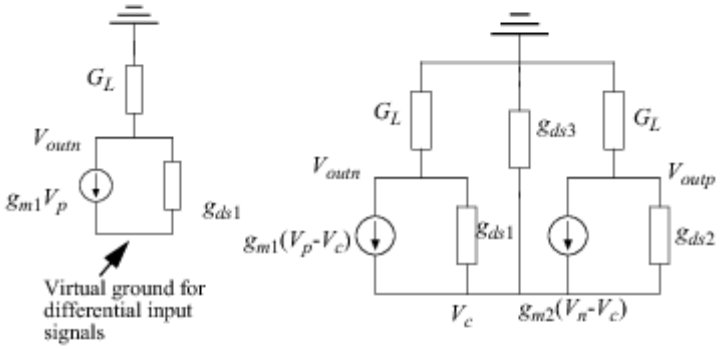


Figure 44: The ESSS of a differential gain stage for computing a) the differential gain (half circuit) and b) the gain from the common-mode input to the common-mode output voltage.

$$A_{diff} = \frac{V_{outp} - V_{outn}}{V_p - V_n} = -\frac{V_{outn}}{V_p} = \frac{g_{m1}}{g_{ds1} + G_L} \tag{11.1}$$

The second equality comes from the fact that $V_{outp} = -V_{outn}$ and $V_p = -V_n$ and we have a fully differential gain stage. Nearly the same computation as in Exercise 10.

b) The gain from the common-mode input voltage to the common-mode output voltage is computed using nodal analysis in the ESSS shown in Figure 44b. The nodal analysis is performed in nodes V_{outn}, V_{outp} and gnd.

$$V_{outn}G_L + (V_{outn} - V_c)g_{ds1} + g_{m1}(V_p - V_c) = 0 \tag{11.2}$$

$$V_{outp}G_L + (V_{outp} - V_c)g_{ds2} + g_{m2}(V_n - V_c) = 0 \tag{11.3}$$

$$V_{outn}G_L + V_{outp}G_L + V_c g_{ds3} = 0 \tag{11.4}$$

Solving for V_c in Eq. (11.4) gives

$$V_c = -\frac{G_L}{g_{ds3}}(V_{outp} + V_{outn}) \tag{11.5}$$

Adding the Eq. (11.2) and Eq. (11.3) gives

$$\begin{aligned}(V_{outp} + V_{outn})G_L + V_{outp}g_{ds2} + V_{outn}g_{ds1} + V_p g_{m1} + V_n g_{m2} = \\ (g_{ds1} + g_{ds2} + g_{m1} + g_{m2})V_c\end{aligned} \tag{11.6}$$

The design is fully symmetrical (i.e. transistor M_1 is equal to M_2 yielding the same transconductances, g_m, and output conductances, g_{ds}). The Eq. (11.6) is then simplified to

$$(V_{outp} + V_{outn})(g_{ds} + G_L) + (V_p + V_n)g_m = 2(g_{ds} + g_m)V_c \tag{11.7}$$

Combining Eq. (11.5) and Eq. (11.7) gives the gain

$$A_{cm,cm} = \frac{\frac{V_{outp}+V_{outn}}{2}}{\frac{V_p+V_n}{2}} = -\frac{g_{ds3}g_m}{g_{ds3}(g_{ds}+G_L)+2G_L(g_{ds}+g_m)} \tag{11.8}$$

c) The power supply rejection ration (PSRR) from the negative supply is defined as

$$PSRR_n = A_{diff}/\left(\frac{(V_{outp}-V_{outn})/2}{V_{gnd}}\right) \tag{11.9}$$

The differential gain is already computed so it is just the differential output variations due to a noisy ground line that is of interest. The small-signal model is shown in Figure 45. The small-

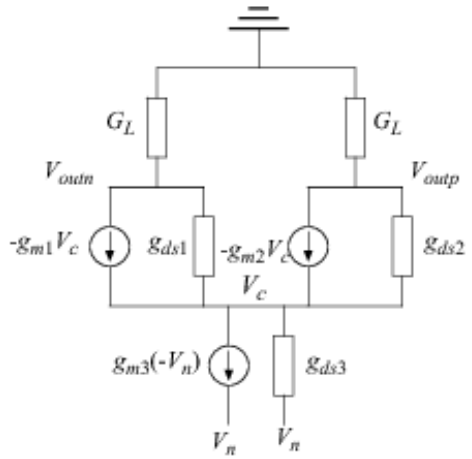


Figure 45: The ESSS for computing the negative power supply noise gain to the differential output.

signal source is V_n. Nodal analysis in nodes V_n, V_p, and V_c gives the following equations.

$$V_{outn}G_L + (V_{outn}-V_c)g_{ds1} + g_{m1}(-V_c) = 0 \tag{11.10}$$

$$V_{outp}G_L + (V_{outp}-V_c)g_{ds2} + g_{m2}(-V_c) = 0 \tag{11.11}$$

$$-V_c g_{m1} - V_c g_{m2} + (V_{outn}-V_c)g_{ds1} + (V_{outp}-V_c)g_{ds2} + (V_n-V_c)g_{ds3} + V_n g_{m3} = 0$$

We take the difference between Eq. (11.10) and Eq. (11.11) and assuming that transistor M_1 is matched to M_2.

$$(V_{outn}-V_{outp})(G_L+g_{ds}) = 0 \tag{11.12}$$

This yields that the gain from the negative supply to the differential output is zero and thereby the negative PSRR is infinite

4.3. Differential signals

In one of the branches we will have

$$V_{out,p} = A_0 + A_1 \cdot V_{in,p} + A_2 \cdot V_{in,p}^2 + A_3 \cdot V_{in,p}^3 \quad (20)$$

and on the other

$$V_{out,n} = A_0 + A_1 \cdot V_{in,n} + A_2 \cdot V_{in,n}^2 + A_3 \cdot V_{in,n}^3 \quad (21)$$

This gives us the differential output as

$$V_{out} = V_{out,p} - V_{out,n} = A_1 \cdot \left(V_{in,p} - V_{in,n}\right) + A_2 \cdot \left(V_{in,p}^2 - V_{in,n}^2\right) + A_3 \cdot \left(V_{in,p}^3 - V_{in,n}^3\right) \quad (22)$$

If now, $V_{in,p} = -V_{in,n}$, we get

$$V_{out} = 2A_1 \cdot V_{in,p} + 2A_3 \cdot V_{in,p}^3 \quad (23)$$

Since the second-order terms disappear, the linearity is also improved.

What about noise? Assume we have noise added to the outputs

$$V_{out,p} = A_0 + A_1 \cdot V_{in,p} + A_2 \cdot V_{in,p}^2 + A_3 \cdot V_{in,p}^3 + v_{n,p} \quad (24)$$

and on the other

$$V_{out,n} = A_0 + A_1 \cdot V_{in,n} + A_2 \cdot V_{in,n}^2 + A_3 \cdot V_{in,n}^3 + v_{n,n} \quad (25)$$

This gives us the differential output as

$$V_{out} = 2A_1 \cdot V_{in,p} + 2A_3 \cdot V_{in,p}^3 + v_{n,p} - v_{n,n} \quad (26)$$

For the noise ananlysis, we can neglect the effect of distortion.

$$V_{out} = 2A_1 \cdot V_{in,p} + \left(v_{n,p} - v_{n,n}\right) \quad (27)$$

The output power can be found by taking the expectation value of the square.

$$P_{out} = E\left(V_{out}^2\right) = E\left(\left(2A_1 \cdot V_{in,p} + \left(v_{n,p} - v_{n,n}\right)\right)^2\right) = E\left(\left(2A_1 \cdot V_{in,p}\right)^2\right) + E\left(\left(v_{n,p} - v_{n,n}\right)^2\right) \quad (28)$$

The first part is the signal power and the second part the noise power. The noise is uncorrelated, and the power of the signal is given by the amplitude.

$$P_s = E\left(\left(2A_1 \cdot V_{in,p}\right)^2\right) = 4A_1^2 V_{pp} \text{ and } P_n = E\left(\left(v_{n,p} - v_{n,n}\right)^2\right) = E\left(v_{n,p}^2\right) + E\left(v_{n,n}^2\right) = 2P'_n \quad (29)$$

The signal-to-noise ratio becomes

$$SNR_d = \frac{P_s}{P_n} = \frac{4\,A_1^2 V_{pp}}{2\,P'_n} \tag{30}$$

which can be compared to the single branch

$$SNR_s = \frac{P_s}{P_n} = \frac{A_1^2 V_{pp}}{P'_n} = \frac{SNR_d}{2} \tag{31}$$

EXERCISE SECTION 5: OTAS AND OPS

5.1. OP and OTA

An operational amplifier (OP) has ideally zero output impedance and is thus suitable for driving resistive loads, since in this way there is no voltage division between the output imepdance and the load resistance. Resistive loads are most often used off-chip, but also on chip in, e.g., active RC filters.

The operational transconducatance amplifier (OTA), however has ideally infinite output impedance, and os thus suitable for driving capacitive loads, as is often the case in "on-chip" situations, such as Gm-C filters or sample-and-hold circuits, or SC circuits.

5.2. Current mirror OTA

13. Current mirror OTA.

We start by some useful relations

$$g_m \approx 2\alpha V_{eff} \approx \sqrt{4\alpha I_D} = \sqrt{2\mu C_{ox}\frac{W}{L}I_D} \tag{13.1}$$

Which gives

$$W \approx \frac{g_m^2 L}{2\mu C_{ox} I_D} \tag{13.2}$$

Furthermore,

$$g_{ds} \approx \lambda I_D \tag{13.3}$$

The total power dissipation is

$$P_{diss} = V_{dd} I_{tot} = V_{dd} I_b \left(\frac{3}{2} + \frac{K}{2}\right) \tag{13.4}$$

Where K is the current-mirror gain. Solving for I_b gives

$$I_b = \frac{2}{3+K}\frac{P_{diss}}{V_{dd}} \tag{13.5}$$

From Johns&Martin (pages 273 -)

$$SR = \frac{KI_b}{C_L} = 2\frac{P_{diss}}{C_L V_{dd}}\frac{K}{3+K} \tag{13.6}$$

$$\omega_u \approx \frac{Kg_{m1}}{C_L} \Rightarrow g_{m1} \approx \frac{C_L}{K}\omega_u \tag{13.7}$$

$$A_0 = Kg_{m1} r_{out} \Rightarrow r_{out} = \frac{A_0}{Kg_{m1}} \tag{13.8}$$

Solution:

We start with the slew-rate specification to determine the K value. Solving for K in Eq. (13.6) gives

$$K = \frac{3SR}{\frac{2P_{diss}}{V_{dd}C_L} - SR} \approx 2{,}36 \tag{13.9}$$

When K is chosen we get $I_b \approx 170\mu A$ and we determine W_1 by combining Eq. (13.7) and Eq. (13.2) yielding

$$W_1 = \frac{C_L^2\omega_u^2 L}{2\mu K^2 C_{ox} I_{D1}} = \frac{C_L^2\omega_u^2 L}{K^2\mu C_{ox} I_b} \approx 58\mu m \tag{13.10}$$

From Eq. (13.8) we get the required output resistance $r_{out} \approx 3{,}18\mathrm{M}\Omega$.

The output stage is a common-source amplifier with cascodes like the one in the Ex. 9. The output conductance is given by the parallel combination of the nmos and pmos resistances. Here we have chosen the size of the output resistances of the nmos and pmos transistors equal to $r_p = r_n = 2r_{out}$. The pmos resistance is given by

$$r_p = \frac{1}{g_{ds8}}\frac{g_{m10}}{g_{ds10}} = \frac{g_{mp}}{g_{dsp}^2} \Rightarrow g_{mp} = r_p g_{dsp}^2 \tag{13.11}$$

Similarly

$$r_n = \frac{1}{g_{ds14}}\frac{g_{m12}}{g_{ds12}} = \frac{g_{mn}}{g_{dsn}^2} \Rightarrow g_{mn} = r_n g_{dsn}^2 \tag{13.12}$$

Here we have assumed that the size of transistors M_8 is equal to M_{10} and M_{12} is equal to M_{14} and thereby they will have the same small-signal parameters.

The DC current through the output stage is given by $I_D = I_b K/2$ and we know that $g_{ds} = \lambda I_D$. These two expression together with Eq. (13.11) and Eq. (13.12) gives

$$g_{mp} = 2r_{out}(\lambda_p I_b K/2)^2 \approx 1{,}5mS \tag{13.13}$$

$$g_{mn} = 2r_{out}(\lambda_n I_b K/2)^2 \approx 0{,}544\mu S \tag{13.14}$$

Solving for the widths by using Eq. (13.1) gives

$$W_8 = W_{10} = \frac{g_{mp}^2 L}{2\mu_p C_{ox} I_D} \approx 113\mu m \tag{13.15}$$

$$W_{12} = W_{14} = \frac{g_{mn}^2 L}{2\mu_n C_{ox} I_D} \approx 4{,}8\mu m \tag{13.16}$$

$$W_3 = W_4 = W_5 = W_6 = W_7 = W_9 = \frac{W_8}{K} \approx 48\mu m \tag{13.17}$$

$$W_{11} = W_{13} = \frac{W_{12}}{K} \approx 2\mu m \tag{13.18}$$

5.3. A simplified model of a two-stage operational transconductance amplifier

14. A simplified model of a two-stage operational transconductance amplifier.

a) A compensation circuit can for example consist of a capacitor, or a capacitor and a resistor. For a useful compensation circuit there can not be a DC path between the nodes of the compensation circuit. We use the approximation $g_m \gg g_{ds}$ and assume that M_1 and M_2 are equally sized, and that M_3 and M_4 are equally sized. Further, the bulk effect is neglected.

$$g_I = g_{ds2} + g_{ds4} \tag{14.1}$$

$$g_{II} = g_{ds6} + g_{ds7} \tag{14.2}$$

$$g_{mI} = g_{m1} = g_{m2} \tag{14.3}$$

$$g_{mII} = g_{m7} \tag{14.4}$$

$$C_I = C_{gs7} + C_{ds4} + C_{db4} + C_{ds2} + C_{db2} + C_{gb7} \tag{14.5}$$

$$C_{II} = C_L + C_{ds7} + C_{db7} + C_{ds6} + C_{db6} \tag{14.6}$$

b) The small-signal properties are calculated using nodal analysis in the nodes V_x and V_{out}.

$$g_{mI}V_{in} + V_x(g_I + sC_I) + (V_x - V_{out})sC_c = 0 \tag{14.7}$$

$$g_{mII}V_x + V_{out}(g_{II} + sC_{II}) + (V_{out} - V_x)sC_c = 0 \tag{14.8}$$

Solving for V_x in Eq. (14.8) and inserting it into Eq. (14.7) gives

$$\frac{V_{out}}{V_{in}} = \frac{g_{mI}(g_{mII} - sC_c)}{g_I g_{II} + s((C_{II} + C_c)g_I + (C_I + C_c)g_{II} + C_c g_{mII}) + s^2(C_I C_{II} + C_c(C_I + C_{II}))}$$

We simplify the expression above by assuming that $g_{mII} \gg g_I, g_{II}$ and $C_c, C_{II} \gg C_I$, yielding

$$\frac{V_{out}}{V_{in}} \approx \frac{g_{mI}(g_{mII} - sC_c)}{g_I g_{II} + sC_c g_{mII} + s^2 C_c C_{II}} \tag{14.9}$$

Eq. (14.9) can be used to get the DC gain, poles and zero.

$$A_0 = \frac{g_{mI}}{g_I}\frac{g_{mII}}{g_{II}} \tag{14.10}$$

$$p_1 \approx \frac{g_I g_{II}}{g_{mII} C_c} \tag{14.11}$$

$$p_2 \approx \frac{g_I g_{II}}{C_c C_{II}}\frac{1}{p_1} = \frac{g_{mII}}{C_{II}} \tag{14.12}$$

$$z_1 = -\frac{g_{mII}}{C_c} \tag{14.13}$$

The zero is located in the right half plane (RHP).

The unity-gain frequency is approximately given by the expression $\omega_u \approx A_0 p_1$ if the poles are well separated.

$$\omega_u \approx \frac{g_{m1}}{g_I}\frac{g_{mII}}{g_{II}}\frac{g_I g_{II}}{g_{mII} C_c} = \frac{g_{m1}}{C_c} \tag{14.14}$$

Q.E.D.

c, d, and e) Recall that $g_m \propto \sqrt{W(I_D/L)}$ and $g_{ds} \propto I_D/L$. The DC gain, unity-gain frequency and the first pole can be expressed as

$$A_0 = \frac{g_{m2}g_{m7}}{(g_{ds2}+g_{ds4})(g_{ds6}+g_{ds7})} \propto \frac{\sqrt{\frac{W_2}{2L_2}I_{D5}}\sqrt{\frac{W_7}{L_7}I_{D6}}}{\left(\frac{1}{L_2}+\frac{1}{L_4}\right)\frac{I_{D5}}{2}\left(\frac{1}{L_6}+\frac{1}{L_7}\right)I_{D6}} = \frac{L_4\sqrt{2W_2L_2}}{(L_2+L_4)\sqrt{I_{D5}}}\frac{L_6\sqrt{W_7L_7}}{(L_6+L_7)\sqrt{I_{D6}}} \tag{14.15}$$

$$\omega_u \approx \frac{g_{m1}}{C_c} \propto \sqrt{\frac{W_2}{2L_2}I_{D5}} \tag{14.16}$$

$$p_1 \approx \frac{(g_{ds2}+g_{ds4})(g_{ds6}+g_{ds7})}{g_{m7}C_c} \propto \frac{\left(\frac{1}{L_2}+\frac{1}{L_4}\right)\frac{I_{D5}}{2}\left(\frac{1}{L_6}+\frac{1}{L_7}\right)\frac{I_{D6}}{2}}{\sqrt{\frac{W_7}{L_7}I_{D6}}C_c} = \frac{1}{4}\left(\frac{1}{L_2}+\frac{1}{L_4}\right)\frac{(L_6+L_7)}{L_6\sqrt{W_7L_7}}I_{D5}\sqrt{I_{D6}} \tag{14.17, 14.18}$$

	DC gain	**unity-gain frequency**	**bandwidth**
W_2 **increased**	Increased	Increased	-
I_{bias} **increased**	Decreased	Increased	Increased
W_4 **increased**	-	-	-

5.4. A two-stage OTA without compensation circuit

15. A two-stage OTA without compensation circuit.

The ESSS of the two-stage amplifier is shown in Figure 46. The following assumption has been

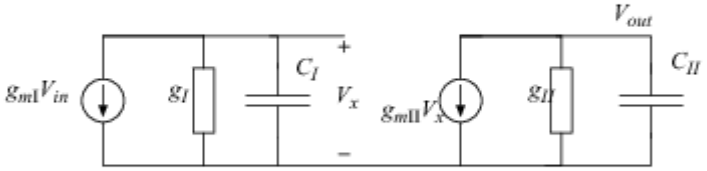


Figure 46: The ESSS of an ordinary two-stage amplifier with no compensation.

used, $g_m \gg g_{ds}$ and no bulk effect.

Since there is no connection between the first stage and the second stage, i.e. no component between the node V_x and V_{out}, the transfer function can be computed directly by the following expression

$$A(s) = \frac{V_{out}}{V_{in}} = \frac{V_{out}}{V_x}\frac{V_x}{V_{in}} = \frac{g_{mII}}{g_{II}+sC_{II}}\frac{g_{mI}}{g_I+sC_I} \tag{15.1}$$

where $g_{mII} = g_{m7}$, $g_{mI} = g_{m1} = g_{m2}$, $g_{II} = g_{ds6}+g_{ds7}$, $g_I = g_{ds2}+g_{ds4}$, $C_I = C_{gs7}$, and $C_{II} = C_L$.

The DC gain is

$$A_0 = \frac{g_{m2}g_{m7}}{(g_{ds2}+g_{ds4})(g_{ds6}+g_{ds7})} \propto \frac{L_4\sqrt{2W_2L_2}}{(L_2+L_4)\sqrt{I_{D5}}}\frac{L_6\sqrt{W_7L_7}}{(L_6+L_7)\sqrt{I_{D6}}} \tag{15.2}$$

which gives that

$$A_0 \propto \frac{1}{\sqrt{I_{D5}I_{D6}}} \tag{15.3}$$

b) The dominant pole is located at

$$p_1 = \frac{g_{ds6}+g_{ds7}}{C_L} \tag{15.4}$$

if the load capacitor is assumed to be much larger than the capacitive parasitics. The non dominant pole is located at

$$p_2 = \frac{g_{ds2}+g_{ds4}}{C_{gs7}} \tag{15.5}$$

c) The unity-gain frequency

$$\omega_u \approx A_0 p_1 = \frac{g_{m2}g_{m7}}{(g_{ds2}+g_{ds4})C_L} \tag{15.6}$$

The phase margin is defined as $\phi_m = \pi + \arg A(j\omega_u)$.

$$\phi_m = \pi - \operatorname{atan}\frac{\omega_u}{p_1} - \operatorname{atan}\frac{\omega_u}{p_2} \tag{15.7}$$

d) An ideal operational amplifier has zero output impedance. To decrease the output impedance we have to compute the output resistance of the amplifier. Adding a voltage source at the output and calculating the current delivered by the source according to the following

$$I_{out} = V_{out}(g_{ds6} + g_{ds7}) \tag{15.8}$$

The output resistance is, thus,

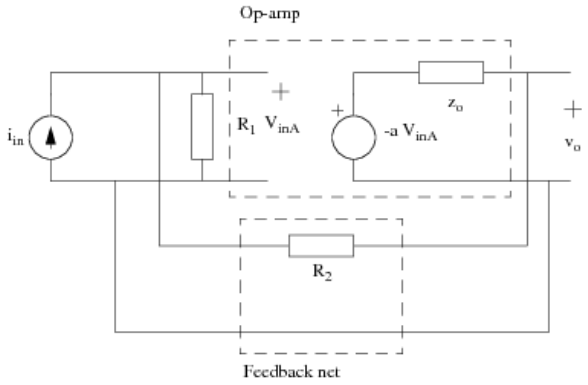
$$r_{out} = \frac{V_{out}}{I_{out}} = \frac{1}{g_{ds6} + g_{ds7}} \approx \frac{1}{\left(\frac{1}{L_6} + \frac{1}{L_7}\right) I_{D6}} \tag{15.9}$$

The output resistance is decreased if the current through the output stage is increased. Another way to decrease the output resistance is to add a buffer stage, for example a common-drain amplifier, at the output of the circuit.

5.5. Feedback modes (K2)

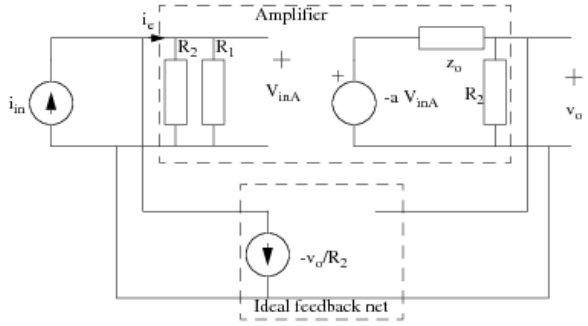
Exercise K2

a) Small-signal model



It is seen in the figure that the feedback net is connected in parallel with the amplifier at both the input and the output. The type of feedback is thus shunt-shunt which means that the input and output impedance of the amplifier will be divided by (1+T) where T is the loop-gain.

Replace the feedback net with y-parameter representation:

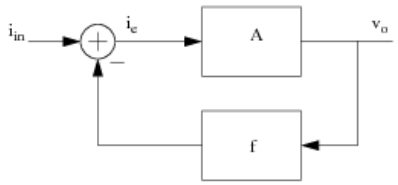


The upper circuit can be interpreted as an amplifier with:

$$z_{inA} = R_1 \| R_2,\ z_{outA} = z_o \| R_2 \text{ and } A = \frac{R_2}{R_2 + z_o}(-a)(R_1 \| R_2)$$

where $v_o = A i_\epsilon$.

The system level model for the circuit above is shown below



The loop gain is determined by:

$$T = Af = \frac{R_2}{R_2 + z_o}(-a)(R_1 \| R_2) \cdot \left(-\frac{1}{R_2}\right)$$

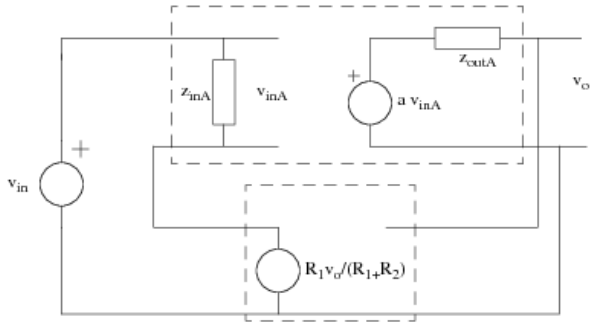
The input and output impedance of the feedback system is given by:

$$z_{in} = \frac{z_{inA}}{1+T} = \frac{R_1 \| R_2}{1+T},\ z_{out} = \frac{z_{outA}}{1+T} = \frac{R_2 \| z_o}{1+T}$$

The transfer function is given by:

$$\frac{v_o}{i_e} = \frac{A}{1+Af} = \frac{1}{1/A + f} \approx \frac{1}{f} = -R_2$$

b) By replacing the feedback net with its h-parameter representation (see 1b)) the following small-signal model can be used:



where $z_{inA} = \infty$, $z_{outA} = z_o \| (R_1 + R_2)$, $A = \frac{R_1 + R_2}{R_1 + R_2 + z_o} a$ and $v_o = A v_{inA}$.

The loop gain is given by $T = Af = \left(\frac{R_1 + R_2}{R_1 + R_2 + z_o} a\right) \frac{R_2}{R_1 + R_2}$

The type of feedback is series-shunt and therefore the total input and output impedance are given by

$$z_{in} = z_{inA}(1+T) = \infty \text{ and } \frac{z_{outA}}{1+T} = \frac{z_o \| (R_1 + R_2)}{1+T}$$

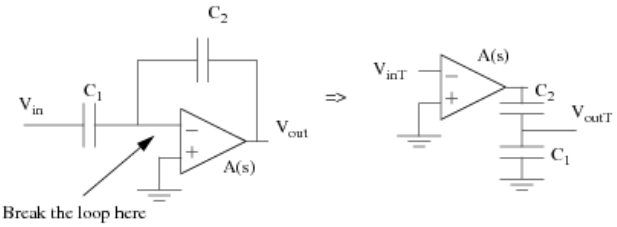
The transfer function is given by

$$\frac{v_o}{v_{in}} = \frac{A}{1+Af} \approx \frac{1}{f} = \frac{R_1+R_2}{R_2}$$

5.6. Feedback factor (K4)

Exercise K4

Calculated the loop gain: Break the feedback loop



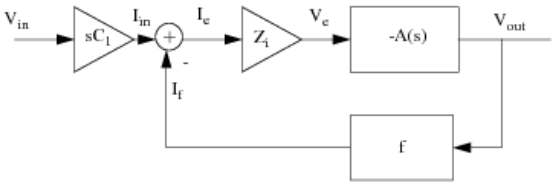
Loop gain:

$$T(s) = A(s)\frac{1/(sC_1)}{1/(sC_1)+1/(sC_2)} = \frac{C_2}{C_1+C_2}A(s) = \beta A(s)$$

The feedback factor:

$$\beta = \frac{C_2}{C_1+C_2}$$

The closed loop system can be modelled as below (see lesson 1)



where $f = -sC_2$ and $Z_i = \frac{1}{sC_1+sC_2}$.

The closed loop transfer function is thus given by

$$A_{CL}(s) = \frac{V_{out}}{V_{in}} = sC_1\frac{Z_i(-A(s))}{1+Z_i(-A(s))f} = sC_1\frac{Z_i}{\frac{1}{-A(s)}+Z_if} \approx \frac{sC_1}{f} = -\frac{C_1}{C_2}$$

The loop gain calculated from the system model:

$$T(s) = Z_i(-A(s))f = \frac{1}{sC_1+sC_2}(-sC_2)(-A(s)) = \frac{C_2}{C_1+C_2}A(s) \Rightarrow \beta = \frac{C_2}{C_1+C_2}$$

Conclusion: When calculating the loop gain we can break the loop to directly get the loop gain and feedback factor β, but the total transfer function is **not** given by $1/\beta$ when using shunt-shunt feedback.

5.7. Compensation of a two-stage OTA

16. Compensation of a two-stage OTA.

a) The resistor value can be choose so that the compensation zero is located at infinity, nulling resistor. The other way is to use the lead compensation method where the zero is placed slightly higher in frequency than the unity-gain frequency.

b) Starting with the *Miller capacitor* compensation:

The simplified ESSS is shown in Figure 47. The transfer function is calculated using nodal anal-

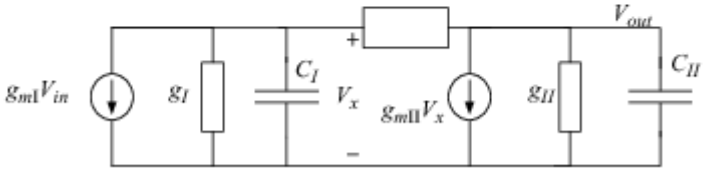


Figure 47: The ESSS of an ordinary two-stage amplifier with compensation.

ysis in the nodes V_x and V_{out}.

$$g_{m1}V_{in} + V_x(g_I + sC_I) + (V_x - V_{out})sC_c = 0 \tag{16.1}$$

$$g_{mII}V_x + V_{out}(g_{II} + sC_{II}) + (V_{out} - V_x)sC_c = 0 \tag{16.2}$$

Solving for V_x in Eq. (16.2) and inserting it into Eq. (16.1) gives

$$\frac{V_{out}}{V_{in}} = \frac{g_{mI}(g_{mII} - sC_c)}{g_I g_{II} + s((C_{II} + C_c)g_I + (C_I + C_c)g_{II} + C_c g_{mII}) + s^2(C_I C_{II} + C_c(C_I + C_{II}))}$$

Some simplification can be in place. $g_m \gg g$, $C_c \gg C_I$, $C_c \approx C_{II}$.

$$\frac{V_{out}}{V_{in}} \approx \frac{g_{mI}(g_{mII} - sC_c)}{g_I g_{II} + sC_c g_{mII} + s^2 C_c C_{II}} \tag{16.3}$$

The above equation can be used to get the DC gain, poles and zero.

$$A_0 = \frac{g_{mI}}{g_I}\frac{g_{mII}}{g_{II}} \tag{16.4}$$

$$p_1 \approx \frac{g_I g_{II}}{g_{mII} C_c} \tag{16.5}$$

$$p_2 \approx \frac{g_I g_{II}}{C_c C_{II}}\frac{1}{p_1} = \frac{g_{mII}}{C_{II}} \tag{16.6}$$

$$z_1 = \frac{g_{mII}}{C_c} \tag{16.7}$$

The zero is located in the right hand plane (RHP).

The unity-gain frequency is approximately give by the expression $\omega_u \approx A_0 p_1$ if the poles are well separated.

$$\omega_u \approx \frac{g_{mI}}{g_I}\frac{g_{mII}}{g_{II}}\frac{g_I g_{II}}{g_{mII} C_c} = \frac{g_{mI}}{C_c} \tag{16.8}$$

The *resistor and capacitor (lead) compensation* is shown in Figure 48. Nodal analysis in the

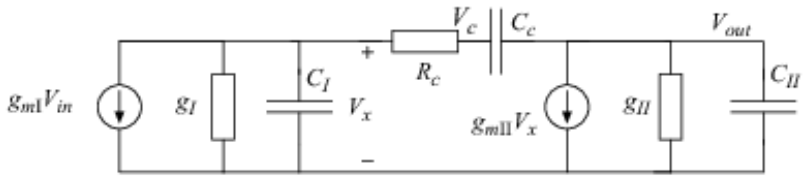


Figure 48: The ESSS of a two-stage amplifier compensated with a resistor and a capacitor.

nodes V_x, V_c and V_{out} gives the following equations.

$$g_{mI}V_{in} + V_x(g_I + sC_I) + (V_x - V_c)G_c = 0 \tag{16.9}$$

$$(V_x - V_c)G_c + (V_{out} - V_c)sC_c = 0 \tag{16.10}$$

$$g_{mII}V_x + V_{out}(g_{II} + sC_{II}) + (V_{out} - V_c)sC_c = 0 \tag{16.11}$$

Solving this system of equations gives

$$\frac{V_{out}}{V_{in}} = \frac{g_{mI}(G_c g_{mII} + C_c(-G_c + g_{mII}))s}{a + bs + cs^2 + ds^3} \tag{16.12}$$

where

$$a = g_I g_{II} G_c \tag{16.13}$$

$$b = (C_{II}g_I + C_I g_{II})G_c + C_c(g_I g_{II} + G_c(g_I + g_{II} + g_{mII})) \tag{16.14}$$

$$c = C_I C_{II} G_c + C_c(C_{II}g_I + C_I g_{II} + (C_I + C_{II})G_c) \tag{16.15}$$

$$d = C_I C_{II} C_c \tag{16.16}$$

The above expressions can be simplified by $C_I \ll C_{II}$, $C_I \ll C_c$, $g \ll g_m$, and $g \ll G_c$

$$b \approx C_{II}g_I G_c + C_c G_c g_{mII} \tag{16.17}$$

$$c \approx C_c C_{II} G_c \tag{16.18}$$

The DC gain is

$$A_0 = \frac{g_{mI}g_{mII}G_c}{g_I g_{II} G_c} = \frac{g_{mI}g_{mII}}{g_I g_{II}} \tag{16.19}$$

The first pole is well separated from the other ones.

$$p_1 \approx \frac{a}{b} \approx \frac{g_I g_{II} G_c}{C_{II}g_I G_c + C_c G_c g_{mII}} = \frac{g_I g_{II}}{C_{II}g_I + C_c g_{mII}} \approx \frac{g_I g_{II}}{C_c g_{mII}} \tag{16.20}$$

The zero is located at

$$z_1 = \frac{G_c g_{mII}}{C_c(-G_c + g_{mII})} = -\frac{1}{C_c\left(\frac{1}{g_{mII}} - \frac{1}{G_c}\right)} \tag{16.21}$$

The unity-gain frequency is

$$\omega_u \approx A_0 p_1 \approx \frac{g_{mI}}{C_c} \tag{16.22}$$

When the compensation circuit is inserted the first pole will decrease in frequency at the same time as the DC gain is not changed. This will result in a decreased unity-gain frequency and a more stable amplifier.

c) To increase the phase margin of the system we need to place the compensation zero of the circuit at a frequency higher than the unity-gain frequency. $|z_1| > \omega_u$ gives

$$-\frac{1}{C_c\left(\frac{1}{g_{mII}} - \frac{1}{G_c}\right)} > \frac{g_{mI}}{C_c} \tag{16.23}$$

which can be rearranged according to

$$R_c > \frac{1}{g_{mI}} + \frac{1}{g_{mII}} \tag{16.24}$$

If $R_c > 1/g_{mII}$ then we will have a zero in the left hand plane.

5.8. A folded-cascode OTA

17. A folded-cascode OTA.

For symmetrical fully differential circuits with only a differential input signal, the node at the source of M_5 is small-signal ground. Further, the circuit is a fully differential gain stage and thereby it is sufficient to compute the small-signal transfer function of half the circuit.

The equivalent small-signal model is shown in Figure 49.

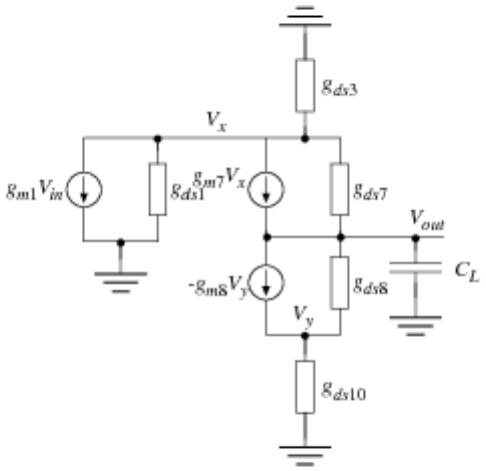


Figure 49: ESSS for the folded-cascode amplifier.

Performing nodal analysis in the nodes V_x, V_y, and V_{out} results in the following equations

$$\begin{aligned} g_{m1}V_{in} + V_x g_{ds1} + V_x g_{ds1} + g_{m7}V_x + (V_x - V_{out})g_{ds7} &= 0 \\ g_{m8}V_y + (V_y - V_{out})g_{ds8} + V_y g_{ds10} &= 0 \\ g_{m7}V_x + (V_x - V_{out})g_{ds7} - V_{out}sC_L + g_{m8}V_y + (V_y - V_{out})g_{ds8} &= 0 \end{aligned} \tag{17.1}$$

Solving for V_{out} in the system of equations gives

$$\frac{V_{out}}{V_{in}} = \frac{-g_{m1}(g_{m7}+g_{ds7})(g_{m8}+g_{ds8}+g_{ds10})}{(g_{ds1}+g_{ds3})g_{ds7}(g_{m8}+g_{ds8}+g_{ds10}) + (g_{ds1}+g_{ds3}+g_{ds7}+g_{m7})(g_{ds8}+g_{ds10}) + sC_L} \tag{17.2}$$

dividing by the two expressions within the parenthesis in the numerator and assuming that $g_m \gg g_{ds}$ gives the following expression

$$\frac{V_{out}}{V_{in}} = \frac{-g_{m1}}{\dfrac{(g_{ds1}+g_{ds3})g_{ds7}}{g_{m7}} + \dfrac{g_{ds8}g_{ds10}}{g_{m8}} + sC_L} \tag{17.3}$$

The DC gain is extracted from Eq. (17.3).

$$A_0 = \frac{-g_{m1}}{\dfrac{(g_{ds1}+g_{ds3})g_{ds7}}{g_{m7}} + \dfrac{g_{ds8}g_{ds10}}{g_{m8}}} = \frac{-g_{m1}}{g_{out}} \tag{17.4}$$

and the first pole is given by

$$p_1 = \frac{g_{out}}{C_L} \tag{17.5}$$

b) The phase margin is increased if the ratio between the second pole and the unity-gain frequency is increased. The unity-gain frequency can be expressed as

$$\omega_u \approx A_0 p_1 \approx \frac{g_{m1}}{C_L} \approx \frac{\sqrt{2\mu_n C_{ox}\frac{W_1}{L_1} I_{diff}}}{C_L} \tag{17.6}$$

where I_{diff} is the current through transistor M_1. The second pole is given in the exercise to be

$$p_2 \approx \frac{g_{m7}}{C_x} \approx \frac{g_{m7}}{C_{gs7}} \approx \frac{\sqrt{2\mu_p C_{ox}\frac{W_7}{L_7} I_{casc}}}{\frac{2}{3}C_{ox}W_7L_7} = \frac{\sqrt{2\mu_p}}{\frac{2}{3}\sqrt{C_{ox}}}\frac{\sqrt{I_{casc}}}{L_7\sqrt{W_7L_7}} \tag{17.7}$$

where I_{casc} is the current through transistors M_7, M_8 and M_{10}. The expression for the ratio between the second pole and the unity-gain frequency is given by

$$\frac{p_2}{\omega_u} \approx \frac{\frac{\sqrt{2\mu_p}}{\frac{2}{3}\sqrt{C_{ox}}}\frac{\sqrt{I_{casc}}}{L_7\sqrt{W_7L_7}}}{\frac{\sqrt{2\mu_n C_{ox}\frac{W_1}{L_1} I_{diff}}}{C_L}} = \frac{3}{2}\sqrt{\frac{\mu_p}{\mu_n}}\frac{\sqrt{L_1}C_L}{C_{ox}L_7\sqrt{W_7L_7W_1}}\sqrt{\frac{I_{casc}}{I_{diff}}} \tag{17.8}$$

Further, the DC gain can be expressed as

$$\begin{aligned} A_0 &\approx \frac{-g_{m1}}{\frac{(g_{ds1}+g_{ds3})g_{ds7}}{g_{m7}} + \frac{g_{ds8}g_{ds10}}{g_{m8}}} \approx \\ &\frac{\sqrt{2\mu_n C_{ox}\frac{W_1}{L_1} I_{diff}}}{\frac{(\lambda_1 I_{diff} + \lambda_3(I_{diff}+I_{casc}))\lambda_7 I_{casc}}{\sqrt{2\mu_p C_{ox}\frac{W_7}{L_7} I_{casc}}} + \frac{\lambda_8\lambda_{10} I_{casc}^2}{\sqrt{2\mu_n C_{ox}\frac{W_8}{L_8} I_{casc}}}} \approx \\ &\sqrt{2\mu_n C_{ox}}\frac{\sqrt{\frac{W_1}{L_1} I_{diff}}}{\frac{\left(\frac{1}{L_1}I_{diff} + \frac{1}{L_3}(I_{diff}+I_{casc})\right)\sqrt{I_{casc}}}{\sqrt{W_7L_7}} + \frac{I_{casc}^{3/2}}{\sqrt{2\mu_n C_{ox}}\sqrt{W_8L_8}L_{10}}} \end{aligned} \tag{17.9}$$

From Eq. (17.8) and Eq. (17.9) the solution can be computed.

The phase margin can be increased if the area is limited by for example:

- Increasing I_{casc} the drawbacks will be higher power consumption and lower DC gain.

The phase margin can be increased if the power is critical by for example:

- Increasing C_L, the drawbacks is decreased slew rate and unity-gain frequency, but the DC gain will not be changed.
- Decrease W_7, the drawback is decreased DC gain, no changes to the unity-gain frequency or the slew rate.

The phase margin can be increased if the unity-gain frequency and the power consumption is critical for example by:

- Decrease W_7, the drawback is decreased DC gain, no changes to the unity-gain frequency or the slew rate.

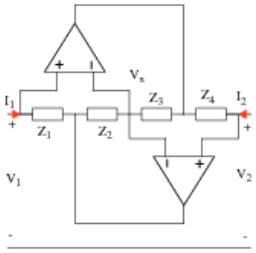
5.9. OP application (K9)

Exercises

Exercise K9

GIC - *Generalized impedance converter.*

The gic can be used to realize on-chip inductances. However, the circuit is area consuming and there are some other drawbacks.



Derive the K-matrix

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} V_2 \\ -I_2 \end{bmatrix}$$

where

$$A = \left.\frac{V_1}{V_2}\right|_{-I_2=0}, \; B = \left.\frac{V_1}{-I_2}\right|_{V_2=0}, \; C = \left.\frac{I_1}{V_2}\right|_{-I_2=0}, \; D = \left.\frac{I_1}{-I_2}\right|_{V_2=0}$$

(If N links with K-matrix K_i are cascaded, the total system can be described by the matrix product $K_{TOT} = K_1 K_2 \ldots K_N$.)

Assume that the OPamps are ideal. This implies that the voltage over the input must be zero. This forces the potential in V_x to be equal to V_1 **and** V_2, and further $V_1 = V_2$. With KCL, and denoting the currents through Z_2 and Z_3 with I_{Z2} and I_{Z3}, respectively, we have:

$$V_1 - I_1 Z_1 - I_{Z2} Z_2 = V_x = V_1 \text{ which gives } I_{Z2} = -I_1 Z_1 / Z_2$$
$$V_2 - I_2 Z_4 - I_{Z3} Z_3 = V_x = V_2 \text{ which gives } I_{Z3} = -I_2 Z_4 / Z_3$$

Due to the infinite input impedance, there can be no current flowing into the OPamps, and:

$$I_{Z2} = -I_{Z3} \text{ which gives } -I_1 Z_1 / Z_2 = I_2 Z_4 / Z_3, \text{ or } I_1 = -I_2 \frac{Z_2 Z_4}{Z_1 Z_3}$$

From this we get

$$A = 1, \; B = 0, \; C = 0, \; D = \frac{Z_2 Z_4}{Z_1 Z_3}$$

If an impedance, Z, is terminating port two, the relation between output current and voltage is given by

$$V_2 = -I_2 Z$$

Equations $V_1 = V_2$ and $I_1 = \frac{Z_2 Z_4}{Z_1 Z_3} \cdot \frac{V_2}{Z}$ give

$$Z_{in} = \frac{V_1}{I_1} = \frac{V_2}{\frac{Z_2 Z_4}{Z_1 Z_3} \cdot \frac{V_2}{Z}} = Z \frac{Z_1 Z_3}{Z_2 Z_4}$$

Suppose

$$Z = Z_1 = Z_3 = Z_2 = R \text{ and } Z_4 = \frac{1}{sC}$$

we have

$$Z_{in} = sCR^2 = sL$$

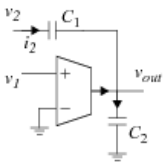
which simulates an inductor.

Exercise Extra

Find a signal flow chart which describes a 4th order leapfrog filter. Or generally, an even order leapfrog filter.

5.10. Gm-C application (K10)

Exercise K10



The equations for the circuit are given by

$$I_2 = sC_1 \cdot (V_2 - V_{out})$$

$$I_x = G_m \cdot V_1$$

$$I_2 + I_x = sC_2 \cdot V_{out}$$

$$V_{out} = \frac{1}{sC_2} \cdot (I_2 + I_x) = \frac{C_1}{C_2}(V_2 - V_{out}) + \frac{G_m}{sC_2} \cdot V_1$$

$$V_{out} = \frac{G_m}{s\alpha} V_1 + \frac{C_1}{\alpha} V_2 \text{ where } \alpha = C_1 + C_2$$

With this circuit we can perform an addition and an integration.

5.11. OP/OTA stability

a) Transfer function

The total transfer function is simply given by identification.

$$\frac{v_{out}}{v_{in}}=\frac{\frac{g_m}{G_I}\cdot\frac{g_m}{G_{II}}}{\left(1+\frac{s}{\frac{G_I}{C_I}}\right)\cdot\left(1+\frac{s}{\frac{G_{II}}{C_{II}}}\right)} \tag{32}$$

b) Well-separated pools

If the poles are well separated, splitted, then we know that either is $p_I \gg p_{II}$ or $p_{II} \gg p_I$, where the poles are identified from first (I) or second (II) stage.

The phase margin is given by

$$\varphi_m=90-atan\left(\frac{\omega_{ug}}{p_2}\right) \tag{33}$$

where p_2 is the dominant pole (either p_I or p_{II}) and $\omega_{ug}=A_0\,p_1$.

In the 45-degree phase margin case, the $p_2=\omega_{ug}$.

$$\omega_{ug}=A_0\cdot p_1=A_I\cdot A_{II}\cdot p_1=p_2\Rightarrow\frac{g_m^2}{G_I G_{II}}\cdot p_1=p_2 \tag{34}$$

which gives us two cases:

$$\frac{g_m^2}{G_I G_{II}}\cdot\frac{G_I}{C_I}=\frac{G_{II}}{C_{II}} \text{ and } \frac{g_m^2}{G_I G_{II}}\cdot\frac{G_{II}}{C_{II}}=\frac{G_I}{C_I} \tag{35}$$

which boils down to

$$\frac{g_m^2}{G_{II}^2}=\frac{C_I}{C_{II}} \text{ and } \frac{g_m^2}{G_I^2}=\frac{C_{II}}{C_I} \tag{36}$$

Further on,

$$\frac{g_m^2}{G_I G_{II}}=7200 \text{ and } \frac{g_m}{G_{II}}=8\frac{g_m}{G_I}\Rightarrow G_I=8\,G_{II} \tag{37}$$

Combining them

$$8\frac{g_m^2}{G_{II}G_I}=\frac{C_I}{C_{II}}\Rightarrow\frac{C_I}{C_{II}}=8\cdot 7200 \quad \text{and} \quad \frac{g_m^2}{8G_IG_{II}}=\frac{C_{II}}{C_I}\Rightarrow\frac{C_{II}}{C_I}=7200/8=900 \tag{38}$$

So either

$$C_{II}<\frac{C_I}{8\cdot 7200} \quad \text{or} \quad C_{II}>900\,C_I \tag{39}$$

EXERCISE SECTION 6: NOISE IN CMOS CIRCUITS

- If not stated otherwise, we use the process parameters given in Sec. (), the power supply voltage is $V_{DD}=3.3$ V, the transistor lengths are $L=1$ um.

- If not stated otherwise, the bulks of the NMOS and PMOS transistors are connected to ground and positive supply, respectively.

6.1. Noise in a multi-stage amplifier

18. Noise in a multi-stage amplifier.

a) In Figure 50(b) the small-signal equivalent for the circuit is shown. Further, the gain for each

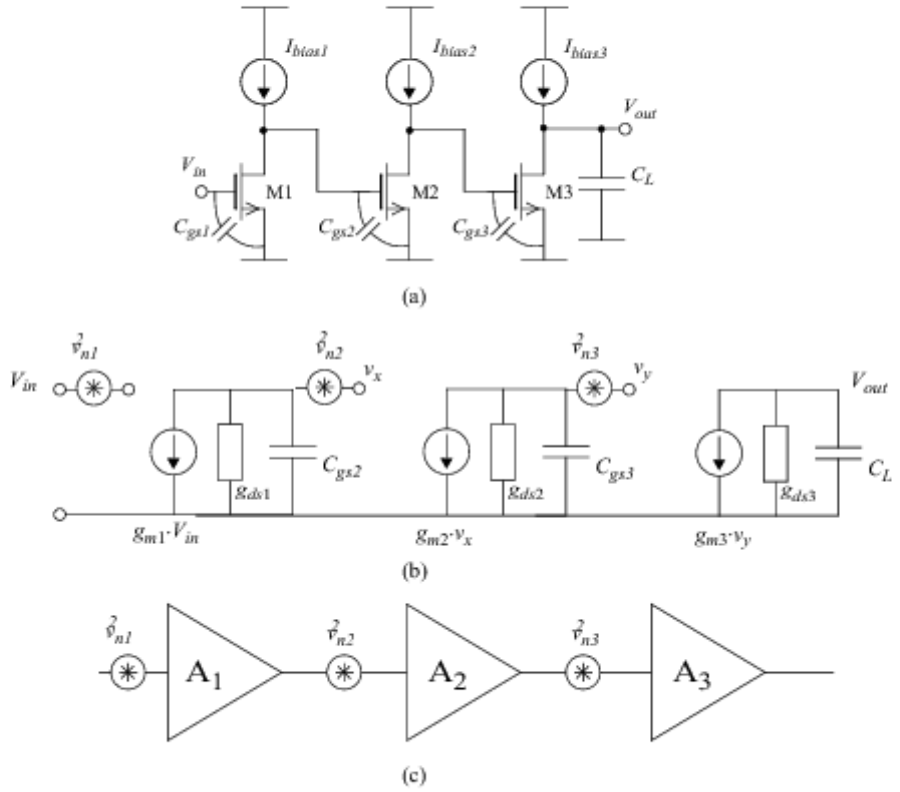


Figure 50: (a) Multi-stage circuit, (b) small-signal equivalent and (c) superposition principle.

gain stage is computed to

$$A_1 = \frac{-g_{m1}}{g_{ds1} + sC_{gs2}}; A_2 = \frac{-g_{m2}}{g_{ds2} + sC_{gs3}} \text{ and } A_3 = \frac{-g_{m3}}{g_{ds3} + sC_L} \tag{18.1}$$

The total output noise is now given by superpositioning the different noise contributions according to

$$V_{N,TOT}^2 = v_{n1}^2 \left|A_1 A_2 A_3\right|^2 + v_{n2}^2 \left|A_2 A_3\right|^2 + v_{n3}^2 \left|A_3\right|^2 \tag{18.2}$$

where

$$v_{ni}^2 = \frac{8kT}{3}\frac{1}{g_{mi}} \tag{18.3}$$

By combining Eq. (18.1), Eq. (18.2) and Eq. (18.3) we get

$$V_{N,TOT}^2 = \frac{8kT}{3}\frac{1}{g_{m1}}\frac{g_{m1}^2 g_{m2}^2 g_{m3}^2}{|g_{ds1}+j2\pi fC_{gs2}|^2|g_{ds2}+j2\pi fC_{gs3}|^2|g_{ds3}+j2\pi fC_L|^2} + \\ + \frac{8kT}{3}\frac{1}{g_{m2}}\frac{g_{m2}^2 g_{m3}^2}{|g_{ds2}+j2\pi fC_{gs3}|^2|g_{ds3}+j2\pi fC_L|^2} + \frac{8kT}{3}\frac{1}{g_{m3}}\frac{g_{m3}^2}{|g_{ds3}+j2\pi fC_L|^2} \tag{18.4}$$

and with all I_{bias} equal and all transistors equally sized -> equal g_m, g_{ds}, and C_{gs} we get

$$V_{N,TOT}^2 = \frac{8kT}{3}\frac{g_m}{|g_{ds}+j2\pi fC_L|^2}\left(\frac{g_m^4}{|g_{ds}+j2\pi fC_{gs}|^4} + \frac{g_m^2}{|g_{ds}+j2\pi fC_{gs}|^2} + 1\right) \tag{18.5}$$

The equivalent output noise power is computed as the integral of the spectral density over the frequency spectrum. This is here approximated using the noise bandwidth concept. Hence, the output noise power is

$$P_{out} = V_{N,TOT}^2\frac{p_1}{4} = \frac{2kT}{3}\frac{g_m}{g_{ds}^2}\left(\frac{g_m^4}{g_{ds}^4} + \frac{g_m^2}{g_{ds}^2} + 1\right)\frac{g_{ds}}{C_L} = \\ \frac{2kT}{3C_L}\frac{g_m}{g_{ds}}\left(\frac{g_m^4}{g_{ds}^4} + \frac{g_m^2}{g_{ds}^2} + 1\right) \tag{18.6}$$

b) The total output noise scales with I_D as

$$V_{N,TOT}^2 \sim \frac{g_m}{g_{ds}}\left(\frac{g_m^4}{g_{ds}^4} + \frac{g_m^2}{g_{ds}^2} + 1\right) \sim \frac{1}{\sqrt{I_D}}\left(\frac{1}{I_D^2} + \frac{1}{I_D} + 1\right) ;(g_m \approx 2\sqrt{\alpha I_D}, \\ g_{ds} \approx \lambda I_D), \tag{18.7}$$

i.e., increasing I_D decreases the equivalent output noise power.

The DC gain of the circuit is given by

$$A_{TOT} = A_1A_2A_3 = \frac{g_{m1}g_{m2}g_{m3}}{g_{ds1}g_{ds2}g_{ds3}} \sim \left(\frac{1}{I_D}\right)^{3/2}, \tag{18.8}$$

i.e., the DC gain will be lower for a larger I_D.

The bandwidth of the circuit is approximately given by the dominating pole because $C_L \gg C_{gs}$. This pole is computed from

$$A_3 = \frac{g_{m3}}{(g_{ds3}+sC_L)} = \frac{g_{m3}/g_{ds3}}{\left(1+\frac{sC_L}{g_{ds3}}\right)}, \tag{18.9}$$

i.e., the pole is given by

$$p_1 = \frac{g_{ds}}{C_L}. \tag{18.10}$$

Hence, the bandwidth scales as $p_1 \sim \lambda I_D$ -> larger bandwidth for a larger I_D.

c) From Eq. (18.2) we can see that A_3 amplifies all noise sources, i.e., this stage should have the smallest gain. A_1 on the other hand only amplifies the first noise source and should therefore have the largest gain.

6.2. Noise in CMOS circuits

19. Noise in CMOS circuits.

a) The equivalent small-signal model for the circuit is shown in Figure 51.

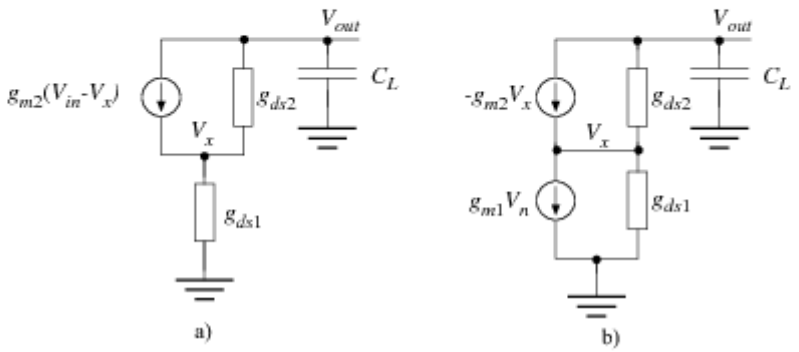


Figure 51: ESSS for the source-degenerated CS stage. a) Input to output. b) bias to output.

To compute the equivalent output noise power the transfer function from V_{in} to V_{out} and from V_b to V_{out} is computed. We start by setting up the equations required to compute the transfer function from the input to the output.

$$g_{m1}(V_{in}-V_x)-g_{mbs1}V_x+(V_{out}-V_x)g_{ds1}-V_xg_{ds2}=0 \tag{19.1}$$

$$g_{m1}(V_{in}-V_x)-g_{mbs1}V_x+(V_{out}-V_x)g_{ds1}+V_{out}sC_L=0 \tag{19.2}$$

Solving for V_{out} by eliminating V_x gives the following transfer function

$$H_1=\frac{V_{out}}{V_{in}}=\frac{g_{m1}}{g_{ds1}}\frac{1}{1+\dfrac{s}{\dfrac{g_{ds1}g_{ds2}}{C_L(g_{m1}+g_{mbs1}+g_{ds1}+g_{ds2})}}} \tag{19.3}$$

The equations for the transfer function between V_b and V_{out} is given by

$$g_{m2}V_n+g_{ds2}V_x+g_{m1}V_x+g_{mbs1}V_x+(V_x-V_{out})g_{ds1}=0 \tag{19.4}$$

$$g_{m1}V_x+g_{mbs1}V_x+(V_x-V_{out})g_{ds1}-V_{out}sC_L=0 \tag{19.5}$$

Solving for V_{out} by eliminating V_x results in

$$H_2=\frac{V_{out}}{V_b}=\frac{(g_{m1}+g_{mbs1}+g_{ds1})g_{m2}}{g_{ds1}g_{ds2}}\frac{1}{1+\dfrac{s}{\dfrac{g_{ds1}g_{ds2}}{C_L(g_{m1}+g_{mbs1}+g_{ds1}+g_{ds2})}}}$$

$$\approx\frac{(g_{m1}+g_{mbs1})g_{m2}}{g_{ds1}g_{ds2}}\frac{1}{1+\dfrac{s}{\dfrac{g_{ds1}g_{ds2}}{C_L(g_{m1}+g_{mbs1}+g_{ds1}+g_{ds2})}}} \tag{19.6}$$

The rms output noise is given by

$$V_{no}^2=\int|H_1|^2V_{in}^2df+\int|H_2|^2V_b^2df \tag{19.7}$$

where

$$V_{in}^2 = \frac{8kT}{3}\frac{1}{g_{m1}} \tag{19.8}$$

and

$$V_b^2 = \frac{8kT}{3}\frac{1}{g_{m2}} \tag{19.9}$$

The last two equations comes from the fact that the thermal noise power of a transistor is modelled as a gaussian white noise source.

The two integrals in Eq. (19.7) can be calculated using the concept of noise bandwidth which results in the following computation.

$$V_{no}^2 = \left(\frac{g_{m1}}{g_{ds1}}\right)^2 p_1 \frac{V_{in}^2}{4} + \left(\frac{(g_{m1}+g_{mbs1})g_{m2}}{g_{ds1}g_{ds2}}\right)^2 p_1 \frac{V_b^2}{4} \tag{19.10}$$

$$\begin{aligned} V_{no}^2 &= \frac{2kT}{3C_L}\left(\frac{g_{m1}}{g_{ds1}}g_{ds2} + \frac{(g_{m1}+g_{mbs1})^2 g_{m2}}{g_{ds1}g_{ds2}}\right)\frac{1}{g_{m1}+g_{mbs1}+g_{ds1}+g_{ds2}} \approx \\ &\approx \frac{2kT}{3C_L}\left(\frac{g_{m1}}{g_{ds1}(g_{m1}+g_{mbs1})}g_{ds2} + \frac{(g_{m1}+g_{mbs1})g_{m2}}{g_{ds1}g_{ds2}}\right) \\ &\approx \frac{2kT}{3C_L}\left(\frac{g_{ds2}}{g_{ds1}} + \frac{g_{m1}g_{m2}}{g_{ds1}g_{ds2}}\right) \end{aligned} \tag{19.11}$$

b) Relevant design parameters are for example the current through the circuit and the size of the transistor.

Rewriting the Eq. (19.11) with the design parameters yields

$$V_{no}^2 = \frac{2kT}{3}\frac{1}{C_L}\left(\frac{L_2}{L_1} + \frac{\sqrt{2\mu_n C_{ox} W_1 L_1}\sqrt{2\mu_n C_{ox} W_2 L_2}}{I_{bias}}\right) \tag{19.12}$$

The DC gain from the input to the output is given by

$$A_0 = \frac{g_{m1}}{g_{ds1}} \approx \sqrt{\frac{2\mu_n C_{ox} W_1 L_1}{I_{bias}}} \tag{19.13}$$

and the unity-gain frequency is given by

$$\omega_u \approx A_0 p_1 \approx \frac{g_{ds2}g_{m1}}{(g_{m1}+g_{mbs1}+g_{ds1}+g_{ds2})C_L} \approx \frac{g_{ds2}}{C_L} \approx \frac{I_{bias}}{L_2 C_L} \tag{19.14}$$

The equivalent output noise power can be reduced by:

- Increase the bias current -> Decreased DC gain, Increased unity-gain frequency, and Increased slew rate.
- Decreased W_2 -> No change to the DC gain, unity-gain frequency or slew rate.
- Decrease L_2 -> No change to the DC gain, increased unity-gain freq. and no change to the slew rate.

6.3. Noise in an amplifier

20. Noise in an amplifier.

a) The ESSS is shown in Figure 52.

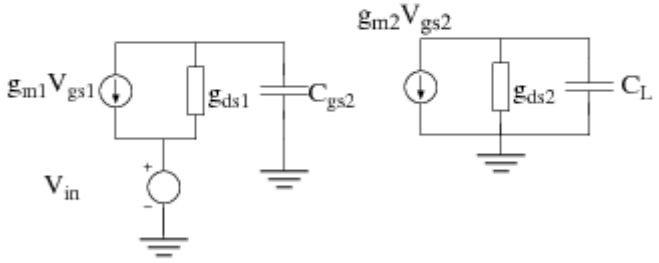


Figure 52: The ESSS of the noisy circuit

We have to calculate the transfer function from the gate of transistor M1 to the output, $H1$, from transistor M2 to the output, $H2$, and from the V_{in} to the output, H.

$$H1 = \frac{g_{m1}g_{m2}}{g_{ds1}g_{ds2} + s(g_{ds1}C_L + g_{ds2}C_{gs2}) + s^2C_LC_{gs2}} \tag{20.1}$$

According to exercise 2 the poles of the transfer function can be extracted directly.

$$p_{11} \approx \frac{g_{ds2}}{C_L} \tag{20.2}$$

and

$$p_{12} \approx \frac{g_{ds1}}{C_{gs2}} \tag{20.3}$$

Continuing with the transfer function from the gate of M2 to the output.

$$H2 = -\frac{g_{m2}}{g_{ds2} + sC_L} \tag{20.4}$$

The transfer function from V_{in} to the output is

$$H = \frac{(g_{m1} + g_{ds1})g_{m2}}{g_{ds1}g_{ds2} + s(g_{ds1}C_L + g_{ds2}C_{gs2}) + s^2C_LC_{gs2}} \tag{20.5}$$

The spectral density of the output can be calculated as

$$S_{out}(f) = |H_1(f)|^2V_{n1} + |H_2(f)|^2V_{n2} \tag{20.6}$$

where

$$V_{ni} = \frac{8kT}{3}\frac{1}{g_{mi}} \tag{20.7}$$

The noise power at the output can now be calculated according to the equation below.

$$V_{out}^2 = \int_0^\infty S_{out}(f)df \tag{20.8}$$

If we do not like to perform the integration we can use the concept of noise bandwidth (see

chapter 4 in Johns&Martin). The integral of a one pole system (or a system with well separated poles) is equivalent to the integral of a rectangle with the width of the dominant pole divided by four.

$$V_{out}^2 = \frac{2kT}{3}\frac{g_{m2}}{g_{ds2}}\frac{1}{C_L}\left(\frac{g_{m1}g_{m2}}{g_{ds1}^2}+1\right) \tag{20.9}$$

b) Derive the noise voltage that can be referred to the input.

The input referred noise voltage can be obtain by dividing the output referred noise voltage by $|H_1|^2$.

$$S_{in}(f) = S_{out}(f)/|H_1|^2 \tag{20.10}$$

This gives the answer

$$S_{in}(f) = \frac{8kT}{3}\frac{g_{ds2}}{g_{m1}}\left(1+\frac{g_{ds1}}{g_{m1}g_{m2}}^2\right) \tag{20.11}$$

c) Propose one way to increase the maximum signal-to-noise ratio, SNR in the circuit. What will happen to the DC gain, unity-gain frequency, bandwidth and the phase margin of the circuit?

The gain, p1, p2, ω_u of the circuit are already derived. Assume that the input voltage source is white.

$$V_{in}^2 = S_{in}(f) = \frac{2kT}{3}\frac{1}{g_{m1}}\left(1+\frac{g_{ds1}^2}{g_{m1}g_{m2}}\right)\frac{g_{ds2}}{C_L} \tag{20.12}$$

$$\propto \frac{2kT}{3}\frac{g_{ds2}}{g_{m1}}\frac{1}{C_L}\left(1+\frac{g_{ds1}^2}{g_{m1}g_{m2}}\right) \tag{20.13}$$

$$\propto \frac{I_2}{L_2}\sqrt{\frac{L_1}{W_1 I_1}}\left(1+\frac{I_1^2}{L_1^2}\sqrt{\frac{L_1L_2I_1I_2}{W_1W_2}}\right) \tag{20.14}$$

$$A_0 = \frac{g_{m1}g_{m2}}{g_{ds1}g_{ds2}} \propto \sqrt{\frac{W_1L_1W_2L_2}{I_{bias1}I_{bias2}}} \tag{20.15}$$

$$p1 = \frac{g_{ds2}}{C_L} \propto \frac{I_2}{L_2C_L} \tag{20.16}$$

$$p_2 \approx \frac{g_{ds1}}{C_{gs2}} \propto \frac{I_1}{W_2L_1L_2} \tag{20.17}$$

$$\omega_u \approx A_0p_1 = \frac{g_{m1}g_{m2}}{g_{ds1}C_L} \propto \sqrt{\frac{W_1L_1W_2I_{bias2}}{L_2I_{bias1}C_L}} \tag{20.18}$$

The above five equations shows that will happen if a parameter is changed. Remember that

$$1 \gg \frac{g_{ds1}}{g_{m1}g_{m2}}^2 \qquad (20.19)$$

Change	noise	A0	p1	unity-gain	phase margin
Increase W1	decreases	Increases	no change	increases	decreases
increase I1	decreases	decreases	no change	decreases	increases
Increase W2	decreases	increases	no change	increases	decreases
decrease I2	decreases	increases	decreases	decreases	increases

6.4. Noise in a common-source amplifier biased by a current mirror

21. Noise in a common-source amplifier biased by a current mirror.

a) The spectral density function of for the resistor is given by

$$V_R^2(f) = 4kTR \tag{21.1}$$

The ESSS is shown in Figure 53.

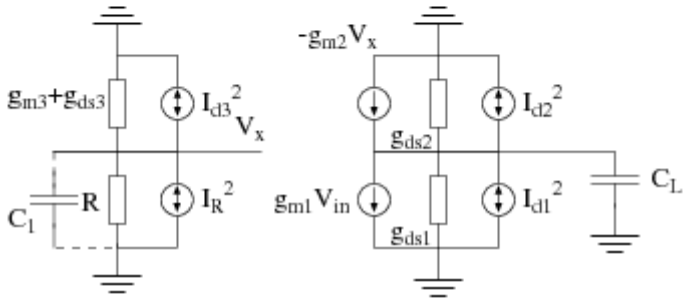


Figure 53: The ESSS of the noisy circuit.

We have to calculate the transfer function from the drain of transistor M1 to the output, H1, from transistor M2 to the output, H2, from transistor M3 to the output, H3, and from the resistor to the output, H4.

Consider a current source at in parallel with transistor M1 this will give a transfer function from that current source to the output according to

$$H1 = -\frac{1}{g_{ds1}+g_{ds2}+sC_L} \tag{21.2}$$

the pole is located in

$$p_1 = \frac{g_{ds1}+g_{ds2}}{C_L} \tag{21.3}$$

Continuing with the transfer function from the noise current source in transistor M2 to the output. This gives that $H2 = H1$.

The transfer function from M3 to the output is given by

$$H_3 = \frac{V_{out}}{V_x}\frac{V_x}{I_{nM3}} = -\frac{g_{m2}}{g_{ds1}+g_{ds2}+sC_L}\frac{1}{g_{ds3}+g_{m3}+\frac{1}{R}} \tag{21.4}$$

The transfer function from the resistor to the output is given by

$$H_4 = \frac{V_{out}}{V_x}\frac{V_x}{I_R} = -\frac{g_{m2}}{g_{ds1}+g_{ds2}+sC_L}\frac{1}{g_{ds3}+g_{m3}+\frac{1}{R}} \tag{21.5}$$

The spectral density function of the output can be calculated as

$$S_{out}(f) = |H_1(f)|^2 I_{n1}^2 + |H_2(f)|^2 I_{n2}^2 + |H_3(f)|^2 I_{n3}^2 + |H_4(f)|^2 I_R^2 \quad (21.6)$$

where

$$I_{ni} = \frac{8kT}{3} g_{mi} \quad (21.7)$$

The noise power at the output can now be calculated according to

$$V_{out}^2 = \int_0^\infty S_{out}(f)\,df \quad (21.8)$$

If we do not like to perform the integration we can use the concept of noise bandwidth (see chapter 4 in Johns&Martin). The integral of a one pole system (or a system with well separated poles) is equivalent to the integral of a rectangle with the width of the dominant pole divided by four.

$$V_{out}^2 = \frac{2kT}{g_{ds2} + g_{ds1}} \frac{1}{C_L} \left(\frac{g_{m1}}{3} + \frac{g_{m2}}{3} + \frac{g_{m2}^2}{\left(\frac{1}{R} + g_{m3} + g_{ds3}\right)^2} \left(\frac{g_{m3}}{3} + \frac{1}{2R} \right) \right) \quad (21.9)$$

b)

- Increase the load capacitor. This will decrease the unity-gain frequency of the amplifier, but the gain will not change.
- Decrease the resistance R. This will increase the current through transistor M3 and thereby through all transistors. The output noise voltage is approximately proportional to the inverse of the square root of the current through transistor M1. $g_{m3} \gg 1/R$ is assumed. Increasing the current will decrease the DC gain of the circuit but increase the unity-gain frequency.
- Decrease the size of M1. Decreases the DC gain and the unity-gain frequency.
- Decrease the size of both M2 and M3 => approximately constant current. No change will happen to neither the DC gain nor the unity-gain frequency.

c) The ESSS is the same as in Figure 53. The transfer function H1 and H2 will not be affected, but H3 and H4 will be changed.

$$H_3 = \frac{g_{m2}}{g_{ds1} + g_{ds2} + sC_L} \frac{1}{\frac{1}{R} + g_{m3} + g_{ds3} + sC_1} \quad (21.10)$$

$$H_4 = \frac{g_{m2}}{g_{ds1} + g_{ds2} + sC_L} \frac{1}{\frac{1}{R} + g_{m3} + g_{ds3} + sC_1} \quad (21.11)$$

The dominating pole of both H3 and H4 are approximately

$$p = \frac{\frac{1}{R} + g_{m3} + g_{ds3}}{C_1} \quad (21.12)$$

Using the same way to calculate the output noise as in 3a) gives

$$V_{out}^2 = \frac{2kT}{g_{ds2} + g_{ds1}} \left(\frac{1}{3C_L}(g_{m1} + g_{m2}) + \frac{g_{m2}^2}{g_{ds2} + g_{ds1}} \frac{1}{\frac{1}{R} + g_{m3} + g_{ds3}} \left(\frac{g_{m3}}{3C_1} + \frac{1}{2R} \right) \right)$$

6.5. Opamp noise (K6)

Exercise K6

1. Determine the transfer functions, $H_i = \frac{V_o}{V_{ni}}$, from all the noise sources in the amplifier (one for each transistor) to the output.

2. Calculate the total output noise by $S_{o,tot}(f) = \sum_{1=1}^{7} |H_i| S_i(f)$

3. calculate the equivalent input noise by $S_{i,tot}(f) = \frac{S_{o,tot}(f)}{A_{tot}}$

The noise sources in the differential amplifier have the following transfer functions to the gate of M_7 (the output of stage 1: V_{o1}).

$$\left|\frac{V_{o1}}{V_{n1}}\right| = \left|\frac{V_{o1}}{V_{n2}}\right| = g_{m1}R_{out1}, \left|\frac{V_{o1}}{V_{n3}}\right| = \left|\frac{V_{o1}}{V_{n4}}\right| = g_{m3}R_{out1} \text{ and } \left|\frac{V_{o1}}{V_{n5}}\right| = \frac{g_{m5}}{g_{m3}}$$

where $R_{out1} = r_{ds4} \| r_{ds2}$ and $R_{out2} = r_{ds6} \| r_{ds7}$.

To get the total transfer function to the output the noise voltages are amplified by the gain of stage 2:

$|H_1| = |H_2| = g_{m1}R_{out1} \cdot g_{m7}R_{out2}$, $|H_3| = |H_4| = g_{m3}R_{out1} \cdot g_{m7}R_{out2}$ and

$|H_5| = g_{m5}/g_{m3} \cdot g_{m7}R_{out2}$.

The transfer functions for the transistors in stage 2 are:

$|H_6| = g_{m6}R_{out2}$ and $|H_7| = g_{m7}R_{out2}$.

The total equivalent input noise spectral density is thus given by

$$S_{i,tot}(f) = \sum_{1=1}^{7} \frac{|H_i| S_i(f)}{A_{tot}} = S_1(f) + S_2(f) + \left(\frac{g_{m3}}{g_{m1}}\right)^2 (S_3(f) + S_4(f)) +$$

$$+ \left(\frac{g_{m5}}{g_{m3}A_1}\right)^2 S_5(f) + \left(\frac{1}{A_1}\right)^2 S_7(f) + \left(\frac{g_{m6}}{g_{m7}A_1}\right)^2 S_5(f) \approx$$

$$\approx 2 \cdot S_1(f) + \left(\frac{g_{m3}}{g_{m1}}\right)^2 2 \cdot S_3(f)$$

where $S_i(f) = 4kT\frac{2}{3}\frac{1}{g_{mi}} + \frac{K}{(W/L)_i C_{ox} f}$

Conclusions:

- Noise contributions from M_5-M_7 are small
- Large area for the transistors => small 1/f-noise
- $g_{m1} > g_{m3}$ => small contribution from M_3-M_4.
- Large g_{m1} => Small thermal noise in M_1-M_2.

6.6. Opamp noise 1

6.7. Opamp noise 2

6.8. Opamp noise 3

EXERCISE SECTION 7: CONTINUOUS-TIME FILTERS

7.1. First-order filter

Some important reasons for migrating to an active filter implementation are

- Poles and zeros can be placed anywhere in the real axis
- Poles and zeros can be placed independently
- The filter can be loaded without altering the transfer function.
- Integration and differentiation functions can be implemented
- Active filters can be designed to have a certain gain
- Cascading is possible to realize higher-order filters

7.2. Bilinear transfer functions

TBD Solution to be added.

7.3. Higher-order filters starting point (S 5.3)

TBD Refer pp. 104-107, 'Design of Analog Filters' , Schaumann and Valkenburg

7.4. Biquads (S 5.4)

TBD Refer Ex 3.11, pp. 107-109, 'Design of Analog Filters' , Schaumann and Valkenburg

7.5. Tow-Thomas (S 5.6)

TBD Refer pp. 129-134, 'Design of Analog Filters' , Schaumann and Valkenburg

7.6. Sensitivity analysis (S 5.7)

a) passive low pass RLC - Refer pp. 460-461, 'Design of Analog Filters' , Schaumann and Valkenburg

b) inverting amplifier - Refer pp. 457-458, 'Design of Analog Filters' , Schaumann and Valkenburg

7.7. Sallen Key

TBD Solution to be added.

7.8. Butterworth LP-filter

2.9 — Continuous-time filters

22. Butterworth LP-filter.

From the specification we get that $A_{max} = 3\,\text{dB}$ at $\omega_c = 2\pi \cdot 3{,}5 \cdot 10^3 \approx 22\,\text{krad/s}$ and that $A_{min} = 25\,\text{dB}$ at $\omega_s = 2\pi \cdot 10 \cdot 10^3 \approx 63$ krad/s.

Nomogram and formulas gives us a filter order of $N = 3$ (page 27 and 25).

According to the "Tabell och Formelsamlingen" at page 23 the in-resistance for the voltage supply is normalized to $1/R_i$. This gives us the refection factor $r = R_L/R_i = 600/1200 = 0{,}5$.

From the table at page 28 ($r = 0{,}5$) we get the normalized values:

$L_{1n} = 3{,}2612$, $C_{2n} = 0{,}7789$, $L_{3n} = 1{,}1811$

Which are de normalized according to $L = \frac{R_0 L_n}{\omega_0}$ and $C = \frac{C_n}{\omega_0 R_0}$ which finally gets us:

$L_1 = 88{,}9mH$, $C_2 = 59nF$, $L_3 = 49mH$

7.9. Chebychev LP filter

23. Chebychev LP filter.

The specification is given as:

$\omega_c = 1000$ rad/s, $\omega_s = 2000$ rad/s, $Z_L = 1k\Omega$, $Z_i = 125\Omega$.

A filter of Chebyshev I type shall be implemented, with lowest possible order that meets the specification above. The transfer curve is normalized giving us the maximal value $H_0 = 1$. By using that and the information given by the specification we get:

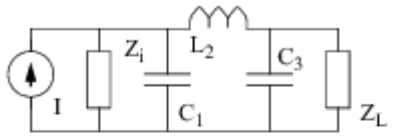
$$A_{max} = 20\log 1{,}2 \approx 1{,}58\,\text{dB} \text{ and } A_{min} = 20\log(1/0{,}1) = 20\,\text{dB} \tag{23.1}$$

By using a nomogram we can derive the filter order but it can also be calculated as

$$N = \left\lceil \operatorname{acosh}\sqrt{\frac{10^{0{,}1A_{min}}-1}{10^{0{,}1A_{max}}-1}} / \operatorname{acosh}\left(\frac{\omega_s}{\omega_c}\right) \right\rceil \approx \lceil 2{,}58 \rceil = 3 \tag{23.2}$$

We also know that we shall implement a current-mode filter and that $r = |Z_i/Z_L| = 1/8$. The ripple can be derived to be approximately 1,6 dB. This means that we shall use the closest lower value given by the table (= 1dB, page 36). We read the component values – and since we have a current mode filter and we have an odd filter order ($N = 3$) the first component must be a capacitance (page 23).

$C_{1n} = 12{,}5563$
$L_{2n} = 0{,}1657$
$C_{3n} = 8{,}8038$

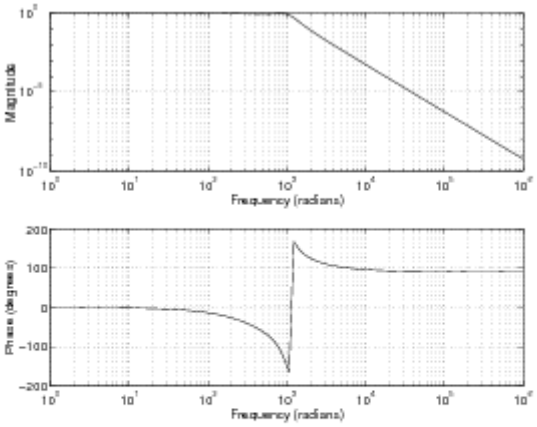


The values are de normalized, which gives us:

$$C_1 = \frac{C_{1n}}{\omega_0 Z_L} = \frac{12{,}5563}{1000 \cdot 1000} = 12{,}5563\mu F \tag{23.3}$$

$$L_2 = \frac{Z_L L_{2n}}{\omega_0} = \frac{1000 \cdot 0{,}1657}{1000} = 0{,}1657H \tag{23.4}$$

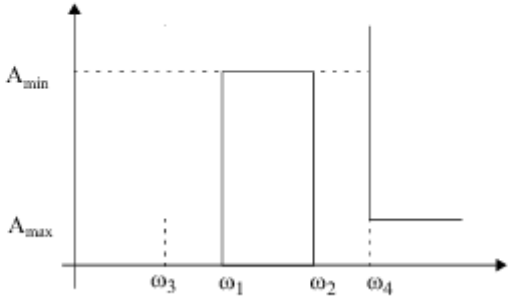
$$C_3 = \frac{C_{3n}}{\omega_0 Z_L} = 8{,}8038\mu F \tag{23.5}$$



7.10. Butterworth BS-filter

24. Butterworth BS-filter.

From the text we get the following specification.



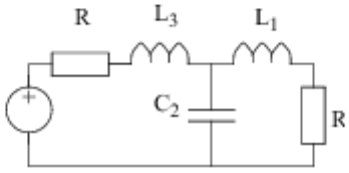
$$\begin{cases} \omega_1 = 1600\ [\text{rad/s}] \\ \omega_2 = 2000\ [\text{rad/s}] \\ \omega_3 = 800\ [\text{rad/s}] \\ \omega_4 = 4000\ [\text{rad/s}] \\ A_{min} = 50\ [\text{dB}] \\ A_{max} = 3\ [\text{dB}] \end{cases}$$

First we transform the BS-specification to an LP-specification. According to page 67 in "Tabell och Formelsamlingen" we get:

$$\begin{cases} \omega_I^2 = \omega_1\omega_2 = \omega_3\omega_4 = 1600 \cdot 2000 = 32 \cdot 10^6 \\ \Omega_2 = \dfrac{\omega_I^2}{\omega_4 - \omega_3} = \dfrac{32 \cdot 10^5}{3200} = 1 \cdot 10^3\ [\text{rad/s}] \\ \Omega_3 = \dfrac{\omega_I^2}{\omega_2 - \omega_1} = \dfrac{32 \cdot 10^5}{400} = 8 \cdot 10^3\ [\text{rad/s}] \end{cases}$$

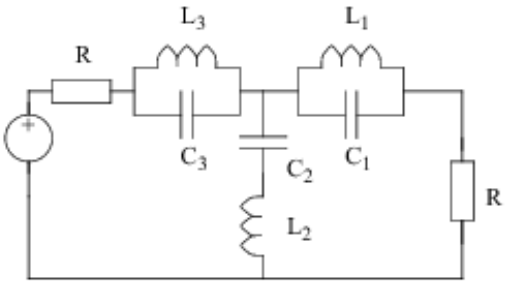
Nomogram, (the requirement on the attenuation is the same as for the BS specification) and the transformed frequencies gives the filter order N=3. We now get the normalized element values from table (r=1) and we de normalized them according to page 22 in "Tabell och Formelsamlingen" ($R_0 = 100$, $\omega_0 = \Omega_2$):

$$\begin{cases} R = 1 \\ L_1 = 1 \\ L_3 = 1 \\ C_2 = 2 \end{cases} \quad \text{denormalization} \quad \begin{cases} R = 100\Omega \\ L_1 = 0{,}1\text{H} \\ L_3 = 0{,}1\text{H} \\ C_2 = 20\mu\text{F} \end{cases}$$



Now we can transform our LP-filter back to the specified BP-filter according to page 67 in

"T&F", which gives us the final BS-filer:



$$\begin{cases} R = 100\Omega \\ L_1 = L_3 = 100\text{mH} \\ C_1 = C_3 = 3{,}13\mu\text{F} \\ C_2 = 20\mu\text{F} \\ L_2 = 15{,}6\text{mH} \end{cases}$$

7.11. A doubly resistive terminated ladder network

25. A doubly resistive terminated ladder network.

The solution is much the same as for Exercise 1.3, but since it is not specified which filter type to use it could be interesting to se how the filter order differs between the different filter types. First we transform the BS-specification to an LP-specification according to:

$$\begin{cases} \omega_I^2 = 4\pi^2 \cdot 0{,}9 \cdot 9 \cdot 10^6 \\ \Omega_2 = 2\pi \cdot 10^3 \text{ [rad/s]} \\ \Omega_3 = 2\pi \cdot 3 \cdot 10^3 \text{ [rad/s]} \end{cases}$$

Now we can use either a nomogram or some computer based program, e.g, Matlab to derive the different filter orders.

The following Matlab code can be used to derive the filter orders for a Butterworth-, Chebyshev I-, and a Cauer-type filter.

```
% Filter specification
Wc = 2*pi*1e3;
Ws = 6*pi*1e3;
Amax = 1;
Amin = 40;
% Filter order for a Butterworth-type filter
NBW = buttord(Wc, Ws, Amax, Amin,'s')
> NBW = 5
% Filter order for a Chebyshev I-type filter
NCI = cheb1ord(Wc, Ws, Amax, Amin,'s')
> NCI = 4
% Filter order for a Cauer-type filter
NCA = ellipord(Wc, Ws, Amax, Amin,'s')
> NCA = 3
```

Here we can see that for the given specification the Cauer-type filter gives the lowest filter order (N=3) followed by the Chebyshev I-type filter (N=4) and finally the Butterworth-type filter (N=5).

2.10 — Switched Capacitor Circuits

7.12. First-order GmC filter (Ex. 15.2 J&M)

✗ Covered by the main course book. The solutions are found via the course web page.

7.13. Second-order GmC filter (Ex. 15.3 J&M)

✗ Covered by the main course book. The solutions are found via the course web page.

7.14. Active filters (K11)

Exercise K11

Realize the filter having the transfer function

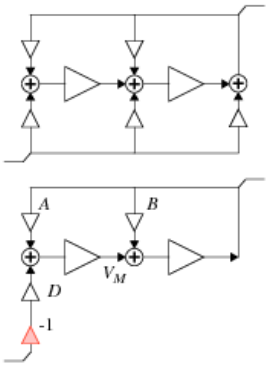
$$H(s) = \frac{1\times10^6}{s^2+3\times10^5\cdot s+6\times10^6}$$

We rewrite the function as

$$Y(s)\cdot[s^2+3\times10^5\cdot s+6\times10^6] = 1\times10^6\cdot X(s)$$

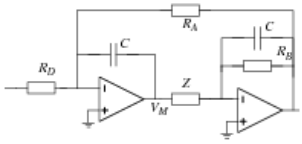
Or

$$Y(s) = -\frac{3\times10^5}{s}Y(s)-\frac{6\times10^6}{s^2}Y(s)+\frac{1\times10^6}{s^2}X(s)$$



The flow graph is transformed. $A = -6\times10^6$, $B = -3\times10^5$ and $D = -1\times10^6$. Note the insertion of the inverter. This can now be used to implement the active filter.

(Note that there is no inversion included in the active RC filter implementation). Now the component values have to be determined. Assume all capacitances to be equal. We can see that the intermediate node can be written as



$$V_M = \frac{A}{s}\cdot Y(s)+\frac{D}{s}\cdot X(s)$$

Identifying this from the active implementation, we have

$$V_M = -\frac{1}{sR_AC}\cdot Y(s)-\frac{1}{sR_CC}\cdot X(s)$$

This gives

$$A = -\frac{1}{R_AC} = -6\times10^6 \text{ and } D = -\frac{1}{R_DC} = -1\times10^6$$

We also see that the output can be written as

$$Y(s) = \frac{1}{s}\cdot V_M+\frac{B}{s}\cdot X(s)$$

Identifying this from the active implementation, we have

$$B = -\frac{1}{R_BC} = -3\times10^5$$

We also see that the implementation above is impossible. The intermediate node V_M is **not** transformed correctly. In fact, we have to inverse the voltage with a buffer.

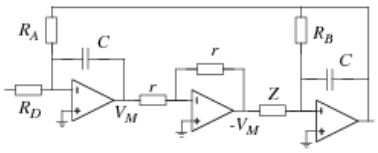
Then we identify

$$\frac{1}{sZC} = \frac{1}{s} \text{ or } Z = \frac{1}{C}$$

Set the capacitance to say $C = 1\mu\text{F}$. The equations give

$$R_A = \frac{1}{6},\ R_D = \frac{1}{1},\ R_B = \frac{10}{3} \text{ and}$$

$$Z = R = 1\times10^{6}.$$



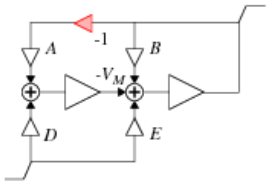
We do some notations. The structure could be changed by letting A be positive using an inverting buffer on the output signal instead. This decreases the number of opamps with one. We thereby also conclude that we do not find the simplest structure by forcing all input arguments to the summation nodes to be negative. We also see that we can use the inverting buffers to scale signal levels and relaxing the size on Z. There are numerous way to implement the filter. One can also soon realize that R_A, R_D and Z can dependently be scaled and still maintain true transfer function, see next exercise.

7.15. Active filters (K12)

Exercise K12

Realize the filter having the transfer function

$$H(s) = \frac{-1\times10^6(s-1)}{s^2+3\times10^5\cdot s+6\times10^6}$$



The function is rewritten in the same manner as in the previous exercise. In this case we however have a slightly different structure.

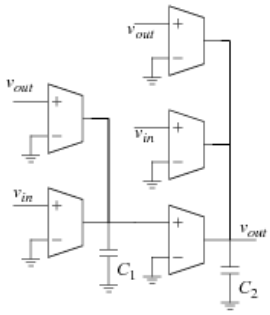
$$Y(s) = -\frac{3\times10^5}{s}Y(s) - \frac{6\times10^6}{s^2}Y(s) - \frac{1\times10^6}{s}X(s) + \frac{1\times10^6}{s^2}X(s)$$

We assume that we feed back the positive output (constant A) and we construct with a negative intermediate node, $-V_M$.

With

$A = 6\times10^6$, $B = -3\times10^5$, $D = 1\times10^6$ and $E = -1\times10^6$

In this implementation we will follow the signal flow graph



7.16. Active filters (K13)

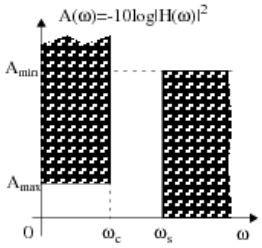
TBD Solutions to be added.

7.17. Active filters (K14)

TBD Solutions to be added.

7.18. Leapfrog filters (K15)

Exercise K15



Pass Band: $0 < f < 3.5\,\text{kHz}$ and $A_{max} = 1\,\text{dB}$

Stop Band $f > 10\,\text{kHz}$ and $A_{min} = 20\,\text{dB}$

Passive Butterworthfilter, order is found in table to be $N = 3$.

We choose a voltage driven π-net with reflection $r = 1$ for symmetry. Resistances are chosen to be

$$R_i = R_L = R_0 = 1k\Omega$$

Component values are found in table to be:

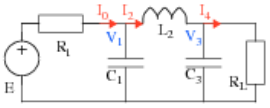
$$C_{3n} = 1,\ L_{2n} = 2 \text{ and } C_{1n} = 1$$

These values are denormalized according table to

$$C = \frac{C_n}{\omega_0 R_0},\ L = \frac{R_0 L_n}{\omega_0}, \text{ with } \omega_0 = \omega_c \varepsilon^{-1/N} = \omega_c [\sqrt{10^{0.1A_{max}} - 1}]^{-1/N} \approx 27.55\,\text{krad/s}.$$

This gives

$$C_1 = C_3 = 36.3nF \text{ and } L_2 = 72.6mH$$



A number of filter components have been found. Create a signal flow chart for the circuit. The nodal voltages for the circuit is found to be (normalized with R):

$$I_0 = \frac{E - V_1}{R_i} \qquad RI_0 = \frac{R}{R_i}(E - V_1)$$

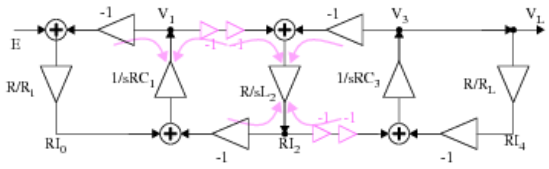
$$V_1 = \frac{1}{sC_1}(I_0 - I_2) \qquad V_1 = \frac{1}{sC_1 R}(RI_0 - RI_2)$$

$$I_2 = \frac{V_1 - V_3}{sL_2} \qquad RI_2 = \frac{R}{sL_2}(V_1 - V_3)$$

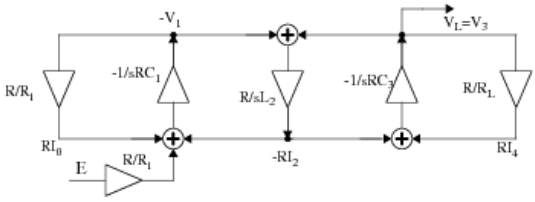
$$V_3 = \frac{1}{sC_3}(I_2 - I_4) \qquad V_3 = \frac{1}{sRC_3}(RI_2 - RI_4)$$

$$I_4 = \frac{V_3}{R_L} \qquad RI_4 = \frac{R}{R_L}V_3$$

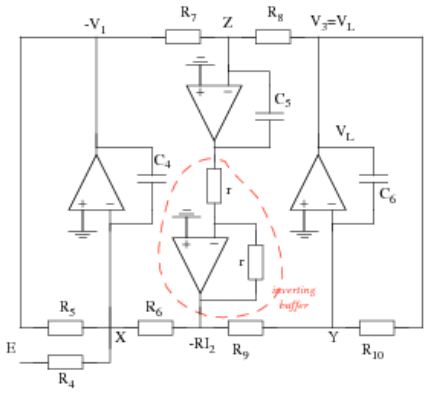
From these equations we find:



Modify the graph by propagating the inverters and denote negative voltage nodes:



We now have a number of integrators, $K\frac{1}{s}$. Realized with operational amplifiers we have a structure according to



We now have to determine the component values for this realization, This is done by comparing the signal flow chart with the OPamp net:

Leapfrog Signal flow graph Result

$$[-V_1]_E = -\frac{1}{sC_4}\frac{E}{R_4} \qquad [-V_1]_E = \frac{R}{R_i}\cdot\frac{-E}{sRC_1} = -\frac{E}{sR_iC_1} \quad C_4R_4 = C_1R_i$$

$$[-V_1]_{-V_1} = -\frac{1}{sC_4}\cdot\frac{V_1}{R_5} \qquad [-V_1]_{-V_1} = \frac{R}{R_i}\cdot\frac{-V_1}{sRC_1} = -\frac{-V_1}{sR_iC_1} \quad C_4R_5 = C_1R_i$$

$$[-V_1]_{-RI_2} = -\frac{1}{sC_4}\frac{-RI_2}{R_6} \qquad [-V_1]_{-RI_2} = -\frac{1}{sRC_1}(-RI_2) \qquad C_4R_6 = C_1R$$

$$[-RI_2]_{-V_1} = -\frac{(-1)}{sC_5}\cdot\frac{-V_1}{R_7} \qquad [-RI_2]_{-V_1} = \frac{R}{sL_2}(-V_1) \qquad C_5R_7 = L_2/R$$

$$[-RI_2]_{V_3} = -\frac{(-1)}{sC_5}\cdot\frac{V_3}{R_8} \qquad [-RI_2]_{V_3} = \frac{R}{sL_2}V_3 \qquad C_5R_8 = L_2/R$$

$$[V_3]_{-RI_2} = -\frac{1}{sC_6}\frac{-RI_2}{R_9} \qquad [V_3]_{-RI_2} = -\frac{1}{sRC_3}(-RI_2) \qquad C_6R_9 = C_3R$$

$$[V_3]_{V_3} = -\frac{1}{sC_6}\frac{V_3}{R_{10}} \qquad [V_3]_{V_3} = -\frac{1}{sRC_3}\frac{R}{R_L}V_3 = -\frac{V_3}{sC_3R_L} \quad C_6R_{10} = C_3R_L$$

Now we have several equations. Choose all capacitors to be equally large, maybe:

$$C_4 = C_5 = C_6 = 30nF$$

The values are chosen to be approximately equal to those found in the ladder filter realization, which would give reasonable resistance values. From the equations we also find:

$$R_4 = R_5 = \frac{C_1R_i}{C_4} = \frac{36.3nF\cdot 1k\Omega}{30nF} = 1.21k\Omega \text{ och } R_{10} = \frac{C_3R_L}{C_6} = 1.21k\Omega$$

And this also gives

$$R_6 = R_9 = \frac{C_1R}{C_4} \text{ and } R_7 = R_8 = \frac{L_2}{C_5R}$$

For symmetry, $R_6 = R_7 = R_8 = R_9$ are chosen to be equal, which gives:

$$R^2 = \frac{L_2C_4}{C_1C_5} \Rightarrow R = \sqrt{L_2/C_1} = 1000\sqrt{72.6/36.3} \approx 1.41k\Omega$$

Finally, we have

$$R_6 = R_7 = R_8 = R_9 = 1.21\cdot 1.41k\Omega \approx 1.71k\Omega.$$

The final value that has to be determined is the resistor value used in the invering buffer, r. Choose r to be equal to anyone of the other resistances, i.e., :

$$r = R_6 = 1.71k\Omega.$$

7.19. Leapfrog filters (K16)

Exercise K16

Synthesize an active elliptic leapfrog filter. Termination resistances are $1k\Omega$. Specification gives:

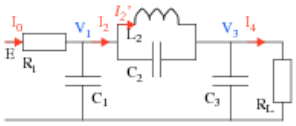
Pass band: $0 < \omega < 2\pi$ krad/s, $A_{max} = 0.1$ dB

Stop band: $\omega > 4\pi$ krad/s, $A_{min} > 20$ dB

Order is found with table to be $N = 3$.

This gives following filter structure. Component values are found to be

$C_1' = C_3' = 0.8740$, $C_2' = 0.2411$ and $L_2' = 0.9083$, and $R_i = R_L = 1k\Omega$, $\kappa^2 = 1$.



Denormalized values are given by

$$C = \frac{C_n}{\omega_0 R_0} \text{ and } L = \frac{R_0}{\omega_0} L_n \text{ give } C_1 = C_3 \approx 139.1nF,\ C_2 \approx 38.4nF,\ L_2 \approx 144.6mH$$

Set up the equations:

$$I_0 = \frac{E - V_1}{R_i} \qquad RI_0 = \frac{R}{R_i}(E - V_1)$$

$$V_1 = \frac{1}{sC_1}(I_0 - I_2) \qquad V_1 = \frac{1}{sRC_1}(RI_0 - RI_2)$$

$$I_2 = \frac{1}{L_2 \| C_2}(V_1 - V_3) \qquad RI_2 = \frac{R}{sL_2/(1 + s^2 L_2 C_2)}(V_1 - V_3)$$

$$V_3 = \frac{1}{sC_3}(I_2 - I_4) \qquad V_3 = \frac{1}{sRC_3}(RI_2 - RI_4)$$

$$I_4 = \frac{V_3}{R_L} \qquad RI_4 = \frac{R}{R_L} V_3$$

Introuduce a current, I'_2, through the inductor. The equations are modified:

$$RI_2 = RI_2' + sRC_2(V_1 - V_3) \text{ and } RI_2' = \frac{R}{sL_2}(V_1 - V_3)$$

The RI_2 expression can be eliminated, and gives:

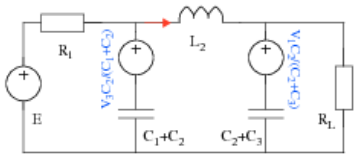
$$V_1 = \frac{1}{sRC_1}(RI_0 - RI_2' - sRC_2(V_1 - V_3)) \Rightarrow$$

$$V_1 = \frac{1}{sR(C_1 + C_2)}(RI_0 - RI_2') + \frac{C_2}{C_1 + C_2} V_3$$

And correspondingly

$$V_3 = \frac{1}{sR(C_2+C_3)}(RI_2' - RI_4) + \frac{C_2}{C_2+C_3}V_1$$

This gives the structure with a pair of "helping" voltage sources.



The equations are written as:

$$RI_0 = \frac{R}{R_i}(E - V_1)$$

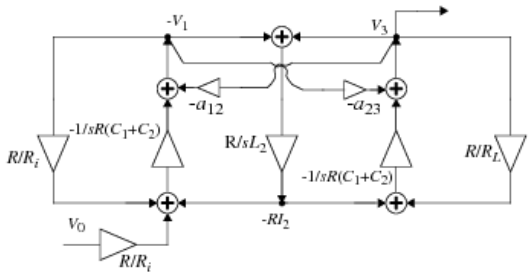
$$V_1 = \frac{1}{sR(C_1+C_2)}(RI_0 - RI_2') + \frac{C_2}{C_1+C_2}V_3$$

$$RI_2' = \frac{R}{sL_2}(V_1 - V_3)$$

$$V_3 = \frac{1}{sR(C_2+C_3)}(RI_2' - RI_4) + \frac{C_2}{C_2+C_3}V_1$$

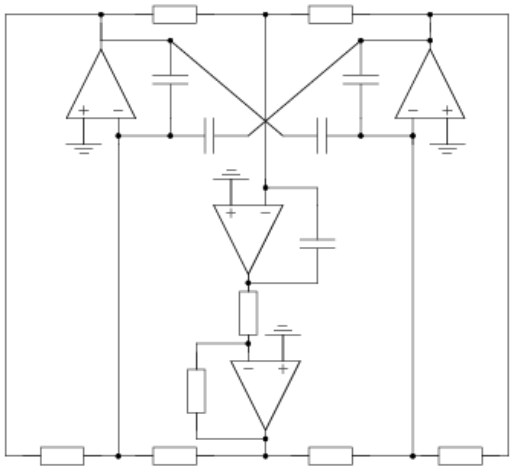
$$RI_4 = \frac{R}{R_L}V_3$$

The signal flow chart is given by



Realization

The a_{ij} terms can be realized by using capacitors instead of resistances. This realizes a negative and scaled signal flow.



Component values are found using the same manner as for the previous exercise. The resistances can be implemented by using transistors.

7.20. Leapfrog filters (K17)

TBD Solutions to be added.

7.21. Leapfrog filters (K18)

TBD Solutions to be added.

7.22. Gyrators (K19)

TBD Solutions to be added.

7.23. Gm-C filters (K20)

TBD Solutions to be added.

7.24. Gm-C filter parasitics (K21)

TBD Solutions to be added.

7.25. Gm-C filters (K22)

TBD Solutions to be added.

EXERCISE SECTION 8: SWITCHED CAPACITOR CIRCUITS

8.1. Switched capacitor accumulator 1

26. Switched capacitor circuit.

a) Here we use the charge analysis. The SC circuit is shown for both clock phases in Figure 54.

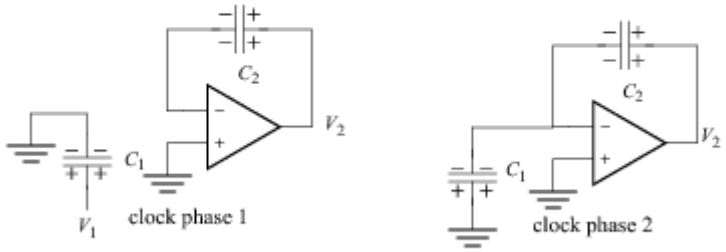


Figure 54: The SC circuit in both clock phases.

Using the charge analysis in the circuit starting at time t *(clock phase 1)*

$$q_1(t) = (V_1(t) - 0)C_1 \tag{26.1}$$

$$q_2(t) = (V_2(t) - 0)C_2 \tag{26.2}$$

At time $t + \tau$ *(clock phase 2)*

$$q_1(t+\tau) = (0 - 0)C_1 \tag{26.3}$$

$$q_2(t+\tau) = (V_2(t+\tau) - 0)C_2 \tag{26.4}$$

At time $t + 2\tau$ *(clock phase 1)*

$$q_1(t+2\tau) = (V_1(t+2\tau) - 0)C_1 \tag{26.5}$$

$$q_2(t+2\tau) = (V_2(t+2\tau) - 0)C_2 \tag{26.6}$$

Another equation is required to be able to compute the transfer function. This equation comes from the charge conservation. In clock phase 2 the charge of the two capacitors can not disappear since the charge can not be discharged through the opamp input terminals. This means that the charge on the capacitors at the end of clock phase 1 is equal to the charge of the capacitors during the whole clock phase 2.

$$q_1(t) + q_2(t) = q_1(t+\tau) + q_2(t+\tau) \tag{26.7}$$

The charge of C_2 at the time $t + \tau$ is equal to the charge of C_2 at time $t + 2\tau$ since no charge can be given by the opamp input.

$$q_2(t+\tau) = q_2(t+2\tau) \tag{26.8}$$

Inserting the above equations into Eq. (26.7) gives

$$V_1(t)C_1 + V_2(t)C_2 = V_2(t+\tau)C_2 = V_2(t+2\tau)C_2 \tag{26.9}$$

To compute the transfer function we have to take the Z-transform of both sides.

$$V_1(z)C_1 + V_2(z)C_2 = V_2(z)zC_2 \tag{26.10}$$

Solving for $V_2(z)/V_1(z)$ gives

$$\frac{V_2(z)}{V_1(z)} = \frac{C_1}{C_2}\frac{1}{z-1} = \frac{C_1}{C_2}\frac{z^{-1}}{1-z^{-1}} \tag{26.11}$$

This is a non inverting discrete-time accumulator (compare continuous-time integrator) with

a delay of one clock period $T = 2\tau$.

b) Each switch and capacitor has parasitic capacitances connected to ground. In Figure 55 the

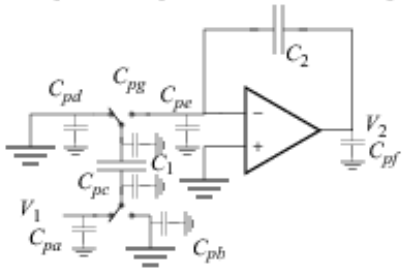


Figure 55: A non inverting accumulator with parasitics.

parasitics are shown.

C_{pa} is connected between the ideal input and ground and will not change the transfer function.

C_{pb} is connected between ground and ground and thereby not change the transfer function.

C_{pc} is connected between the ideal input and ground or shorted to ground. No effect on the transfer function.

C_{pd} Connected to ground. No effect on the transfer function.

C_{pe} is connected between ground and virtual ground thereby not changing the transfer function.

C_{pf} is connected to the ideal operational amplifier and ground not changing the transfer function.

C_{pg} is connected to either ground or virtual ground and thereby not changing the transfer function.

The transfer function is not sensitive to parasitics.

8.2. Switched capacitor accumulator 2

27. Switched capacitor circuit.

a) Here we use the charge analysis. The SC circuit is shown for both clock phases in Figure 56.

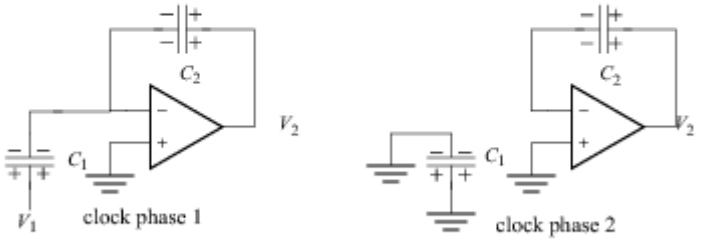


Figure 56: The SC circuit in both clock phases.o

Using the charge analysis in the circuit starting at time t *(clock phase 1)*

$$q_1(t) = (V_1(t)-0)C_1 \tag{27.1}$$

$$q_2(t) = (V_2(t)-0)C_2 \tag{27.2}$$

At time $t+\tau$ *(clock phase 2)*

$$q_1(t+\tau) = (0-0)C_1 \tag{27.3}$$

$$q_2(t+\tau) = (V_2(t+\tau)-0)C_2 \tag{27.4}$$

At time $t+2\tau$ *(clock phase 1)*

$$q_1(t+2\tau) = (V_1(t+2\tau)-0)C_1 \tag{27.5}$$

$$q_2(t+2\tau) = (V_2(t+2\tau)-0)C_2 \tag{27.6}$$

Another equation is required to be able to compute the transfer function. This equation comes from the charge conservation. In clock phase 1, $t+2\tau$, the charge of the two capacitors can not disappear since the charge can not be discharged through the opamp input terminals. This means that the charge on the capacitors at the end of clock phase 2, $t+\tau$, is equal to the charge of the capacitors during the whole clock phase 1, $t+2\tau$.

$$q_1(t+\tau)+q_2(t+\tau) = q_1(t+2\tau)+q_2(t+2\tau) \tag{27.7}$$

The charge of C_2 at the time t is equal to the charge of C_2 at time $t+\tau$ since no charge can be given by the opamp input.

$$q_2(t) = q_2(t+\tau) \tag{27.8}$$

Inserting the above equations into Eq. (27.7) gives

$$V_2(t+\tau)C_2 = V_2(t+2\tau)C_2 + V_1(t+2\tau)C_1 \tag{27.9}$$

and

$$V_2(t) = V_2(t+\tau) \tag{27.10}$$

To compute the transfer function we have to take the Z-transform of both sides.

$$V_2(z)C_2 = V_2(z)zC_2 + V_1(z)zC_1 \tag{27.11}$$

Solving for $V_2(z)/V_1(z)$ gives

$$\frac{V_2(z)}{V_1(z)} = -\frac{C_1}{C_2}\frac{z}{z-1} = -\frac{C_1}{C_2}\frac{1}{1-z^{-1}} \tag{27.12}$$

This is an inverting discrete-time accumulator (compare continuous-time integrator) with no delay.

b) Each switch and capacitor has parasitic capacitances connected to ground. In Figure 57 the

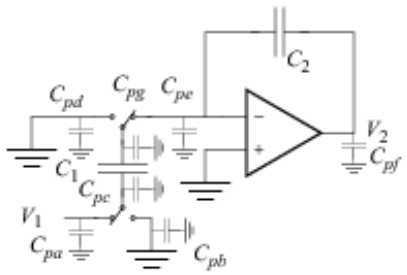


Figure 57: An inverting accumulator with parasitics.

parasitics are shown.

C_{pa} is connected between the ideal input and ground and will not change the transfer function.

C_{pb} is connected between ground and ground and thereby not change the transfer function.

C_{pc} is connected between the ideal input and ground or shorted to ground. No effect on the transfer function.

C_{pd} Connected to ground. No effect on the transfer function.

C_{pe} is connected between ground and virtual ground thereby not changing the transfer function.

C_{pf} is connected to the ideal operational amplifier and ground not changing the transfer function.

C_{pg} is either connected to the virtual ground, ground or ground and ground. Hence, the transfer function of the circuit is not changed.

The transfer function is not sensitive to parasitics.

8.3. Switched capacitor circuit 1

28. Switched capacitor circuit.

a) Here we use the charge analysis. The SC circuit is shown for both clock phases in Figure 58.

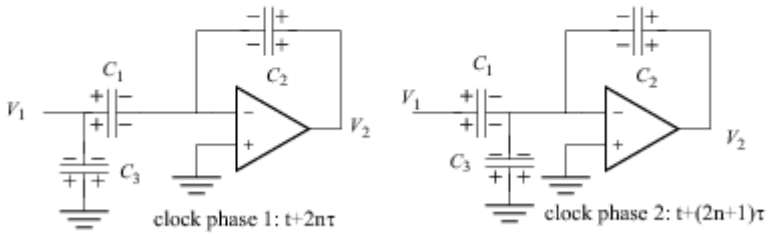


Figure 58: The SC circuit in both clock phases.

Using the charge analysis in the circuit starting at time *t (clock phase 1)*

$$q_1(t) = (V_1(t) - 0)C_1 \tag{28.1}$$

$$q_2(t) = (V_2(t) - 0)C_2 \tag{28.2}$$

$$q_3(t) = (0 - V_1(t))C_3 \tag{28.3}$$

At time $t + \tau$ *(clock phase 2)*

$$q_1(t+\tau) = (V_1(t+\tau) - 0)C_1 \tag{28.4}$$

$$q_2(t+\tau) = (V_2(t+\tau) - 0)C_2 \tag{28.5}$$

$$q_3(t+\tau) = (0 - 0)C_3 \tag{28.6}$$

At time $t + 2\tau$ *(clock phase 1)*

$$q_1(t+2\tau) = (V_1(t+2\tau) - 0)C_1 \tag{28.7}$$

$$q_2(t+2\tau) = (V_2(t+2\tau) - 0)C_2 \tag{28.8}$$

$$q_3(t+2\tau) = (0 - V_1(t+2\tau))C_3 \tag{28.9}$$

Other equations are required to be able to compute the transfer function. These equations come from the charge conservation. In clock phase 2 the charge of the three capacitors can not disappear since the charge can not be discharged through the opamp input terminals. This means that the charge on the capacitors at the end of clock phase 1 is equal to the charge of the capacitors during the whole clock phase 2.

$$q_1(t) + q_2(t) + q_3(t) = q_1(t+\tau) + q_2(t+\tau) + q_3(t+\tau) \tag{28.10}$$

The charge of C_1 and C_2 at the time $t + \tau$ are equal to the charge of C_1 and C_2 at time $t + 2\tau$ since no charge can be given by the opamp input.

$$q_1(t+\tau) + q_2(t+\tau) = q_1(t+2\tau) + q_2(t+2\tau) \tag{28.11}$$

Inserting the above equations into Eq. (28.10) gives

$$V_1(t)C_1 + V_2(t)C_2 - V_1(t)C_3 = V_1(t+\tau)C_1 + V_2(t+\tau)C_2 \tag{28.12}$$

Inserting equation Eq. (28.11) into Eq. (28.12) gives

$$V_1(t)C_1 + V_2(t)C_2 - V_1(t)C_3 = V_1(t+2\tau)C_1 + V_2(t+2\tau)C_2 \tag{28.13}$$

To compute the transfer function we make a Z-transformation of both sides.

$$V_1(z)(C_1 - C_3 - zC_1) = V_2(z)(zC_2 - C_2) \tag{28.14}$$

Solving for $V_2(z)/V_1(z)$ gives

$$\frac{V_2(z)}{V_1(z)} = \frac{C_1 - C_3 - zC_1}{zC_2 - C_2} = -\frac{C_1}{C_2}\frac{1+z}{z-1} = -\frac{C_1}{C_2}\frac{1+z^{-1}}{1-z^{-1}} \tag{28.15}$$

This is a bilinear inverting discrete-time accumulator (compare continuous-time integrator).

b) Each switch and capacitor has parasitic capacitances connected to ground. In Figure 59 the

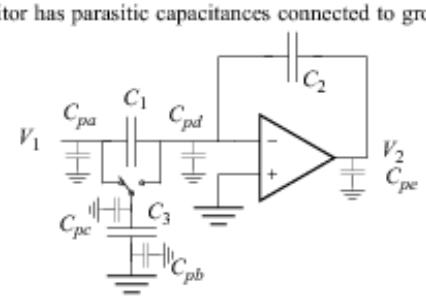


Figure 59: A bilinear inverting accumulator with parasitics.

parasitics are shown.

C_{pa} is connected between the ideal input and ground and will not change the transfer function.

C_{pb} is connected between ground and ground and thereby not change the transfer function.

C_{pc} The parasitic capacitor is in parallel with C_3 and thereby it will change the transfer function according to

$$\frac{V_2(z)}{V_1(z)} = \frac{C_1 - C_3 - C_{pc} - zC_1}{zC_2 - C_2} = -\frac{C_1}{C_2}\frac{1+z}{z-1} - \frac{C_{pc}}{C_2}\frac{1}{z-1} = -\frac{C_1}{C_2}\frac{1+z^{-1}}{1-z^{-1}} - \frac{C_{pc}}{C_2}\frac{z^{-1}}{1-z^{-1}}$$

C_{pd} is connected between ground and virtual ground thereby not changing the transfer function.

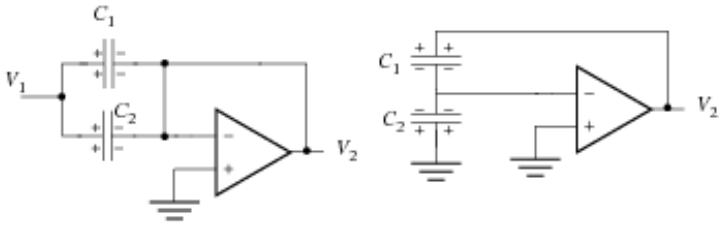
C_{pe} is connected to the ideal operational amplifier and ground not changing the transfer function.

The transfer function is sensitive to parasitics.

8.4. Switched capacitor circuit 2

29. Switched capacitor circuit.

a) The the two different clock phases of the circuit is shown Figure 60.



clock phase 1 clock phase 2

Figure 60: The circuit in the two different clock phases.

Starting in the clock phase 1 at time t:

$$q_1(t) = (V_1(t) - 0)C_1 \tag{29.1}$$

$$q_2(t) = (V_1(t) - 0)C_2 \tag{29.2}$$

At time $t + \tau$

$$q_1(t+\tau) = V_2(t+\tau)C_1 \tag{29.3}$$

$$q_2(t+\tau) = 0 \tag{29.4}$$

At time $t + 2\tau$

$$q_2(t+2\tau) = (V_1(t+2\tau) - 0)C_1 \tag{29.5}$$

$$q_2(t+2\tau) = (V_1(t+2\tau) - 0)C_2 \tag{29.6}$$

The last equation comes from the charge conservation. The charge at the end of clock phase t is equal to the charge during clock phase $t + \tau$ since no charge can vanish into the operational amplifier.

$$q_1(t) + q_2(t) = q_1(t+\tau) + q_2(t+\tau) \tag{29.7}$$

Inserting the above equations into Eq. (29.7) gives.

$$V_1(t)C_1 + V_1(t)C_2 = V_2(t+\tau)C_1 + 0 \tag{29.8}$$

performing z-transformation on both sides gives

$$V_1(z)(C_1 + C_2) = z^{1/2}V_2(z)C_1 \tag{29.9}$$

which gives the following transfer function

$$\frac{V_2(z)}{V_z(z)} = z^{-1/2}\frac{C_1 + C_2}{C_1} = z^{-1/2}\left(1 + \frac{C_2}{C_1}\right) \tag{29.10}$$

The factor $z^{-1/2}$ is just a time delay from the input to the output, it means that when the input is sampled at time t, the output will not be available until the time $t + \tau$.

b) There will be parasitic capacitances at both sides of each switch and the input and output of the operational amplifier as shown in Figure 61.

C_{pa} is connected between the ideal input and ground. Not changing the transfer function

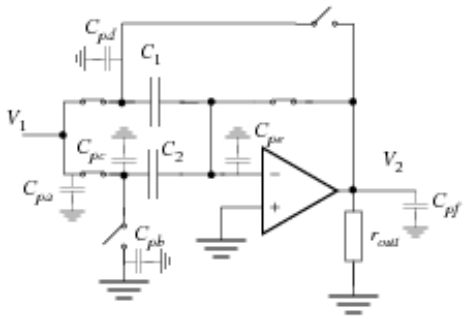


Figure 61: The SC-circuit with all parasitic capacitances.

thereby not interacting with the transfer function.

C_{pd} is connected between ideal input and ground or the ideal output of the opamp and ground and thereby no change in the transfer function will appear.

C_{pe} is connected between the virtual ground and ground not causing any change in the transfer function.

C_{pf} is connected between the ideal output of the opamp and ground and thereby not changing the transfer function.

Hence, the circuit is insensitive of capacitive parasitics with respect to the transfer function.

c) To handle the offset voltage it is assumed to be a function of time with the properties, $V_{os}(t+n\cdot\tau) = V_{os}(t)\forall n$ and the Z-transform of $V_{os}(t)$ equals $V_{os}(z)$.

At time t, $t+2\tau$, $t+4\tau$ and so on, the potential at the negative input of the operational amplifier, V_x, will be equal to

$$V_x(t+n\tau) = \frac{A}{1+A}V_{os}(t)\,. \tag{29.11}$$

At time $t+\tau$, $t+3\tau$, $t+5\tau$ and so on, the potential at the negative input of the operational amplifier will be equal to

$$V_x(t+(n+1)\tau) = V_{os}(t) - \frac{V_2(t+(n+1)\tau)}{A}\,. \tag{29.12}$$

Using charge analysis gives:

$$q_1(t) = \left(V_1(t) - \frac{A}{1+A}V_{os}(t)\right)C_1 \tag{29.13}$$

$$q_2(t) = \left(V_1(t) - \frac{A}{1+A}V_{os}(t)\right)C_2 \tag{29.14}$$

$$q_1(t+\tau) = (V_2(t+\tau) - V_x(t+\tau))C_1 =$$

$$= \left(V_2(t+\tau)\left(1+\frac{1}{A}\right) - V_{os}(t)\right)C_1 \tag{29.15}$$

8.5. Switched capacitor circuit 3

30. Switched capacitor circuit.
The circuit is shown in Figure 62.

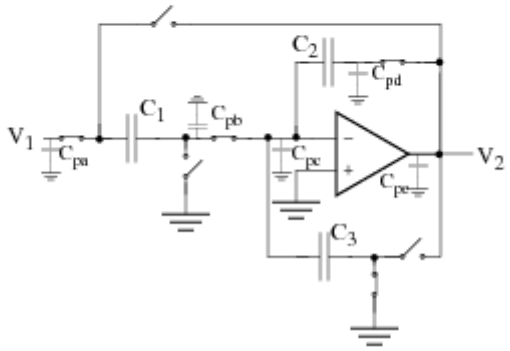


Figure 62: The SC circuit with parasitic capacitances

V_n is the input voltage of the amplifier. The transfer function can be derived by using charge analysis.

t:

$$q_1(t) = C_1(V_1(t) - V_n(t)) \tag{30.1}$$

$$q_2(t) = C_2(V_2(t) - V_n(t)) \tag{30.2}$$

$$q_3(t) = C_3(-V_n(t)) \tag{30.3}$$

t+τ:

$$q_1(t+\tau) = C_1 V_2(t+\tau) \tag{30.4}$$

$$q_2(t+\tau) = q_2(t) \tag{30.5}$$

$$q_3(t+\tau) = C_3(V_2(t+\tau) - V_n(t+\tau)) \tag{30.6}$$

t+2τ:

$$q_1(t+2\tau) = C_1(V_1(t+2\tau) - V_n(t+2\tau)) \tag{30.7}$$

$$q_2(t+2\tau) = C_2(V_2(t+2\tau) - V_n(t+2\tau)) \tag{30.8}$$

$$q_3(t+2\tau) = -C_3 V_n(t+2\tau) \tag{30.9}$$

Charge redistribution

$$q_2(t) + q_3(t) = q_2(t+\tau) + q_3(t+\tau) \tag{30.10}$$

$$q_1(t+2\tau) + q_2(t+2\tau) + q_3(t+2\tau) = q_1(t+\tau) + q_2(t+\tau) + q_3(t+\tau) \tag{30.11}$$

We also know that $V_2 = A(V_p - V_n)$ where V_p and V_n is the positive and negative input node of the OTA respectively. An offset voltage of the OTA is modelled by a voltage source at

the positive input. Solve for V_n.

$$V_n(t) = -\frac{V_2}{A} + V_{os}(t) \text{ , where } V_{os}(t + n \cdot \tau) = V_{os}(t) \forall n \tag{30.12}$$

Eq. (30.10) gives that

$$-C_3 V_n(t) = C_3(V_2(t+\tau) - V_n(t+\tau)) \tag{30.13}$$

Solving this equation gives

$$V_2(t+\tau) = \frac{V_2(t)}{(A+1)} \tag{30.14}$$

Inserting all necessary equations in Eq. (30.11) gives the following transfer function:

$$V_2(z) = -\frac{C_1}{C_2 + \frac{1}{A}(C_1 + C_2 + C_3)} \frac{(zV_1(z) - V_{os}(z))}{z - 1 + \frac{\frac{C_1}{A+1}}{C_2(A+1) + C_1 + C_3}} \tag{30.15}$$

b) Yes it is insensitive to parasitics.

Parasitics:

C_{pa} is connected to an ideal voltage source is will not affect the transfer function.

C_{pb} is connected between ground and virtual ground or ground and ground so it will not affect the transfer function.

C_{pc} is connected between ground and virtual ground so it will not affect the transfer function

C_{pd} is either connected to the output of the OTA or it will not be connected so it will not affect the transfer function.

C_{pe} is connected to the output of the OTA and thereby not change the transfer function.

8.6. Switched capacitor circuit 4

31. Switched capacitor circuit.

a) See solution e)

b) Yes it is insensitive to parasitics. All parasitics are shown in Figure 63.

Parasitics:

C_{pa} are connected to an ideal voltage source is will not be affected.

C_{pb} are connected between ground and virtual ground so it will not be affected.

C_{pc} are connected to the output of the ideal OTA, so it will not be affected.

C_{pd} are either connected to the output of the OTA or a node which has a constant voltage. Hence, it will not affect the transfer function.

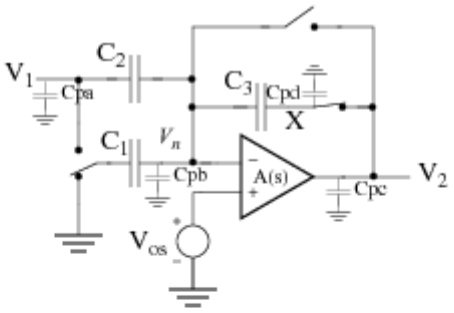


Figure 63: The SC circuit with parasitics.

c) The output from the SC-circuit is shown in Figure 64. Every other output

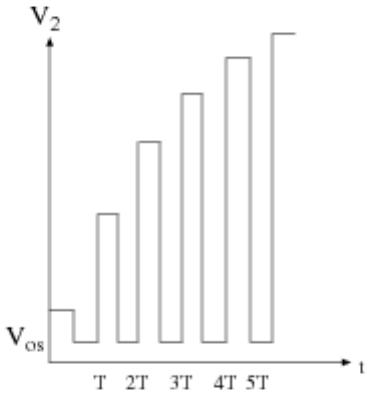


Figure 64: The output voltage as a function of the time.

(T/2) the output voltage will be V_{os}.

d) The circuit is insensitive to parasitics so the transfer function will not change. The speed of the circuit will decrease since a larger load is applied to the output of the amplifier.

e) Assume that at time t the circuit is in the state as shown in Figure 65.

During time t, t+2τ , t+4τ and so on, vi see that

$$V_2(t+2n\tau) = (V_{os}(t) - V_n(t+2n\tau))A \tag{31.1}$$

$$V_2(t+(2n+1)\tau) = (V_{os}(t) - V_2(t+(2n+1)\tau))A \tag{31.2}$$

Eq. (31.1) gives

$$V_n(t+2n\tau) = V_{os}(t) - \frac{V_2(t+2n\tau)}{A} \tag{31.3}$$

Eq. (31.2) gives

$$V_n(t+(2n+1)\tau) = \frac{V_{os}(t)}{1+\frac{1}{A}} \tag{31.4}$$

Use charge redistribution analysis

During time t:

$$q_1(t) = C_1\left(0 - V_{os}(t) + \frac{V_2(t)}{A}\right) \tag{31.5}$$

$$q_2(t) = C_2\left(V_1(t) - V_{os}(t) + \frac{V_2(t)}{A}\right) \tag{31.6}$$

$$q_3(t) = C_3\left(V_2(t) - V_{os}(t) + \frac{V_2(t)}{A}\right) \tag{31.7}$$

During time $t+\tau$ ($V_{os}(t+\tau) = V_{os}(t)$):

$$q_1(t+\tau) = C_1\left(V_1(t+\tau) - \frac{V_{os}(t)}{1+\frac{1}{A}}\right) \tag{31.8}$$

$$q_2(t+\tau) = C_2\left(V_1(t+\tau) - \frac{V_{os}(t)}{1+\frac{1}{A}}\right) \tag{31.9}$$

$$q_3(t+\tau) = q_3(t) \tag{31.10}$$

The charge across capacitor 3 is constant from time t to t+τ since it is not connected anywhere.

During time $t+2\tau$ ($V_{os}(t+2\tau) = V_{os}(t)$):

$$q_1(t+2\tau) = C_1\left(0 - V_{os}(t) + \frac{V_2(t+2\tau)}{A}\right) \tag{31.11}$$

$$q_2(t+2\tau) = C_2\left(V_1(t+2\tau) - V_{os}(t) + \frac{V_2(t+2\tau)}{A}\right) \tag{31.12}$$

$$q_3(t+2\tau) = C_3\left(V_2(t+2\tau) - V_{os}(t) + \frac{V_2(t+2\tau)}{A}\right) \tag{31.13}$$

Charge conservation:

$$q_1(t+\tau)+q_2(t+\tau)+q_3(t+\tau) = q_1(t+2\tau)+q_2(t+2\tau)+q_3(t+2\tau)$$

Inserting the above equations in the charge conservation equation and then a Z-transformation gives the transfer function (Z-transform of $V_{os}(t) = V_{os}(z)$)

$$V_2(z) = \frac{1}{C_3\left(1+\frac{1}{A}\right)+\frac{C_1+C_2}{A}} \cdot \frac{\left((C_1+C_2)z^{\frac{1}{2}}-C_2 z\right)V_1(z)+V_{os}(z)\frac{C_1+C_2}{1+A}}{z-\frac{C_3\left(1+\frac{1}{A}\right)}{C_3\left(1+\frac{1}{A}\right)+\frac{C_1+C_2}{A}}} \tag{31.14}$$

The solution for exercise a) is obtained by letting $A \to \infty$

$$V_2(z) = \frac{1}{C_3}\frac{(C_1+C_2)z^{\frac{1}{2}}-C_2 z}{z-1}V_1(z) \tag{31.15}$$

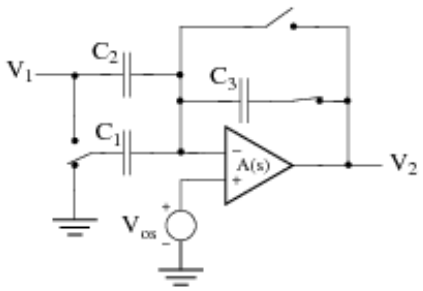


Figure 65: The switched capacitor circuit.

8.7. Switched capacitor circuit 5

32. Switched capacitor circuit.

a) The SC circuit in the different clock phases are shown in Figure 66. We do a charge redis-

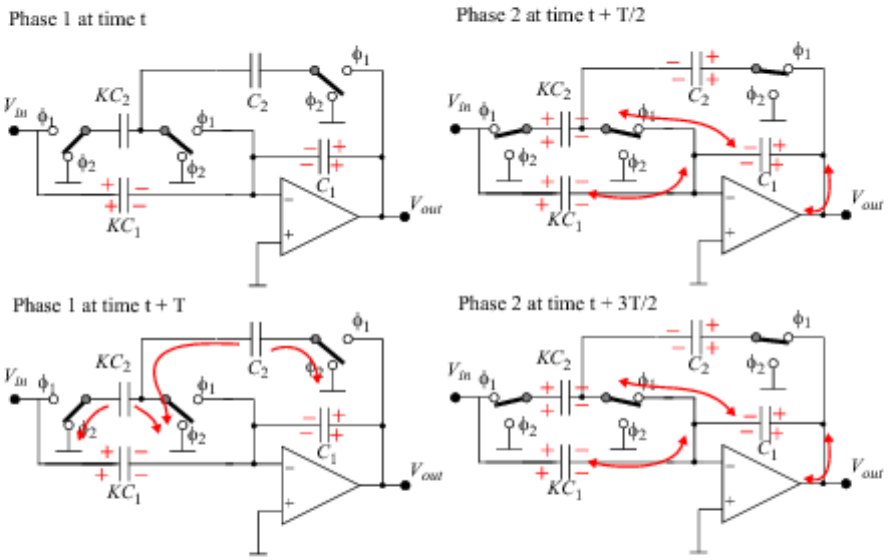


Figure 66: Switched capacitor circuit in different phases

tribution analysis. First we state the initial conditions of the circuit.

Phase 1 at time t

$$q_1(t) = v_{out}(t) \cdot C_1; \tag{32.1}$$

$$q_2(t) = 0 \tag{32.2}$$

$$q_{2K}(t) = 0 \tag{32.3}$$

$$q_{1K}(t) = v_{in}(t) \cdot K \cdot C_1 \tag{32.4}$$

Phase 2 at time $t + T/2$

$$q_1(t+T/2) = v_{out}(t+T/2) \cdot C_1 \tag{32.5}$$

$$q_2(t+T/2) = v_{out}(t+T/2) \cdot C_2 \tag{32.6}$$

$$q_{2K}(t+T/2) = v_{in}(t+T/2) \cdot K \cdot C_2; \tag{32.7}$$

$$q_{1K}(t+T/2) = v_{in}(t+T/2) \cdot K \cdot C_1 \tag{32.8}$$

The charge on the negative input node of the OP ($q_1(t) + q_{1K}(t)$) is distributed between all four capacitances, i.e,

$$q_1(t) + q_{1K}(t) = q_1(t+T/2) + q_2(t+T/2) + \ldots \\ \ldots + q_{1K}(t+T/2) + q_{2K}(t+T/2) \tag{32.9}$$

Phase 1 at time $t + T$

$$q_1(t+T) = v_{out}(t+T)\cdot C_1\,;\; q_2(t+T) = 0\,; \tag{32.10}$$

$$q_{1K}(t+T) = v_{in}(t+T)\cdot C_1\cdot K\,;\; q_{2K}(t+T) = 0 \tag{32.11}$$

and we get a charge conservation because no charge can leave the negative input node of the OP.

$$q_1(t+T)+q_{1K}(t+T) = q_1(t+T/2)+q_{1K}(t+T/2) \tag{32.12}$$

Phase 2 at time $t+3T/2$

$$q_1(t+3T/2) = v_{out}(t+3T/2)\cdot C_1\,;$$
$$q_2(t+3T/2) = v_{out}(t+3T/2)\cdot C_2 \tag{32.13}$$

$$q_{2K}(t+3T/2) = v_{in}(t+3T/2)\cdot K\cdot C_2\,;$$
$$q_{1K}(t+3T/2) = v_{in}(t+3T/2)\cdot K\cdot C_1 \tag{32.14}$$

The charge on the negative input node of the OP is distributed between all four capacitances, i.e,

$$q_1(t+T)+q_{1K}(t+T) = q_1(t+3T/2)+q_2(t+3T/2)+\ \ldots$$
$$\ldots\ +q_{1K}(t+3T/2)+q_{2K}(t+3T/2) \tag{32.15}$$

By combining Eq. (32.12) with Eq. (32.15) we get

$$q_1(t+T/2)+q_{1K}(t+T/2) = q_1(t+3T/2)+q_2(t+3T/2)+\ \ldots$$
$$\ldots\ +q_{1K}(t+3T/2)+q_{2K}(t+3T/2) \tag{32.16}$$

which is equal to

$$v_{out}(t+T/2)\cdot C_1+v_{in}(t+T/2)\cdot C_1\cdot K = v_{out}(t+3T/2)\cdot C_1+$$
$$(v_{out}(t+3T/2)\cdot C_2+v_{in}(t+T/2)\cdot C_2\cdot K+v_{in}(t+T/2)\cdot C_1\cdot K) \tag{32.17}$$

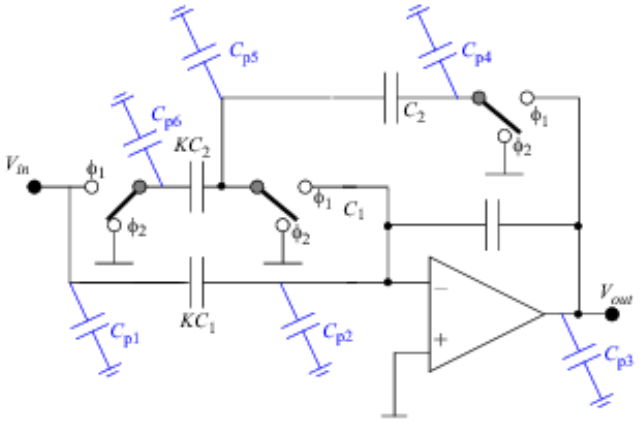
by using the z-transform we finally get the transfer function

$$\frac{V_{out}(z)}{V_{in}(z)} = \frac{K(z(C_2+C_1)-C_1)}{-(z(C_2+C_1)-C_1)} = -K \tag{32.18}$$

, i.e., an inverting amplifier.

b) To see if the circuit is sensitive to parasitics we examine all the parasitic capacitances and

check whether they can destroy the operation.



C_{p1} ... will not affect the transfer function because it is always connected to the input node.

C_{p2} ... is shorted between ground a virtual ground.

C_{p3} ... will not affect the transfer function because it is always connected to the output node.

C_{p4} ... is either shorted or connected to the output node and will never contribute to the output.

C_{p5} ... is either shorted to ground or virtual ground.

C_{p6} ... is either shorted or connected to the input node and will never contribute to the output.

, i.e., the circuit is insensitive to parasitics.

c) If the switch transistors would have a non-negligible on-resistance the charging/discharging through them would not be instantaneously. This affects the speed of the circuit and not the transfer function. To compensate for this problem one have to make sure that we are using non-overlapping switching signals and that they are slow enough so that the circuit has time to settle properly.

8.8. SC circuit (K25)

Example Charge I (K25)

Derive the transfer function and discuss the sensitivity of the circuit. Values are

$$C_1 = C_2 \text{ and } C_1 = 1.12C_2$$

Consider the start-up conditions at time t. The charge at C_1 and C_2 is

$$q_1(t) = 0 \text{ and } q_2(t) = C_2 v_2(t)$$

C_1 is coupled between ground and virtual ground (OPamp input). The charge must be zero.

Time $t+\tau$. Switches have changed.

C_1 is charged by the voltage $v_1(t+\tau)$ and the output of the OPamp, v_2, that adds extra charge. The charge at C_1 becomes

$$q_1(t+\tau) = C_1[v_1(t+\tau) - v_2(t+\tau)]$$

Note the chosen sign of the charge. For C_2 we have

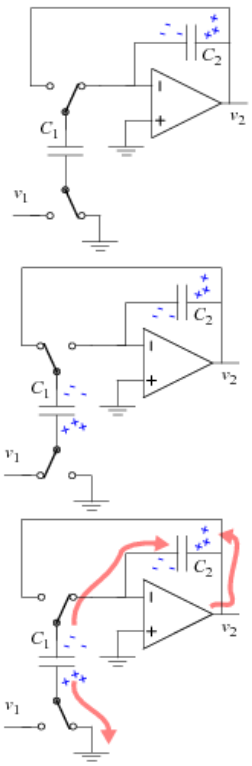
$$q_2(t+\tau) = C_2 v_2(t+\tau).$$

On the negative plate, the charge is stored.

$$q_2(t+\tau) = q_2(t) \text{ dvs } v_2(t+\tau) = v_2(t)$$

(No charge can disappear from the input of the OPamp if it is unconnected).

At time $t+2\tau$ the switches are closed. C_1 is again connected to ground and virtual ground, which empties C_1. The positive charge leaks down to ground, the negative charge is redistributed to the negative plate of C_2. The extra charge needed to compensate the positive plate of C_2 is taken from the OPamp output.



The charge at C_1 and C_2 must be

$$q_1(t+2\tau) = 0 \text{ and } q_2(t+2\tau) = C_2 v_2(t+2\tau)$$

Charge conservation gives (at the negative plate of C_2)

$$-q_2(t+2\tau) = -q_2(t+\tau) + (-q_1(t+\tau)) = -q_2(t) - q_1(t+\tau)$$

This gives

$$C_2 v_2(t+2\tau) = C_2 v_2(t) + C_1[v_1(t+\tau) - v_2(t+\tau)] =$$
$$= C_2 v_2(t+\tau) + C_1[v_1(t+\tau) - v_2(t+\tau)]$$

We also see that

$$v_2(t+2\tau) = v_2(t+3\tau)$$

which gives

$$C_2 v_2(t+3\tau) - C_2 v_2(t+\tau) + C_1 v_2(t+\tau) = C_1 v_1(t+\tau)$$

z-transform, with $t = kT$ and $2\tau = T$

$$[C_2 z^{3/2} - C_2 z^{1/2} + C_1 z^{1/2}] V_2(z) = C_1 z^{1/2} V_1(z)$$

which gives the transfer function

$$H(z) = \frac{V_2(z)}{V_1(z)} = \frac{C_1}{C_2} \cdot \frac{z^{1/2}}{z^{3/2} - (1 - C_1/C_2)} = \frac{C_1}{C_2} \cdot \frac{1}{z - (1 - C_1/C_2)}$$

If the capacitances are equally large, $C_1 = C_2$, the circuit is a simple delay element, (sample-and-hold)

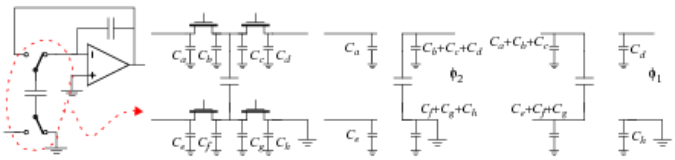
$$H(z) = z^{-1}$$

In the second case, $C_1 = 1.12C_2$, the transfer function becomes

$$H(z) = \frac{1.12}{z + 0.12}$$

This is used to compensate for the sinc weighting of the signal.

Example parasitics I



The parasitic capacitances are associated with all nodes in the circuit. Consider the parasitic capacitances, C_a through C_h. They are the parasitic capacitances associated with the switches as discussed earlier.

During clock phase ϕ_2, C_b, C_c and C_d are coupled in parallel. The same is true for C_f, C_g and C_h. C_a is connected to the output of the OPamp. C_e is connected to the input signal. The previous charge at the capacitances coupled in parallel will redistribute to C_2.

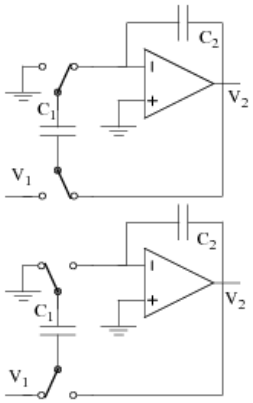
During clock phase ϕ_1, C_a, C_b and C_c are coupled in parallel. The same is true for C_e, C_f and C_g. C_d is coupled to virtual ground at the OPamp input. C_h is connected to ground. The parallel capacitances will be charged and during next clock phase this charge redistribute and affect the transfer function.

Note that C_h and C_d always are connected to ground or virtual ground and will therefore not affect the transfer function. While the input signal is directly connected to C_1 the capacitances

8.9. SC circuit (K26)

C_e, C_f, C_g, C_h will not affect the transfer function.

Example Charge II (K26)



Consider time t. Charge at C_1 and C_2 is

$$q_1(t) = C_1 v_2(t) \text{ and } q_2(t) = C_2 v_2(t)$$

At $t+\tau$ C_1 is charged with $v_1(t)$

$$q_1(t+\tau) = C_1 v_1(t+\tau)$$

C_2 conserves its charge

$$q_2(t) = C_2 v_2(t) = q_2(t+\tau) = C_2 v_2(t+\tau)$$

At time $t+2\tau$ C_1 is switched

$$q_1(t+2\tau) = C_1 v_2(t+2\tau)$$

The charge at C_1 is redistributed between C_2 and C_1 in such a way that the total charge is conserved

$$q_1(t+2\tau) + q_2(t+2\tau) = q_1(t+\tau) + q_2(t+\tau)$$

$$C_1 v_2(t+2\tau) + C_2 v_2(t+2\tau) =$$

$$= C_1 v_1(t+\tau) + C_2 v_2(t+\tau) = (C_1 + C_2) v_2(t+2\tau)$$

At time $t+3\tau$. The charge at C_2 is conserved.

$$v_2(t+3\tau) = v_2(t+2\tau)$$

This is concluded into

$$(C_1 + C_2) v_2(t+3\tau) - C_2 v_2(t+\tau) = C_1 v_1(t+\tau)$$

Let $t = kT$ and $T = 2\tau$, z-transform

$$(z^{3/2}(C_1 + C_2) - z^{1/2} C_2) V_2(z) = C_1 z^{1/2} V_1(z)$$

This gives the transfer function

$$H(z) = \frac{V_2(z)}{V_1(z)} = \frac{C_1}{z(C_1 + C_2) - C_2} = \frac{C_1/(C_1 + C_2)}{z - C_2/(C_1 + C_2)}$$

C_1 must be much larger than C_2, $C_1 \gg C_2$, to achieve a sample-and-hold cirucit

$$H(z) = z^{-1}$$

Example parasitics II

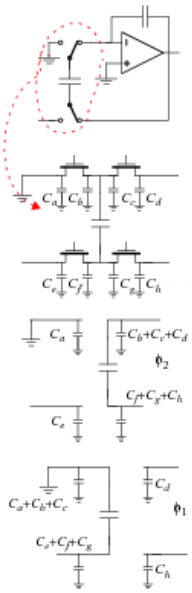
Consider the parasitic capacitances C_a through C_h.

During clock phase ϕ_2, C_b, C_c and C_d are coupled in parallel. The same is true for C_f, C_g and C_h. C_a is short and C_e is connected to the input signal.

The charge on the parallel capacitances will redistribute to C_2.

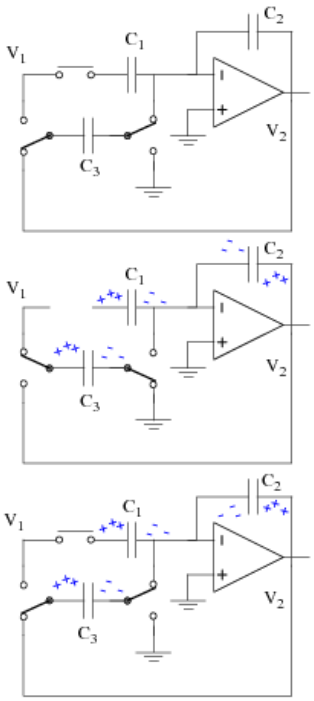
During clock phase ϕ_1, C_a, C_b and C_c are coupled in parallel. The same is true for C_e, C_f and C_g. C_d is coupled to the input of the OPamp. C_h is connected to the output of the OPamp.

Now note that C_a, C_b, C_c and C_d always are connected to ground or virtual ground, hence always short and will not affect the transfer function. The charge on C_1's plate connected to the input of the OPamp determines the transfer function. While the input signal is directly connected to C_1 neither will the capacitances C_e, C_f, C_g, or C_h affect the transfer function.



8.10. SC circuit (K27)

Exercise K27



At time t the charge is discribed by

$$q_1(t) = C_1 v_1(t)$$
$$q_2(t) = C_2 v_2(t)$$
$$q_3(t) = C_3 v_2(t)$$

At time $t+\tau$:

Charge at C_1 and C_2

$$q_1(t+\tau) = q_1(t)$$
$$q_2(t+\tau) = q_2(t)$$

C_3 is charged with the input voltage

$$q_3(t+\tau) = C_3 v_1(t+\tau)$$

At time $t+2\tau$:

Total charge on the three capacitances is

$$q_1(t+2\tau)+q_2(t+2\tau)+q_3(t+2\tau)$$

where

$$q_1(t+2\tau) = C_1 v_1(t+2\tau)$$
$$q_2(t+2\tau) = C_2 v_2(t+2\tau)$$
$$q_3(t+2\tau) = C_3 v_2(t+2\tau)$$

The total charge must be conserved, no charge disappears from the input of the OPamp:

$$q_1(t+2\tau)+q_2(t+2\tau)+q_3(t+2\tau) =$$
$$= q_1(t+\tau)+q_2(t+\tau)+q_3(t+\tau) =$$
$$= q_1(t)+q_2(t)+q_3(t+\tau)$$

Use the charge expression, and we have

$$(C_2+C_3)v_2(t+2\tau)+C_1 v_1(t+2\tau) = C_1 v_1(t)+C_2 v_2(t)+C_3 v_1(t+\tau)$$

which gives

$$v_2(t+2\tau)-\frac{C_2}{C_2+C_3}v_2(t) = \frac{C_1}{C_2+C_3}\left[v_1(t)+\frac{C_3}{C_1}v_1(t+\tau)-v_1(t+2\tau)\right]$$

Let $t = kT$ and $T = 2\tau$. z-transform

$$H(z) = \frac{V_2(z)}{V_1(z)} = \frac{C_1}{C_2+C_3}\frac{1+\frac{C_3}{C_1}z^{1/2}-z}{z-\frac{C_2}{C_2+C_3}} = -\frac{C_1}{C_2+C_3}\frac{z-\left(1+\frac{C_3}{C_1}z^{1/2}\right)}{z-\frac{C_2}{C_2+C_3}}$$

We now see that the output signal is affected by the input signal at each half clock period. Two ways can be used to design a first-order all pass filter.

1) Eliminate $z^{1/2}$ by assuming $v_1(t) = v_1(t+\tau)$ which gives $z^{1/2}V_1(z) = V_1(z)$

2) Eliminate $z^{1/2}$ by assuming $v_1(t+\tau) = v_1(t+2\tau)$ which gives $z^{1/2}V_1(z) = zV_1(z)$

this gives

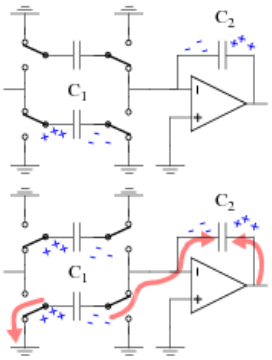
$$H_1(z) = -\frac{C_1}{C_2+C_3}\cdot\frac{z-\frac{C_1+C_3}{C_1}}{z-\frac{C_2}{C_2+C_3}} \text{ or } H_2(z) = -\frac{C_1}{C_2+C_3}\cdot\left(1-\frac{C_3}{C_1}\right)\frac{z-\frac{1}{1-C_3/C_1}}{z-\frac{C_2}{C_2+C_3}}$$

For an all pass filter, if the pole is given by $z = p$, the zero is given by $z = 1/p$. This gives

$$\frac{C_1+C_3}{C_1} = \frac{C_2+C_3}{C_2} \Rightarrow C_2 = C_1 \text{ or } 1-\frac{C_3}{C_1} = \frac{C_2}{C_2+C_3} \Rightarrow C_1 = C_2+C_3$$

8.11. SC circuit (K28)

Exercise K28



At time t the lower C_1 is charged

$$q_{N1}(t) = C_1 v_1(t)$$

The upper is shorted.

$$q_{U1}(t) = 0$$

At time $t+\tau$ the upper C_1 is charged

$$q_{U1}(t+\tau) = C_1 v_1(t+\tau)$$

The lower is shorted. The charge will however redistribute to the negative plate at C_2. The positive plate at C_2 will get extra charge from the output of the OPamp. The charge at C_2 is written as

$$q_2(t+\tau) = C_2 v_2(t+\tau) = q_2(t) + q_{N1}(t) = \\ = C_2 v_2(t) + C_1 v_1(t)$$

At time $t+2\tau$ the operation is practical the same due to the symmetrical capacitances.

$$q_2(t+2\tau) = C_2 v_2(t+2\tau) = q_2(t+\tau) + q_{U1}(t+\tau) = C_2 v_2(t+\tau) + C_1 v_1(t+\tau)$$

We see that the input signal is delayed and switched to the output at every half clock cycle. We have

$$v_2(t+2\tau) = v_2(t) + \frac{C_1}{C_2}[v_1(t+\tau) + v_1(t)]$$

And the transfer function is

$$H(z) = \frac{C_1}{C_2} \cdot \frac{z^{1/2}+1}{z-1}$$

If we now once again assume that $v_1(t) = v_1(t+\tau)$ or $v_1(t+\tau) = v_1(t+2\tau)$, then

$$H(z) = \frac{C_1}{C_2} \cdot \frac{2z^{-1}}{1-z^{-1}} \text{ or } H(z) = \frac{C_1}{C_2} \cdot \frac{1+z^{-1}}{1-z^{-1}}$$

8.12. Clock feedthrough (K29)

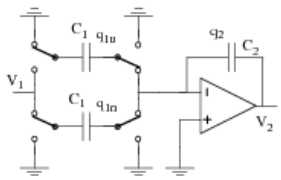
TBD Solutions to be added.

8.13. Switch sharing (K30)

TBD Solutions to be added.

8.14. SC circuit (K37)

Exercise K37



At time t. The upper capacitor is shorted between ground and virtual ground and the lower capacitor is charged with the input voltage:

$$q_{1u}(t) = 0 \text{ and } q_{1n}(t) = C_1 v_1(t)$$

C_2 has the charge:

$$q_2(t) = C_2 v_2(t)$$

At time $t+\tau$. The upper capacitor is charged.

$$q_{1u}(t+\tau) = C_1 v_1(t+\tau)$$

The lower capacitor is shorted, all charge is lost to the ground.

$$q_{1n}(t+\tau) = 0$$

The charge in C_2 is conserved since no charge can disappear from the input of the OPamp.

$$q_2(t+\tau) = q_2(t) \text{ dvs } C_2 v_2(t+\tau) = C_2 v_2(t) \text{ dvs } v_2(t+\tau) = v_2(t)$$

Time $t+2\tau$. The upper capacitor is discharged, but its charge will be redistributed over the lower capacitor and C_2. The redistribution is determined by the input voltage. We have

$$q_{1u}(t+2\tau) = 0,\ q_{1n}(t+2\tau) = C_1 v_1(t+2\tau),\ q_2(t+2\tau) = C_2 v_2(t+2\tau)$$

and

$$-q_{1n}(t+2\tau) + (-q_2(t+2\tau)) = -q_{1u}(t+\tau) + (-q_2(t+\tau))$$

Which gives

$$C_1 v_1(t+2\tau) + C_2 v_2(t+2\tau) = C_1 v_1(t+\tau) + C_2 v_2(t+\tau) = C_1 v_1(t+\tau) + C_2 v_2(t)$$

The input signal is sampled-and-held as

$$v_1(t+\tau) = v_1(t)$$

which gives

$$C_1 v_1(t+2\tau) + C_2 v_2(t+2\tau) = C_1 v_1(t) + C_2 v_2(t)$$

z-transform

$$C_1 \cdot (z-1) \cdot V_1(z) = C_2 \cdot (1-z) \cdot V_2(z)$$

and

$$H(z) = \frac{V_1(z)}{V_2(z)} = -\frac{C_2}{C_1} \cdot \frac{z-1}{z-1} = -\frac{C_2}{C_1}$$

The circuit is an inverting amplifier. Practically, however, a pole on the unit circle can not be cancelled by a zero. The circuit has to be used in a feedback loop.

8.15. Signal switching (K39)

TBD Solutions to be added.

8.16. Sampled noise (K24)

TBD Solutions to be added.

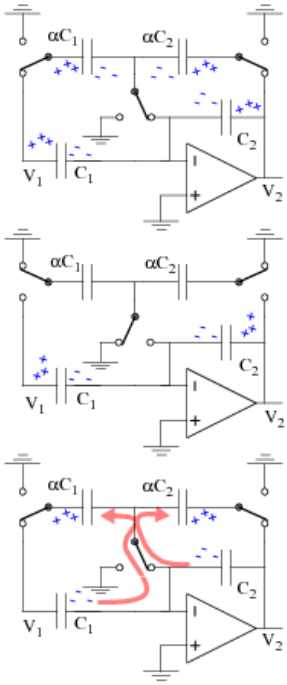
EXERCISE SECTION 9: SC FILTERS

9.1. SC filter building blocks (K36)

Exercises

Exercise K36

Derive the transfer function $H(z)$.



At time t the charge at the transistors is written as

$$q_1(t) = C_1 v_1(t)$$
$$q_2(t) = C_2 v_2(t)$$
$$q_{\alpha 1}(t) = \alpha C_1 v_1(t)$$
$$q_{\alpha 2}(t) = \alpha C_2 v_2(t)$$

At $t+\tau$, αC_1 and αC_2 are completely shorted. The total charge on C_1 and C_2 must however be conserved, while no charge can disappear from the input of the OPamp. Changes of the input signal will determine how the charge is distributed between C_1 and C_2:

$$q_1(t+\tau) + q_2(t+\tau) = q_1(t) + q_2(t)$$
$$q_{\alpha 1}(t+\tau) = q_{\alpha 2}(t+\tau) = 0$$

At $t+2\tau$ we use the same result. No charge disappears from the OPamp input. It has to redistribute to the other (previously discharged) capacitances:

$$\begin{aligned} q_1(t+\tau) + q_2(t+\tau) &= \\ &= q_1(t+2\tau) + q_2(t+2\tau) + \\ &+ q_{\alpha 1}(t+2\tau) + q_{\alpha 2}(t+2\tau) \\ &= q_1(t) - q_2(t) \end{aligned}$$

This gives

$$C_1 v_1(t) + C_2 v_2(t) = (1+\alpha) C_1 v_1(t+2\tau) + (1+\alpha) C_2 v_2(t+2\tau)$$

Let $t = kT$ and $2\tau = T$. z-transform and the transfer function is

$$H(z) = \frac{V_2(z)}{V_1(z)} = -\frac{C_1}{C_2} \cdot \frac{(1+\alpha)z - 1}{(1+\alpha)z - 1} = -\frac{C_1}{C_2} \cdot \frac{z - \frac{1}{1+\alpha}}{z - \frac{1}{1+\alpha}} = -\frac{C_1}{C_2}$$

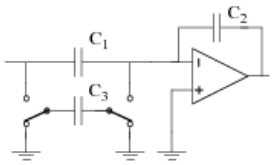
which is an inverting amplifier. The pole is cancelled by the zero.

9.2. Bilinear integrator (K38)

Exercise K38

General transfer function for bilinear integrator:

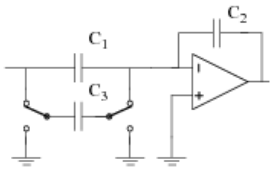
$$H(z) = K \cdot \frac{z-1}{z+1}$$



At time t the charge distribution is

$$q_1(t) = C_1 v_1(t)$$
$$q_2(t) = C_2 v_2(t)$$
$$q_3(t) = 0 \text{ (shorted)}$$

At time $t+\tau$ C_3 is coupled in parallel with C_1 and will take charge from C_2 and C_1:



$$q_1(t+\tau) = C_1 v_1(t+\tau)$$
$$q_2(t+\tau) = C_2 v_2(t+\tau)$$
$$q_3(t+\tau) = C_3 v_1(t+\tau)$$

The charge distribution will be

$$q_1(t+\tau) + q_2(t+\tau) + q_3(t+\tau) = q_1(t) + q_2(t)$$

At time $t+2\tau$ the total charge at C_1 and C_2 is conserved. It will though redistribute due to the change of input voltage.

$$q_1(t+\tau) + q_2(t+\tau) = q_1(t+2\tau) + q_2(t+2\tau)$$

Concludingly, we have

$$q_1(t) + q_2(t) = q_3(t+\tau) + q_1(t+2\tau) + q_2(t+2\tau), \text{ i.e.,}$$
$$C_1 v_1(t) - C_1 v_1(t+2\tau) - C_3 v_1(t+\tau) = C_2[v_2(t+2\tau) - v_2(t)]$$

which gives

$$v_2(t+2\tau) - v_2(t) = -\frac{C_1}{C_2}\left[v_1(t+2\tau) + \frac{C_3}{C_1} v_1(t+\tau) - v_1(t)\right]$$

Suppose $v_1(t) = v_1(t+\tau)$, hence a sample-and-hold circuit at the input, which eliminated the $z^{1/2}$-term in the transfer function. Let $t = kT$ and $2\tau = T$. z-transform

$$H(z) = \frac{V_2(z)}{V_1(z)} = -\frac{C_1}{C_2} \cdot \frac{z + (C_3/C_1 - 1)}{z-1}$$

Choosee $C_3 = 2C_1$ and we have

$$H(z) = -\frac{C_1}{C_2} \cdot \frac{1+z^{-1}}{1-z^{-1}}$$

9.3. LDI transform (K31)

TBD Solutions to be added.

9.4. LDI transform (K32)

TBD Solutions to be added.

9.5. SC filter 1

TBD Solutions to be added.

9.6. Filter scaling (K23)

TBD Solutions to be added.

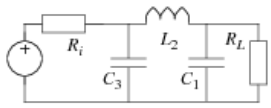
9.7. LDI SC filter (K33)

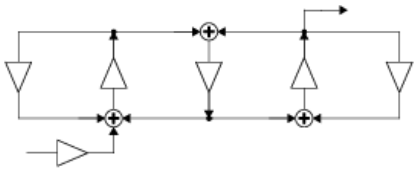
Exercise K33

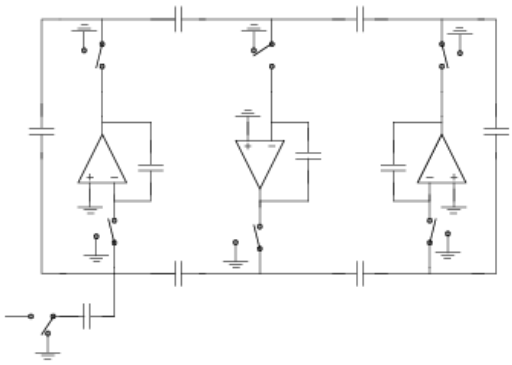
The order is found to be $N = 3$. Values are

$C_{3n} = 1$, $L_{2n} = 2$, $C_{1n} = 1$ and

$R_i = R_L = 1k\Omega$







9.8. SC elliptic filter (K34)

Exercise K34

Due to the fact that

$$R = R_i = R_L$$

we know that the dc gain is $1/2$

You can also see that the filter is realizing a third order elliptic low pass filter. Suppose that the maximum output value is given by dc voltage. This implies that we directly can choose the scaling parameter k_1 in such a way that all nodes in the net become scaled with a factor two, hence $k_1 = 2$.

9.9. SC filter (K35)

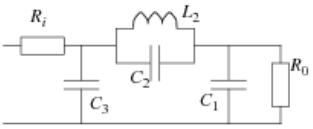
Exercises

Exercise K35

Third order low pass filter with an elliptic reference filter. The specification gives

$f_c = 3.4kHz$, $A_{max} = 0.02\,\text{dB}$,

$f_{sample} = 128kHz$,



Normalized values from table are:

$$R_i = R_0 = 1k\Omega,\ C_{1,n} = C_{3,n} = 0.5275,\ C_{2,n} = 0.1921,\ L_{2,n} = 0.7700$$

LDI transformation gives

$$s = s_0 \cdot \frac{1 - z^{-1}}{z^{-1/2}} \text{ where } s_0 = \frac{\omega_{ac}}{2\sin(\omega_c T/2)}$$

Denormalize the values.

Compensate for the LDI transformation errors.

Find the flow graph

Use standard SC integrators.

Identify the values

9.10. SC filter (K40)

Example Exercise K40

Synthesize an LDI filter. Transformation give

$$s = s_0 \frac{z-1}{z^{1/2}}$$

The specification on the reference filter angular cut-off frequency is chosen to be

$$\omega_c = 2\pi \cdot 1500 \text{ rad/s}$$

Since sampling frequency is $f_s = 40\text{kHz}$ we have the discrete-time cut-off frequency as

$$\Omega_c = \frac{1.5k}{40k} \cdot 2\pi \approx 0.2356$$

and the discrete-time stop-band frequency as

$$\Omega_s = \frac{2.5k}{40k} \cdot 2\pi \approx 0.3927$$

From this we have s_0

$$s_0 = \frac{\omega_c}{2\sin(\Omega_c/2)} =$$

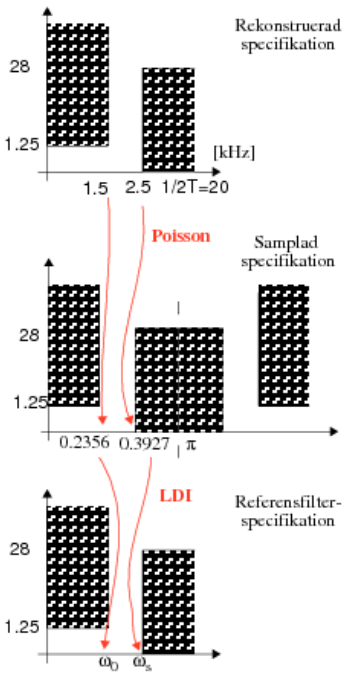
$$= \frac{3000\pi}{2\sin(0.2356/2)} \approx 40.093 \text{ krad/s}$$

We find the ω_s

$$\omega_0 = 2s_0 \sin(\Omega_s/2) \approx$$

$$\approx 2 \cdot 40.093 \cdot \sin(0.3927/2) \approx$$

$$\approx 15.643 \text{ krad/s}$$



Design an elliptic filter. Order is found to be $N = 3$. Suppose the resistors are equal, or

$\kappa^2 = 1$ and choose $R_i = R_0 = 1k\Omega$

The normated values on the components are

$C_{1n} = C_{3n} = 1.9314$, $C_{2n} = 0.3781$ and $L_{2n} = 0.7571$

These are denormalized with

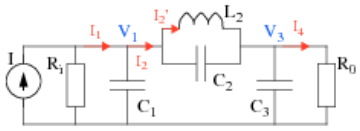
$$L_i = \frac{R_0}{\omega_0} L_{in} \text{ and } C_i = \frac{1}{\omega_0 R_0} C_{in}$$

Which gives

$$C_1 = C_3 = 204.9nF$$

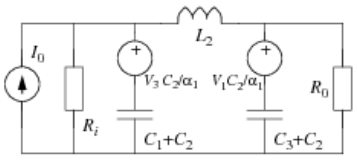
$$L_2 = 80.3mH$$

$$C_2 = 40.1nF$$



The filter is transformed. The constant used in the figure is given by

$$\alpha_1 = C_1 + C_2 = C_2 + C_3$$



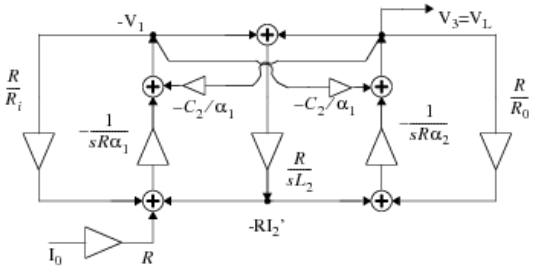
Setting up the wellknown equations for currents and voltages in the filter, we have

$$RI_0 = RI_i - \frac{R}{R_i}V_1$$

$$V_1 = \frac{1}{sRC_1}(RI_0 - RI_2),\ RI_2 = \frac{R}{(sL_2)\,\|\,(1/sC_2)}(V_1 - V_3)$$

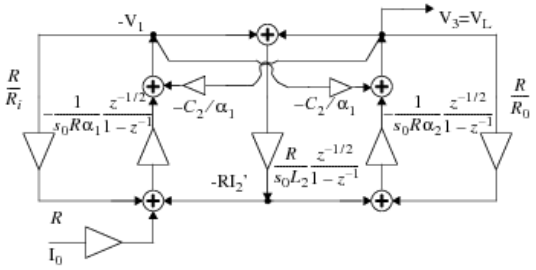
$$V_3 = \frac{1}{sRC_3}(RI_2 - RI_4),\ RI_4 = \frac{R}{R_0}V_3 = \frac{R}{R_0}V_L$$

etc. With this the signal flow graph becomes

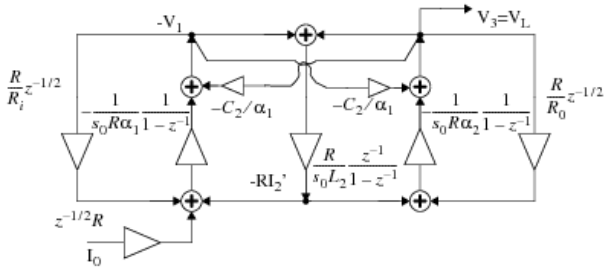


LDI transform by setting

$$s = s_0 \cdot \frac{z-1}{z^{1/2}}$$



Elminate $z^{-1/2}$ in the integrators by propagating backwards.



We now though have $z^{-1/2}$ terms in the outer feedback amplifiers. This is practically not possible to implement. One way to implement this is simply to remove the $z^{-1/2}$ term in the expression:

$$\frac{R}{R_L} \cdot z^{-1/2}$$

We could assume that the original R_L and R_i have the expressions

$$R_L = R_L \cdot z^{-1/2} \text{ and } R_i = R_i \cdot z^{-1/2}$$

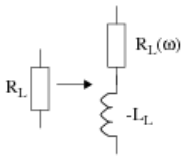
As discussed earlier, $z^{-1/2}$ naturally contains valuable frequency information

$$z^{-1/2} = -j\frac{\omega}{2s_0} + \sqrt{1-\left(\frac{\omega}{2s_0}\right)^2}$$

Thereby

$$R_L \cdot z^{-1/2} = R_L\left[-j\frac{\omega}{2s_0} + \sqrt{1-\left(\frac{\omega}{2s_0}\right)^2}\right] =$$

$$= R_L\sqrt{1-\left(\frac{\omega}{2s_0}\right)^2} - j\omega\frac{R_L}{2s_0} = R_L(\omega) - j\omega L_L$$

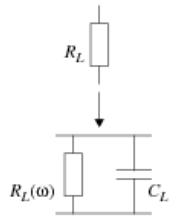


Which is realized by a frequency dependent resistance in series with an inductance, or more useful in this filter implemenation, as a frequency dependet resistance in parallel with a capacitor.

$$R_L \cdot z^{-1/2} = \frac{(R_L(\omega) - j\omega L_L)(R_L(\omega) + j\omega L_L)}{R_L(\omega) + j\omega L_L} =$$

$$= \frac{R_L^2 \cdot 1}{R_L\sqrt{1-(\omega/2s_0)^2} + j\omega R_L/2s_0} =$$

$$= \frac{1}{\frac{1}{R_L/\sqrt{1-(\omega/2s_0)^2}} + \frac{1}{R_L/(j\omega/2s_0)}} = R_L(\omega) \,||\, C_L$$

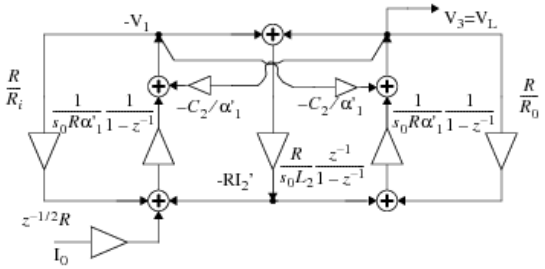


Suppose that C_L is coupled in parallel with C_3 and correspondingly for the inner source resistance C_i is in parallel with C_1. This is corrected by letting the components have the values

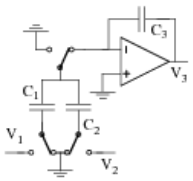
$$C_1' = C_1 - C_i = C_1 - \frac{1}{2s_0R_i} = C_1 - \frac{1}{\omega_0 R_i}\sin\left(\frac{\Omega_0 T}{2}\right) \text{ and}$$

$$C_3' = C_3 - C_L = C_3 - \frac{1}{2s_0R_L} = C_3 - \frac{1}{\omega_0 R_L}\sin\left(\frac{\Omega_0 T}{2}\right)$$

We still have an error that is caused by the fact that we will not implement a frequency dependent resistance. This error is considered to be acceptable. The realization of the filter is given by the flow graph



The two integrators (inverting amplifiers with and without delay) are replaced with their corresponding SC circuits.

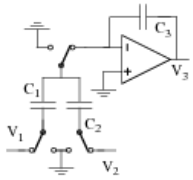


The transfer function of the summing integrator is given by

$$V_3(z) = \frac{z^{-1}}{1-z^{-1}} \cdot \left[\frac{C_1}{C_3} \cdot V_1(z) + \frac{C_2}{C_3} \cdot V_2(z)\right]$$

Check: No direct signal path from input to the output.

The transfer function of the summing and inverting integrator is given by



$$V_3(z) = -\frac{1}{1-z^{-1}} \cdot \left[\frac{C_1}{C_3} \cdot V_1(z) + \frac{C_2}{C_3} \cdot V_2(z)\right]$$

Check: Direct signal path from input to the output.

(Charge that is directed to C_3 is given by a linear combination of the input signals $v_1(t)$ and $v_2(t)$.)

Integrators are used in the realization. The sizes of the capacitors have to be identified. This is done by comparing signal paths in the SC realization with those of the signal flow graph:

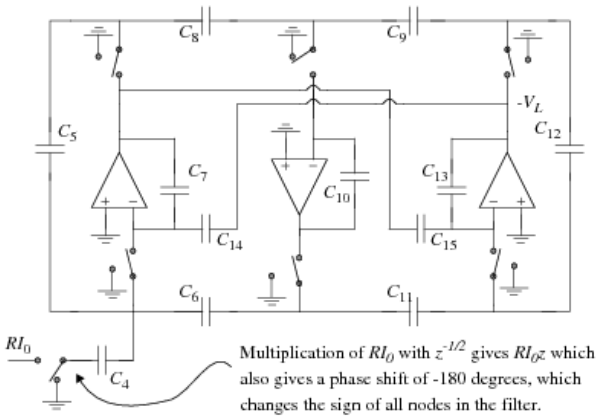
SC filter	Signal Flow Graph	Result
$[-V_1]_E = -\frac{C_4}{C_7}\frac{z^{-1/2}}{1-z^{-1}}$	$[-V_1]_E = -\frac{1}{s_0 R\alpha_1'}\cdot\frac{z^{-1/2}}{1-z^{-1}}$	$\frac{C_4}{C_7} = \frac{1}{s_0 R\alpha_1'}$
$[-V_1]_{-RI_2'} = -\frac{C_6}{C_7}\frac{1}{1-z^{-1}}$	$[-V_1]_{-RI_2'} = -\frac{1}{s_0 R\alpha_1'}$	$\frac{C_6}{C_7} = \frac{1}{s_0 R\alpha_1'}$
$[-V_1]_{-V_3} = -\frac{C_5}{C_7}\frac{1}{1-z^{-1}}$	$[-V_1]_{-V_3} = -\frac{1}{s_0 R\alpha_1'}\frac{R}{R_i} = -\frac{1}{s_0 R_i\alpha_1'}$	$\frac{C_5}{C_7} = \frac{1}{s_0 R_i\alpha_1'}$
$[-RI_2']_{-V_1} = \frac{C_8}{C_{10}}\frac{z^{-1}}{1-z^{-1}}$	$[-RI_2']_{-V_1} = \frac{R}{s_0 L_2}\frac{z^{-1}}{1-z^{-1}}$	$\frac{C_8}{C_{10}} = \frac{R}{s_0 L_2}$
$[-RI_2']_{V_3} = \frac{C_9}{C_{10}}\frac{z^{-1}}{1-z^{-1}}$	$[-RI_2']_{V_3} = \frac{R}{s_0 L_2}\frac{z^{-1}}{1-z^{-1}}$	$\frac{C_9}{C_{10}} = \frac{R}{s_0 L_2}$
$[V_3]_{-RI_2'} = -\frac{C_{11}}{C_{13}}\cdot\frac{1}{1-z^{-1}}$	$[V_3]_{-RI_2'} = -\frac{R}{R_L}\cdot\frac{1}{s_0 RC_3}\cdot\frac{1}{1-z^{-1}}$	$\frac{C_{11}}{C_{13}} = \frac{1}{s_0 R_L\alpha_3'}$
$[V_3]_{V_3} = -\frac{C_{12}}{C_{13}}\frac{1}{1-z^{-1}}$	$[V_3]_{V_3} = -\frac{R}{R_L}\cdot\frac{1}{s_0 RC_3}\cdot\frac{1}{1-z^{-1}}$	$\frac{C_{12}}{C_{13}} = \frac{1}{s_0 R_L\alpha_3'}$

For the feedback we have:

$[-V_1]_{V_3} = -\frac{C_{14}}{C_7}$	$[-V_1]_{V_3} = -\frac{C_2}{\alpha_1'}$	$\frac{C_{14}}{C_7} = \frac{C_2}{\alpha_1'}$
$[V_3]_{-V_3} = -\frac{C_{15}}{C_{13}}$	$[V_3]_{-V_3} = -\frac{C_2}{\alpha_3'}$	$\frac{C_{15}}{C_{13}} = \frac{C_2}{\alpha_3'}$

We assume that

$$R_i = R_L = R$$



Multiplication of RI_0 with $z^{-1/2}$ gives RI_0z which also gives a phase shift of -180 degrees, which changes the sign of all nodes in the filter.

Further, the correction term gives

$$s_0 = \frac{\omega_c}{2\sin(\Omega_c/2)} \text{ and } C_i' = C_i - 1/2s_0R$$

Which yields

$$\frac{C_4}{C_7} = \frac{C_5}{C_7} = \frac{C_6}{C_7} = \left[\frac{\omega_c R(C_1+C_2)}{2\sin(\Omega_c/2)} - \frac{R}{2R}\right]^{-1}, \frac{C_{11}}{C_{13}} = \frac{C_{12}}{C_{13}} = \left[\frac{\omega_c R(C_3+C_2)}{2\sin(\Omega_c/2)} - \frac{R}{2R}\right]^{-1}$$

$$\frac{C_8}{C_{10}} = \frac{C_9}{C_{10}} = \frac{2R\sin(\Omega_c/2)}{\omega_c L_2}$$

$$\frac{C_{14}}{C_{13}} = \frac{C_2}{C_2 + C_1 - \dfrac{\sin(\Omega_c/2)}{R_I\omega_c}} \text{ and } \frac{C_{15}}{C_{13}} = \frac{C_2}{C_2 + C_3 - \dfrac{\sin(\Omega_c/2)}{R_L\omega_c}}$$

With values we have

$$\frac{C_4}{C_7} = \frac{C_5}{C_7} = \frac{C_6}{C_7} = \frac{C_{11}}{C_{13}} = \frac{C_{12}}{C_{13}} = \left[\frac{2\pi\cdot 1500\cdot 1000\cdot(204.9n+40.1n)}{2\sin(0.2356/2)} - \frac{1}{2}\right]^{-1} \approx 0.1072$$

$$\frac{C_8}{C_{10}} = \frac{C_9}{C_{10}} = \frac{2\cdot 1000\cdot\sin(0.2356/2)}{3000\pi\cdot 80.3m} \approx 0.3106$$

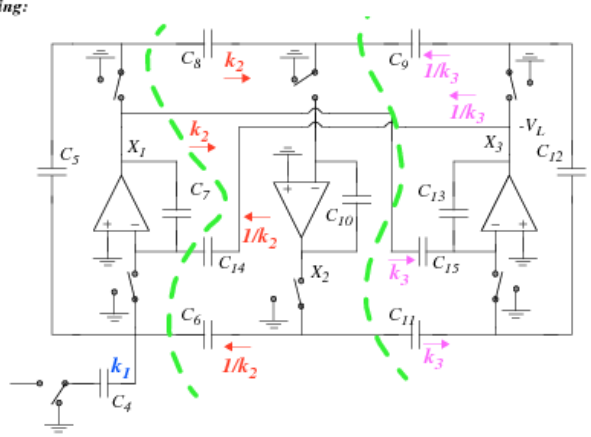
$$\frac{C_{14}}{C_{13}} = \frac{C_{15}}{C_{13}} = \frac{40.1n}{40.1n + 204.9n - \dfrac{\sin(0.2356/2)}{1000\cdot 3000\pi}} \approx 0.1725$$

Choose the integrators' capacitors all equal

$C_7 = C_{10} = C_{13} = 47\,\text{nF}$

From this we have the values of all other capacitors.

Scaling:



Scale the filter so that the relation between the OPamp outputs and the input signal is unity (L_∞-norm). We are scaling the filter to keep the signal levels at wanted levels. The principle of scaling can be described by dividing the net into subnets. The subnets have a number of inputs and outputs. If the inputs are scaled with a constant k_i all nodes of the subnet will be scaled with a factor k_i, as well as we have to scale all outputs with $1/k_i$.

In this case the signal after the first node is scaled to $k_1 X_1$, the second with $k_2 k_1 X_2$ and finally the third (the output) with $k_3 k_2 k_1 X_3$. By changing the values of the capacitances we now can realize the scaling. At C_4 we use $k_1 C_4$ instead. For $C_6 \rightarrow C_6/k_2$, $C_8 \rightarrow C_8 \cdot k_2$, $C_{14} \rightarrow \dfrac{C_{14}}{k_2 k_3}$, $C_{15} \rightarrow C_{15} \cdot k_2 k_3$, $C_9 \rightarrow C_9/k_3$, $C_{11} \rightarrow C_{11} \cdot k_3$ etc.

EXERCISE SECTION 10: DATA CONVERTERS, FUNDAMENTAL

✗ Covered by the main course book. The solutions are found via the course web page.

✗

10.1. D/A swing (Q 11.1 J&M)

For a unipolar D/A converter, all the levels are represented by one single output, i.e., we do not have negative values. The code is offset binary.

A 10-bit converter, will have 2^{10} levels starting from 0 and ending at 2^N-1. This means that the maximum output must be:

$$V_{out,max}=V_{LSB}\cdot\left(2^N-1\right)=1023\cdot 1\ \text{mV}=1.023\ \text{V} \tag{40}$$

10.2. SNR (Q 11.2 J&M)

✗ (Similar to Quiz 5 in the ANIK course 2012).

For any N-bit converter we can write the SNR as

$$\mathrm{SNR} = 6.02 \cdot N + 4.77 - \mathrm{PAR} \tag{41}$$

where $\mathrm{PAR} = P_{pk}/P_{sig}$ is the peak to average ratio for the signal. For a full-scale sinusoidal, this value is 2 (linear scale), i.e., 3 dB. The ADC range is now $V_{ref} = 3$ V, which means that the peak power is

$$P_{pk} = \left(\frac{V_{ref}}{2}\right)^2 = \left(\frac{3}{2}\right)^2 = \frac{9}{4} \tag{42}$$

In the exercise, a sinusoid of 1 Vpp is applied, which means that the signal power is

$$P_{sig} = \frac{1}{2} \cdot \left(\frac{1}{2}\right)^2 = \frac{1}{8} \tag{43}$$

The SNR is thus

$$\mathrm{SNR} = 6.02 \cdot N + 4.77 - 10 \cdot \log_{10}\frac{P_{pk}}{P_{sig}} = 6.02 \cdot 12 + 4.77 - 10 \cdot \log_{10}\frac{9/4}{1/8} \approx 64 \text{ dB} \tag{44}$$

10.3.

10.4.

10.5.

10.6.

10.7. INL/DNL (Q 11.7 J&M)

Measured values are given by:

-0.01, 1.03, 2.02, 2.96, 3.95, 5.02, 6.00, 7.08 V

and ideal values should be

0.00, 1.00, 2.00, 3.00, 4.00, 5.00, 6.00, 7.00 V

Approach 1:

The INL is directly given by the difference between the measured and ideal values, which means that INL is equal to:

-0.01, 0.03, 0.02, -0.04, -0.05, 0.02, 0.00, **0.08**

The DNL is the difference in ideal step between two consecutive values compared to the ideal step (1.00 V):

1.03 - (-0.01) - 1.00 = 0.04
2.02 - 1.03 - 1.00 = -0.01
2.96 - 2.02 - 1.00 = - 0.06
3.95 - 2.96 - 1.00 = -0.01
5.02 - 3.95 - 1.00 = 0.07
6.00 - 5.02 - 1.00 = -0.02
7.08 - 6.00 - 1.00 = **0.08**

The worst-case INL and DNL are given by the absolute max of the values above.

Approach 2: Compensation for gain and offset error

We can compensate for offset and gain error to align the lowest and highest values. The gain error (ideally this should be 0) is

$$G=\underbrace{\frac{7.08-(-0.01)}{1}}_{\text{Real gain}}-\underbrace{\frac{7}{1}}_{\text{Ideal gain}}=0.09 \tag{45}$$

and we find a small offset in the first code, so the offset error is

$$O=-0.01 \tag{46}$$

We can now compensate each value with the gain and offset error according to:

$$V_k = V_{meas} - O - G \cdot \frac{k}{2^N - 1} \tag{47}$$

Now we will get:

0.000, 1.027, 2.004, 2.931, 3.909, 4.966, 5.933, 7.000

With INL

0.000, 0.027, 0.004, -0.069, **-0.091**, -0.034, -0.067, 0.000

and DNL

0.027, -0.023, **-0.073**, -0.022, 0.057, 0.033, 0.067.

The worst-case INL and DNL are given by the absolute max of the values above.

Approach 3: Best-fit compensation

We can assume that offset and gain error can be neglected in some applications. In that case, we want to align according to a best fit line, i.e., not assume that the end values are the correct ones. This implies also that the actual step size is not 1 V anymore.

In this case, the offset and gain errors become

$G = 0.0056$ and $O = -0.0133$

and the compensated values become

0.0033 1.0377 2.0221 2.9565 3.9410 5.0054 5.9798 7.0542

with DNL and INL (referring to the compensated LSB step size, which is $1 + G = 1.0056$).

DNL = 0.0344 -0.0156 -0.0656 -0.0156 0.0644 -0.0256 **0.0744**

INL = 0.0033 0.0377 0.0221 -0.0435 **-0.0590** 0.0054 -0.0202 0.0542

The worst-case INL and DNL are given by the absolute max of the values above.

EXERCISE SECTION 11: DATA CONVERTERS, DAC

✗ Covered by the main course book. The solutions are found via the course web page.

11.1.

11.2.

11.3.

11.4. R-2R ladder DAC (Q 12.11 J&M)

✗ Missing in the manual is that the R_A is the left-most vertical resistor, and R_B is the left-most horizontal resistor. R_C is the right-most vertical resistor.

EXERCISE SECTION 12: DATA CONVERTERS, ADC

✗ Covered by the main course book. The solutions are found via the course web page.

EXERCISE SECTION 13: TRANSMISSION LINES

13.1. Transmission line basics

With higher frequencies the physical distance plays a larger role. From the figure in the exercise, we see that the black (on the top) curve (100 MHz sinusoid) shows a near constant behavior over the 10-cm resistor. One would conclude that the component is lumped (transmission line effects less of concern) for that case.

The book (and lectures) indicate that the physical size should be less than 0.01 of the wavelength to be considered lumped: $l<0.01\,\lambda$.

In the exercise, we assume the speed to be equal to speed of light, $v=c$, we do not have to consider the dielectrica. We get

$$l<0.01\cdot\frac{c}{f}\Rightarrow\frac{3\cdot10^6}{f} \tag{48}$$

With the values inserted, we get

a) $f=20$ kHz: $L=20$ cm, $l=3\cdot10^6/20\cdot10^3=150$ m >> 20 cm. LUMPED.

a) $f=60$ Hz: $L=50$ km, $l=3\cdot10^6/60=50$ km ~ 50 km. DISTRIBUTED.

a) $f=600$ MHz: $L=20$ cm, $l=3\cdot10^6/600\cdot10^6=0.5$ cm << 20 cm. DISTRIBUTED.

a) $f=100$ GHz: $L=1$ mm, $l=3\cdot10^6/100\cdot10^9=0.03$ mm << 1 mm. DISTRIBUTED.

13.2. Reflections

✗ This exercise also exists in the andaLectureTest lab library.

$Z_0=50$ Ω and source resistance of $R_S=1$ Ω. Load resistance of $R_L=1000$ Ω.

The input voltage describes a step function from 0 to 5 Volts at $t=0$, $v=2\cdot10^8$ m/s, $L=0.2$ m.

a) What are the reflection coefficients at both ends?

The reflection coefficients are given by

$$\Gamma=\frac{Z_x-Z_0}{Z_x+Z_0} \tag{49}$$

For the source:

$$\Gamma_s=\frac{R_S-Z_0}{R_S+Z_0}=\frac{1-50}{1+50}=\frac{-49}{51}\approx-1 \tag{50}$$

and for the load

$$\Gamma_s=\frac{R_L+Z_0}{R_L+Z_0}=\frac{1000-50}{1000+50}=\frac{950}{1050}\approx1 \tag{51}$$

At the source it reflects with opposite phase (voltages subtract). At the load it reflects with same phase (voltages add)

b) Find the voltage across the load resistor as a function of time.

First, we identify that it takes $T_0=L/v=1$ ns to travel from source to load. This should be visible in the diagram.

So, first we send off 5 V. The source will "see" a voltage of $5\cdot50/(1+50)$. Notice the voltage division - independent on load.

This wave will travel to the other side, and 1 ns later it arrives at the load. Here the reflection coefficient is high, almost 1.

Almost the entire voltage is reflected back and yields 10 V (!) This wave in turn travels back to source, where the reflection coefficient is -1, such that the wave is cancelled out, etc.

[PICTURE OF THE SETTLING CAN BE OBTAINED FROM THE LAB SETUP]

c) What is the final voltage at the load resistor.

The final voltage at the resistor, after all the bounces back and forth, must be given by the voltage division over the load and source. We have

$$V_L = \frac{R_L}{R_S + R_L} \cdot V_S = \frac{5 \cdot 1000}{1001} \approx 5 \text{ V} \tag{52}$$

13.3. Matched loads

✗ This exercise also exists in the andaLectureTest lab library.

Assume a transmission line $Z_0=50$ Ω, and source resistance of $R_S=25$ Ω, load resistance is $R_L=50$ Ω and the input voltage describes a step function from 0 to 5 Volts at $t=0$.

The speed-of-propagation is $v=20$ cm/ns. The transmission line is 20 cm long.

a) What are the reflection coefficients at both ends?

$$\Gamma=\frac{Z_x-Z_0}{Z_x+Z_0} \tag{53}$$

For the source:

$$\Gamma_s=\frac{R_S-Z_0}{R_S+Z_0}=\frac{25-50}{25+50}=-0.333 \tag{54}$$

and for the load

$$\Gamma_l=\frac{R_L+Z_0}{R_L+Z_0}=\frac{50-50}{50+50}=0 \tag{55}$$

We have a perfect match on the load. The wave will be fully absored at the end.

b) Find the voltage across the load resistor as a function of time.

The outgoing wave from the source is given by

$$V_{first}=5\cdot\frac{Z_0}{R_S+Z_0}=\frac{5\cdot 50}{75}=3.333\ \text{V} \tag{56}$$

The incoming waves will be fully absored at the end and no reflection. This makes the output just accept the incoming puls and at 1 ns. Then ready. The source impedance is of less concern.

c) What is the final voltage at the load resistor.

Voltage division still holds for the end value.

$$V_L=\frac{R_L}{R_S+R_L}\cdot V_S=\frac{5\cdot 50}{75}\approx 3.333\ \text{V} \tag{57}$$

13.4. DC Termination

Transmission line with $Z_0=50$ Ω, and source resistance of $R_S=67$ Ω. Supply is 3.3 V.

a) Dimension R_1 and R_2 to provide matched load and a DC voltage of 0.75 V.

Ignore the source for time being and just set the resistors at the end accordingly:

$$V_{DC}=0.75=3.3\cdot\frac{R_2}{R_1+R_2} \tag{58}$$

And matching requires $R_L=Z_0$.

$$Z_0=\frac{R_1\cdot R_2}{R_1+R_2}=\frac{0.75\,R_1}{3.3}\Rightarrow R_1=3.3\,\frac{Z_0}{0.75}=4.4\,Z_0=220 \text{ and } R_2=\frac{200}{3.4}\approx 60 \tag{59}$$

b) Calculate the current through the driver for the high and low states.

In the settled high-state (of the driver), the path from Supply is a 67 Ohm in parallel with 220 Ohm through 60 Ohms down to ground.

In the settled low-state (of the driver), the path from Ground is a 67 Ohm in parallel with 60 Ohm through 200 Ohms up to supply.

c) With the "traditional" termination (only resistor R_2), what would be the current through the driver for high and low states?

For low states, no current at all.

For high states it would be 67 Ohms in series with 60 Ohms down to ground.

d) Which consumes most power

c)

13.5. Series termination

13.6. Splitted transmission lines

13.7. Termination

EXERCISE SECTION 14: DECOUPLING CAPACITORS AND POWER SYSTEMS

14.1. Board-level bypass capacitor

14.2. Highest effective frequency of a bypass “decap” (decoupling capacitor)

14.3. Non-ideal decaps

14.4. To be added

14.5. To be added

EXERCISE SECTION 15: TIMING AND MISCELLANEOUS

15.1. Loop filter of a PLL

15.2. Sources of jitter and skew

15.3. PLL division ratio

15.4. PLL jitter

15.5. Clock drivers

EXERCISE SECTION 16: COMPUTER-AIDED LESSONS

16.1. Amplifier stages

16.2. Opamp application 1

16.3. Opamp application 2

16.4. Compensation of opamps

16.5. Filters

16.6. Nonideal decoupling capacitors 1

16.7. Non-ideal decoupling capacitors 2

16.8. INL/DNL