ATIK and ANDA Exercises 2014

General information

Welcome to the 2013 versions of the ATIK and ANIK courses. Jointly referred to as the ANTIK courses. This is your exercise manual for this year and more information is found at:

http://www.es.isy.liu.se/courses/A*IK/lessons.html

We are currently compiling most of our material in a more handy format and you now find the new generation of our exercises manual. Unfortunately this (this year) implies that some of the solutions are found in multiple other sources. We have however indicated where to find the solutions in the exercises of this document.

K -- Kompedium

J&M - Johns & Martin

S - Schaumann

The teaching assistant can guide you through how to find the answers to the questions.

> ✗ As usual it is suggested to not print the whole document. Keep your laptop next to you... save some trees.

And as usual:

> ✗ Some of the lessons are also treated as seminars and the student should be interactive with the TA.

List of Exercises

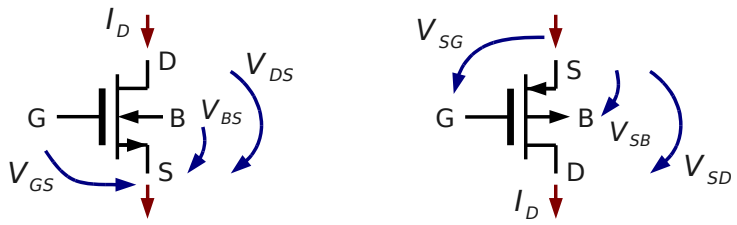
Document history

Rev	Date	Comment	Issued/Created by
0,1	the old days.	Creation.	Anton Blad, Erik Säll, Robert Hägglund, K Ola Andersson, Niklas U Andersson, J Jacob Wikner, etc., etc.
...			
P3C	2011-01-10	Changed document number.	J Jacob Wikner
P4C	2011-01-10	Added continuous-time filters exercises.	Syed Ahmed Aamir
P1D	2012-01-09	Distributed to TAs and LA for feedback. Almost all pictures in place.	J Jacob Wikner
P2D	2012-01-10	Adding the final pictures and ready for review.	J Jacob Wikner
E	2012-01-20	Released for class of 2012 after some typographical corrections.	J Jacob Wikner
E	2013-01-21	Marked filter questions (Ch.7) with 'S'	Prakash Harikumar
P1F	2013-02-21	Added transmission lines and decoupling capacitor chapters (for ANDA). Identified exercises for the computer aided lessons.	Reza Sadeghifar J Jacob Wikner
P2F	2014-01-15	Cleaned up the document for the class of 2014.	J Jacob Wikner Joakim Alvbrant
P3F	2014-01-28		

EXERCISE SECTION 1: INTRODUCTION

1.1. Definitions of voltages and currents

As a quick reference, we have pasted the directions, and indicators to ports, currents, voltages, etc., for the NMOS and PMOS transistors in Figure 1.1.1.



(a) NMOS (b) PMOS

Figure 1.1.1: Schematic symbols of (a) NMOS and (b) PMOS transistors with voltages and currents indicated.

1.2. (Approximate) Device equations

General

For convenience we use a couple of 'abbreviations' and shorter forms, as:

$v_{eff} = V_{GS} - V_T$ ($v_{eff} = V_{SG} - V_T$ for PMOS) is the effective gate voltage. (1)

$\alpha = \frac{\mu_0 C_{ox}}{2} \cdot \frac{W}{L}$, $K = \mu_0 C_{ox}$, $\beta = K \cdot \frac{W}{L}$, $S = \frac{W}{L}$ (2)

$\lambda = \frac{1}{V_\theta}$ is the channel length modulation. (3)

(Notice the deliberately "sloppy" notation with lower and upper cases.)

NMOS transistors

Cut-off region (subthreshold):

$V_{GS} < V_T$ or $v_{eff} < 0$ (4)

$I_D \approx 0$ (5)

✗ The current is considered to be more or less 0 for hand calculations. It should however be mentioned that nowadays one should not be too afraid to use the transistors in the sub-threshold region. As we get close to the threshold the gain of the transistor is comparatively

Linear region:

$V_{GS} \geq V_T$, or $v_{eff} > 0$
$V_{DS} < V_{GS} - V_T$, or $V_{DS} < v_{eff}$ (6)

$$I_D \approx \frac{\mu_0 \cdot C_{ox}}{2} \cdot \frac{W}{L} \cdot \left(2(V_{GS} - V_T) \cdot V_{DS} - V_{DS}^2\right) = \alpha \cdot \left(2 v_{eff} V_{DS} - V_{DS}^2\right) \quad (7)$$

Saturated region:

$V_{GS} \geq V_T$, or $v_{eff} > 0$
$V_{DS} \geq V_{GS} - V_T$, or $V_{DS} \geq v_{eff}$ (8)

$$I_D \approx \frac{\mu_0 \cdot C_{ox}}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_T)^2 \cdot \left(1 + \frac{V_{DS}}{V_\theta}\right) \approx \alpha \cdot v_{eff}^2 \quad (9)$$

Threshold voltage:

$$V_T \approx V_{T,0} + \gamma \cdot \left(\sqrt{2\Phi_F - V_{BS}} - \sqrt{2\Phi_F}\right) \quad (10)$$

✗ The higher source-bulk voltage the higher the threshold voltage, i.e., bad.

PMOS transistors

Cut-off region (subthreshold):

$$V_{SG} < V_T \text{ or } v_{eff} < 0 \tag{11}$$

$$I_D \approx 0 \tag{12}$$

Linear region:

$$\begin{aligned} &V_{SG} \geq V_T \text{, or } v_{eff} > 0 \\ &V_{SD} < V_{SG} - V_T \text{, or } V_{SD} < v_{eff} \end{aligned} \tag{13}$$

$$I_D \approx \frac{\mu_0 \cdot C_{ox}}{2} \cdot \frac{W}{L} \cdot \left(2(V_{SG} - V_T) \cdot V_{SD} - V_{SD}^2 \right) = \alpha \cdot \left(2 v_{eff} V_{SD} - V_{SD}^2 \right) \tag{14}$$

Saturated region:

$$\begin{aligned} &V_{SG} \geq V_T \text{, or } v_{eff} > 0 \\ &V_{SD} \geq V_{SG} - V_T \text{, or } V_{SD} \geq v_{eff} \end{aligned} \tag{15}$$

$$I_D \approx \frac{\mu_0 \cdot C_{ox}}{2} \cdot \frac{W}{L} \cdot (V_{SG} - V_T)^2 \cdot \left(1 + \frac{V_{SD}}{V_\theta} \right) \approx \alpha \cdot v_{eff}^2 \tag{16}$$

Threshold voltage:

$$V_T \approx V_{T,0} + \gamma \cdot \left(\sqrt{2\Phi_F - V_{SB}} - \sqrt{2\Phi_F} \right) \tag{17}$$

1.3. Circuit noise

Noise comes in many flavours and we limit ourselves to two of them.

Thermal noise

The thermal noise spectral density at the gate of a CMOS transistor is

$$v_t^2(f)=\frac{4kT\cdot\gamma}{g_m} \tag{18}$$

where γ traditionally was 2/3, but nowadays it can be higher than 1.

Flicker noise

The flicker noise spectral density at the gate of a CMOS transistor is

$$v_f^2(f)=\frac{K}{WL\cdot C_{ox}f} \tag{19}$$

where K is a constant.

✗ Integrating the noise spectral density over a certain frequency band gives you the noise power. Notice that, in both cases, an infinite noise power is obtained if integrating over all frequencies.

1.4. Approximate parameters for a 0.35-micron process

In Table 1.1 we have compiled some "older" process parameters for hand calculations that are also used throughout the exercises.

✗ Notice that more modern processes will have quite different values, but it is also more difficult to perform the hand calculations in the same way.

Param.	Unit	NMOS	PMOS	Comment
μ_0	$cm^2/V\,s$	400	130	Charge mobility, "holes are slower than electrons".
C_{ox}	nF/cm^2	450	450	
V_θ	V	33	20	$L=1\,\mu m$
V_θ	V	100	50	$L=5\,\mu m$
$V_{T,0}$	V	0.47	0.62	The PMOS typically has higher threshold voltage ...
γ	$\sqrt{V}$	0.62	0.41	... but is less sensitive to bulk variations.
$2\Phi_F$	V	0.86	0.82	

Table 1.1: Some typical values for hand-calculations.

EXERCISE SECTION 2: DC ANALYSIS

- If not stated otherwise, we use the process parameters given in Sec. 1 (Introduction), the power supply voltage is $V_{DD}=3.3$ V, the transistor lengths are $L=1$ um.

- If not stated otherwise, the bulks of the NMOS and PMOS transistors are connected to ground and positive supply, respectively.

2.1. DC analysis on a common-source gain stage with cascodes

Consider the common-source stage of cascode type in Figure 2.1.1.

a) Determine $V_{b,4}$ and the DC level of V_{in}. Also determine suitable values for the bias voltages $V_{b,2}$ and $V_{b,3}$.

b) For these values calculate the output range $[V_{out,min}, V_{out,max}]$.

The widths of all transistors are $W=50\,\mu$m and the current is $I=50\,\mu$A.

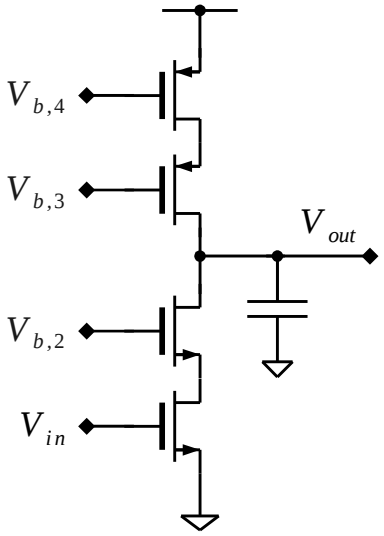


Figure 2.1.1: Common-source amplifier of cascoded type.

2.2. DC analysis of a bias circuit

The circuit in Figure 2.2.1 is used to establish an appropriate bias voltage to an operational amplifier.

Design the circuit such that the output bias voltage is $V_{bias}=0.6$ V and the power dissipation $P_d<16.5\,\mu$W.

Motivate all your assumptions of the circuit and approximations.

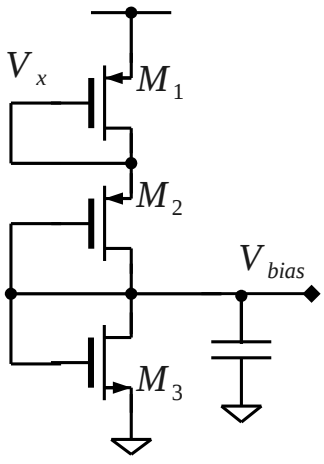


Figure 2.2.1: A bias circuit.

2.3. DC analysis of a common-gate amplifier

An ideal voltage source is connected to the input node, V_{in}, in the common-gate amplifier in Figure 2.3.1.

a) Determine the operation regions of the transistor M_1 when node V_{in} ramps from supply to ground.

b) Explain how to find the input voltage where transistor M_1 starts to operate in its linear operation region.

Assume that transistor M_2 operates as a near-ideal current source delivering an almost ideal current I_b.

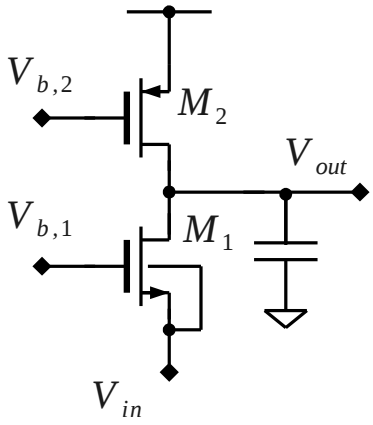


Figure 2.3.1: A common-gate gain stage.

2.4. Simple gain stages with passive load

Consider the three gain stages in Figure 2.4.1.

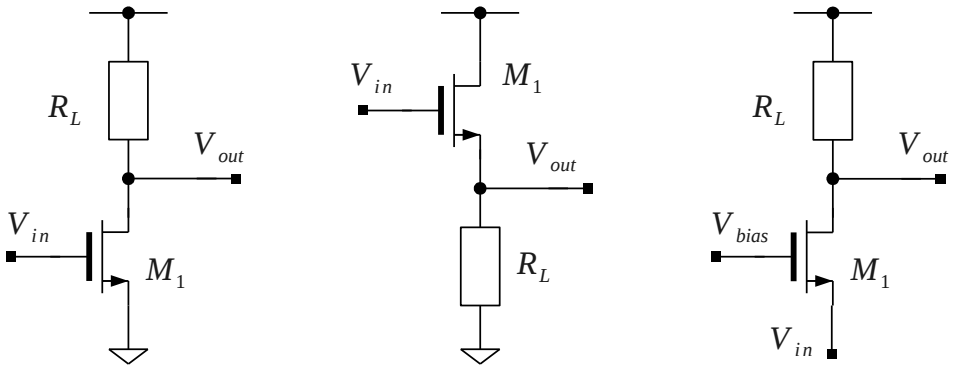
a) Derive the equivalent small-signal models for each of the amplifier stages. Ignore the influence of capacitances and bulk effects.

b) Derive the DC gain and the output resistance of the common-source amplifier.

c) Sketch the output signal as function of the input signal. Assume that the input signal is a ramp from 0 to V_{DD} volts.

d) Derive the same answers in (a) and (b) but for the common-drain and common-gate amplifier when also considering the bulk effects.

e) Derive the highest and lowest output/input voltages that still guarantee that the transistors operate in the saturation regions?



(a) NMOS CS (b) NMOS CD (c) NMOS CG

Figure 2.4.1: Transistor views of single-stage amplifier stages; common-source (a), -drain (b), and -gate (c).

EXERCISE SECTION 3: AC ANALYSIS

- If not stated otherwise, we use the process parameters given in Sec. 1 (Introduction), the power supply voltage is $V_{DD}=3.3$ V, the transistor lengths are $L=1$ um.

- If not stated otherwise, the bulks of the NMOS and PMOS transistors are connected to ground and positive supply, respectively.

3.1. Derivation of small-signal parameters 1

Derive expressions for the small-signal parameters g_m, g_{mbs}, and g_{ds} of an NMOS transistor in

a) the linear region

b) the saturated region

Derive approximate expressions for the small-signal parameters in terms of the **drain current and the effective gate voltage**. Then also elaborate on if

c) a high g_{mbs} is good or bad for your design?

3.2. Derivation of small-signal parameters 2 (K7)

Consider the MOS transistor as a two-port device (gate-source on one side and drain-source on the other).

a) Derive the two-port parameters and choose the most suitable ones (z, y, or h). Choose proper parameters.

b) How do these correspond to the equivalent small signal schematics from exercise 3.1?

3.3. Small-signal parameters (K8)

Using the transistor as something else than a gain circuit.

a) Show how (mathematically and with a sketch) a transistor can be used as a resistor. In what region should the transistor operate?

b) Explain how this resistance depends on the drain, gate, source and bulk voltages.

3.4. Common-gate amplifier with non ideal input source

Assume that a voltage source with an input resistance R_{in} is connected to the node V_1 of a common-gate stage as shown in Figure 3.4.1. Derive the transfer function from V_{in} to V_{out}. Assume that all transistors are operating in the saturation region.

a) First, ignore all parasitic capacitances.

b) Then, consider the influence of the gate-source capacitance of M_1, i.e., C_{gs1}. What happens if C_{gs1} is very large?

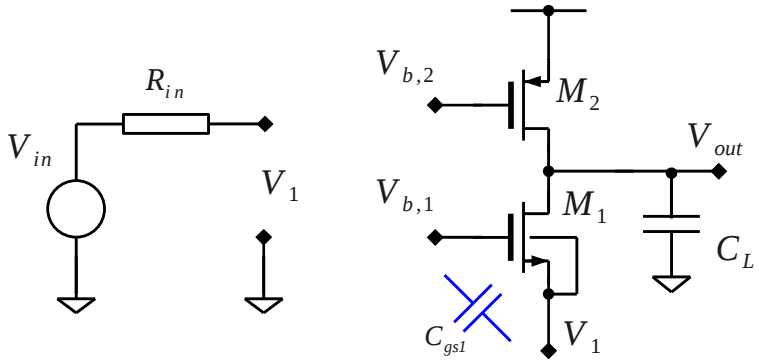


Figure 3.4.1: A non-ideal voltage source with a common-gate gain stage.

3.5. Common-gate amplifier input impedance (K3)

Consider the common-gate amplifier in exercise 2.3. However, now assume that the load impedance is resistive, R_{load}. Also assume that $R_{in}=0$ and that the bulk terminal of M_1 is grounded.

Determine an expression for the low frequency input impedance of the common-gate amplifier.

3.6. Amplifier stages with active load

✗ Computer aided lessons!

Consider the four amplifier stages in Figure 3.6.1.

a) Derive the small-signal models for each one of the four amplifier stages.

b) Derive the DC gain and the output impedance.

c) Derive expressions for the dominant poles, i.e., the bandwidth, of the stages.

d) Assume that all transistors are approximately equally large, which stage has the highest gain?

e) Assume that all transistors are approximately equally large, which stage has the highest bandwidth?

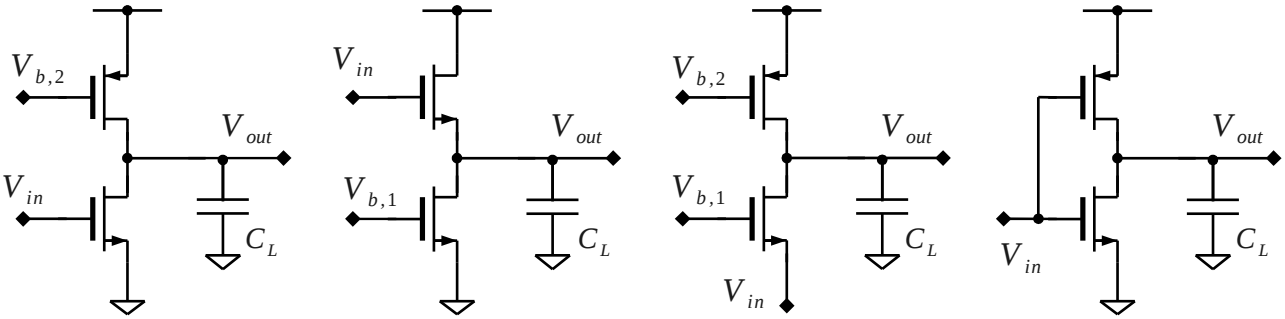


Figure 3.6.1: Transistor views of single-stage amplifier stages. From left: common-source, common-drain, common-gate, and CMOS inverter, respectively.

3.7. Current mirrors

Consider the three current mirrors shown in Figure 3.7.1.

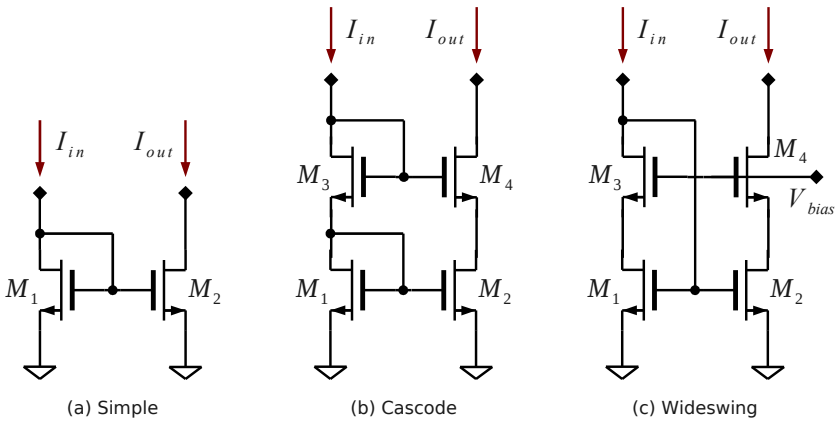


Figure 3.7.1: Simple (a), cascode (b), and wide-swing (c) current mirrors.

a) Derive the input and output impedances for all three.

b) What are the lowest possible input/output/bias voltages required to ensure that all transistors are operating in their saturation regions?

c) Which current mirror is the "best"? Why?

3.8. Gain stages with cascodes

Consider the two amplifier stages shown in Figure 3.8.1.

a) What is the circuit structure to the right called?

b) Derive the output impedance and DC gain for both stages. Also compare the gains with the ones found for the common-source amplifier in Excercise 3.6

c) Consider the amount of parasitic capacitance in the signal path. Which circuit has the lowest bandwidth?

d) Which one of the two approaches is the ”best”? Why?

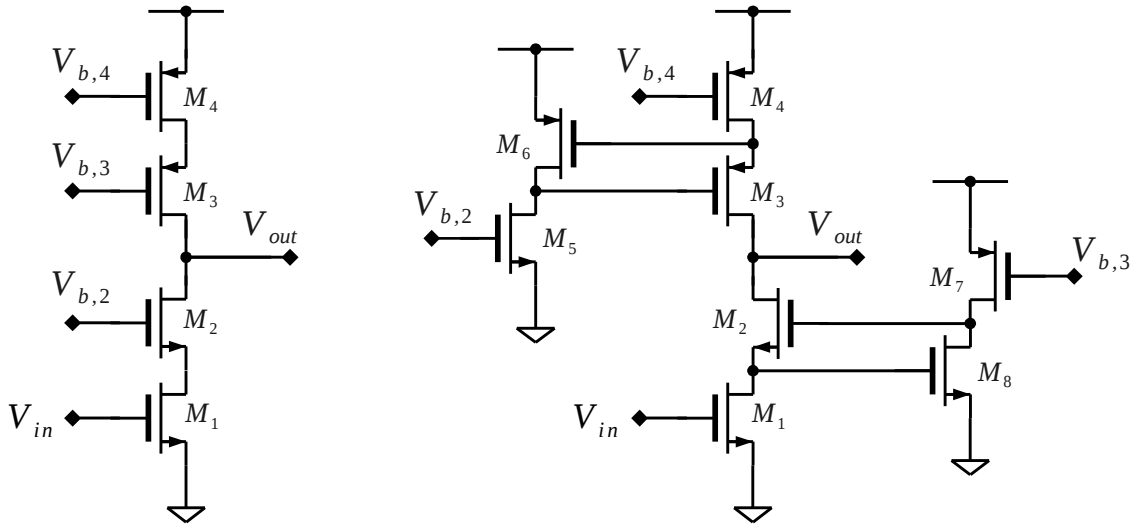


Figure 3.8.1: Amplifiers with higher DC gain than simple amplifiers.

EXERCISE SECTION 4: DIFFERENTIAL GAIN STAGES

- If not stated otherwise, we use the process parameters given in Sec. 1 (Introduction), the power supply voltage is $V_{DD}=3.3$ V, the transistor lengths are $L=1$ um.

- If not stated otherwise, the bulks of the NMOS and PMOS transistors are connected to ground and positive supply, respectively.

4.1. A single-ended differential gain stage

Consider the differential stage in Figure 4.1.1. Assume that the bias transistor has an infinite output impedance (i.e., is an ideal current source giving I_{bias}) when calculating the small-signal characteristics. Further, the size of transistor M_5 is equal to that of M_6.

a) Calculate the output range (OR), the common-mode range (CMR), the output impedance, and the small-signal transfer function.

b) Derive the slew rate (SR) of the differential gain stage.

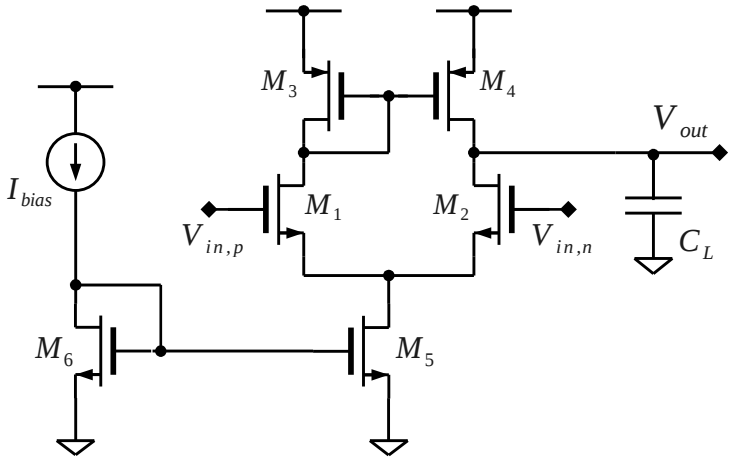


Figure 4.1.1: A differential gain stage.

4.2. Differential stage with passive load

Consider the differential gain stage in Figure 4.2.1.

a) Derive the differential gain and the output impedance.

b) Derive the gain from the common-mode input voltage to the common-mode output voltage, i.e., $A_{cm,cm}=V_{out,cm}/V_{in,cm}$.

c) Derive the power-supply rejection ratio with respect to the ground node.

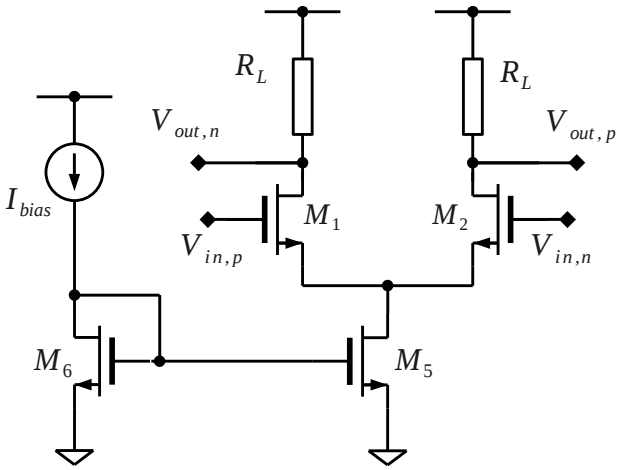


Figure 4.2.1: An NMOS differential stage.

4.3. Differential signals

Assume you have two parallel branches with a input-output transfer characteristic as

$$V_{out}=A_0+A_1\cdot V_{in}+A_2\cdot V_{in}^2+A_3\cdot V_{in}^3. \quad (20)$$

You can assume the same noise power in both branches and you can assume that the noise is uncorrelated.

a) Show that the signal-to-noise ratio improves in a differential circuit.

b) Show that the linearity improves in a differential circuit.

EXERCISE SECTION 5: OTAS AND OPS

- If not stated otherwise, we use the process parameters given in Sec. 1 (Introduction), the power supply voltage is $V_{DD}=3.3$ V, the transistor lengths are $L=1$ um.

- If not stated otherwise, the bulks of the NMOS and PMOS transistors are connected to ground and positive supply, respectively.

5.1. OP and OTA

What are the main differences between an OP and an OTA?

Discuss both the circuits themselves and the applications in which they are used.

5.2. Current mirror OTA

Consider the current mirror OTA in Figure 5.2.1. The following device sizes hold for the different transistors.

$S_1=S_2$, $S_{4,5,6,8,10}=S_3$, $S_{7,9}=K\cdot S_3$, $S_{11}=S_{13}=K\cdot S_{14}$, $S_{12}=S_{14}$

Choose proper transistor sizes and bias current to meet the following specification:

$A_0=80$ dB, $SR=40$ V/us, $\omega_u=2\pi\cdot 50$ Mrad/s, $C_L=10$ pF, and $P_d=1.5$ mW.

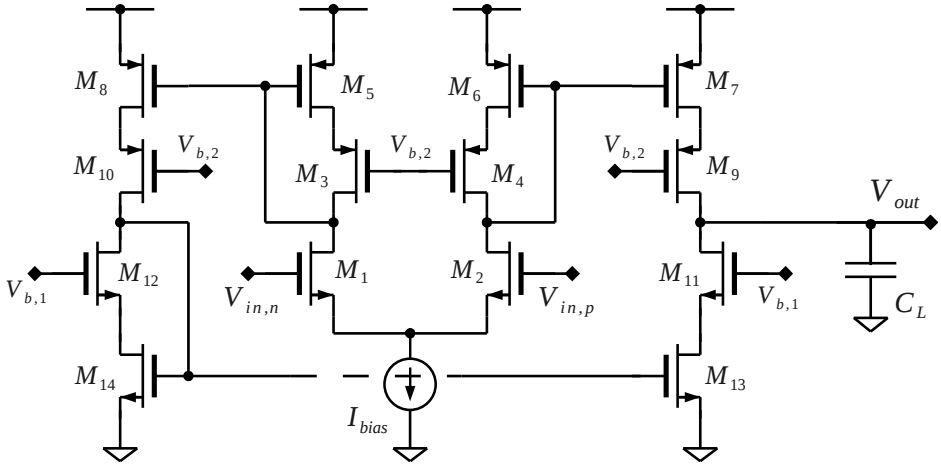


Figure 5.2.1: A current-mirror OTA.

5.3. A simplified model of a two-stage operational transconductance amplifier

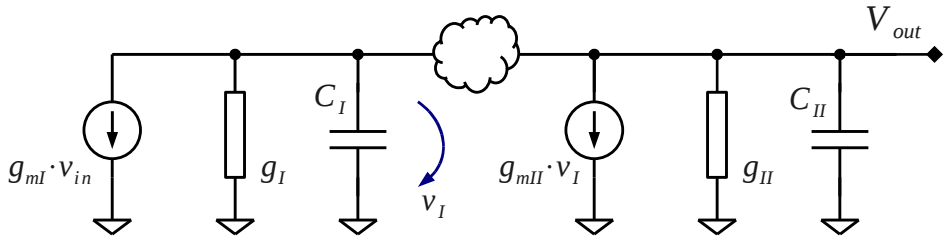


Figure 5.3.1: The small-signal model of a two-stage operational transconductance amplifier.

An equivalent small-signal model of the OP in Figure 5.3.2 is shown in Figure 5.3.1.

a) Which component/components can be used in the compensation circuit? Derive expressions for the parameters g_I, g_{II}, g_{mI}, g_{mII}, C_I, and C_{II}.

b) Assume that the compensation network consists of a single compensation capacitor. Compute the small-signal DC gain. Show that the unity-gain frequency is approximately equal to g_{mI}/C_c.

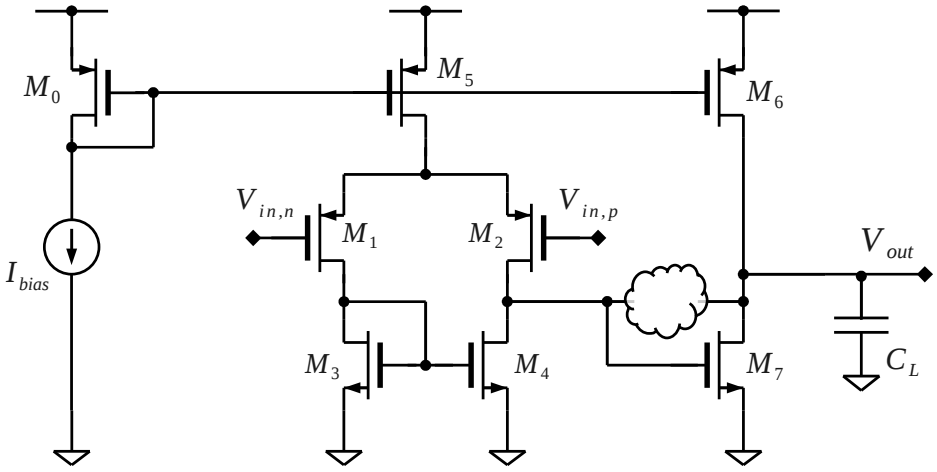


Figure 5.3.2: A two-stage OP/OTA with compensation circuit (the cloud).

What will happen to the gain (A_0), unity-gain frequency (ω_u), and the first pole, p_1, if

c) the widths of the transistors M_1 and M_2 are increased?

d) the bias current is increased?

e) the widths of the transistors M_3 and M_4 are increased?

5.4. A two-stage OTA without compensation circuit

Consider the two-stage OTA in Figure 5.3.2 with the compensation circuit removed.

a) Derive the DC gain. How is the gain related to the branch currents?

b) Find expressions for the dominant and non dominant poles.

c) Derive expressions for the phase margin and unity-gain frequency.

d) What could you do to make the circuit in Figure 5.3.2 become more like an ideal OP in terms of output resistance?

5.5. Feedback modes (K2)

Consider the two OP-amp configurations in Figure 5.5.1.

a) Which type of feedback is used for the circuits below?

b) Calculate the loop gain, input/output impedance and the transfer function for the circuits. The voltage gain of the op-amp is A and the output impedance is Z_{out} .

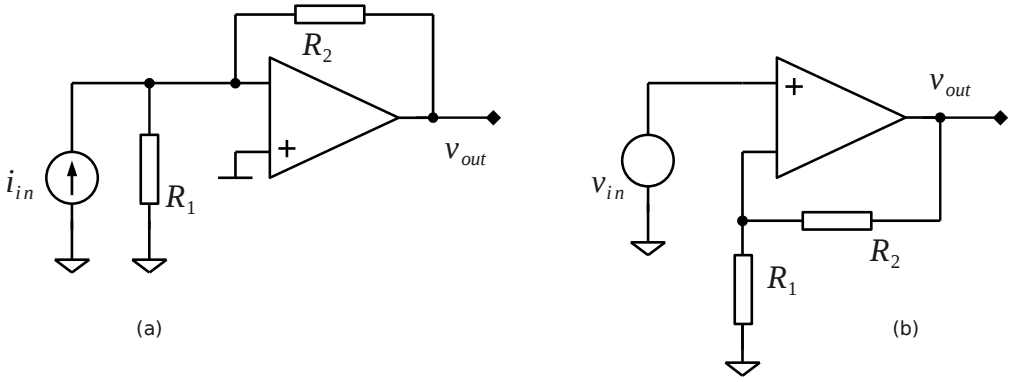


Figure 5.5.1: OP amp feedback configurations.

5.6. Feedback factor (K4)

Determine the loop-gain, feedback factor β and total transfer function for the circuit in Figure 5.6.1.

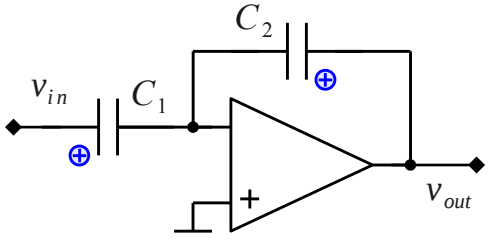


Figure 5.6.1: Amplifier in feedback configuration.

5.7. Compensation of a two-stage OTA

✗ Computer aided lessons!

Consider the two-stage amplifier shown in Figure 5.3.2 and use the results from Excercise 5.4 as well.

a) Consider the two compensation methods: plain Miller capacitance and capacitance with resistance. The latter approach can be used in two different ways in order to cancel zeros. Which are these two methods?

b) Derive expressions that describe the transfer function from differential input to output and also includes the two different compensation circuits.

c) How is the unity-gain frequency affected when you add the compensation circuit? The DC gain? The bandwidth?

d) Explain how to choose the values on R and C (in the compensation network) circuit in order to increase the phase margin.

5.8. A folded-cascode OTA

Consider the folded-cascode OTA in Figure 5.8.1.

✗ Notice that all bulks of the transistors are connected to their sources, i.e., $V_{BS}=V_{SB}=0$.

a) Derive the differential voltage DC gain and the first pole of the circuit. No parasitic capacitances need to be considered.

b) The second pole arises from the parasitic capacitances on the drain of M_1/M_2. The expression for this pole is $p_2 \approx g_{m7}/C_x$ where C_x is the parasitic capacitance

How do you increase the phase margin ...

c) ... if the area is limited?

d) ... if the power is critical?

e) ... if the unity-gain and power are critical?

In each case above,

f) what are the drawbacks of the circuit performance?

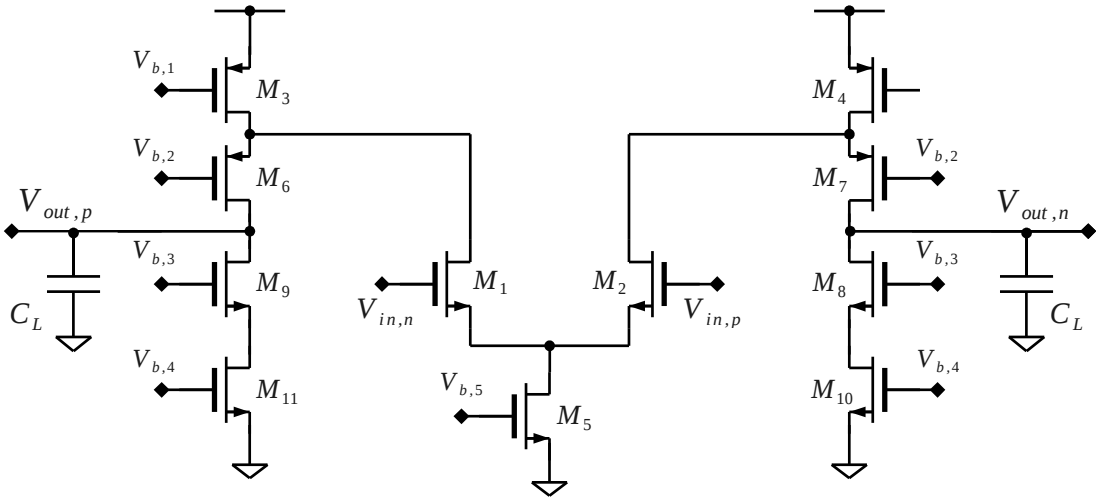


Figure 5.8.1: A folded-cascode differential amplifier.

5.9. OP application (K9)

✗ Computer aided lessons!

Suppose the circuit in Figure 5.9.1 has ideal operational amplifiers.

a) Derive the input impedance and the K-matrix for the circuit.

b) What is the advantage with a circuit like this? How should the components (impedances) be chosen to let the circuit simulate an inductance?

c) Discuss what will happen if the operational amplifiers are non-ideal. How will the input impedance change, etc.?

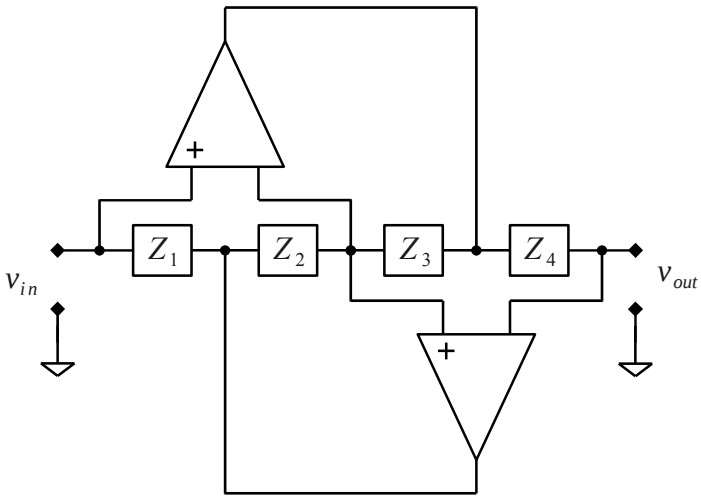


Figure 5.9.1: OP amp circuit.

5.10. Gm-C application (K10)

Consider the Gm-C circuit in Figure 5.10.1.

a) Derive the transfer function.

b) Also derive the transfer function when assuming that the transconductor has a finite output resistance, R_{out}.

c) What is the disadvantage with this circuit?

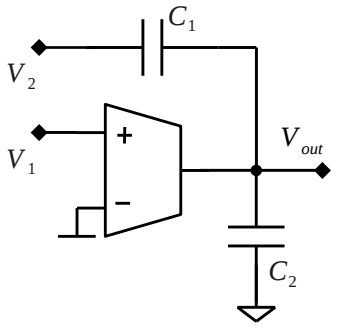


Figure 5.10.1: GmC circuit

5.11. OP/OTA stability

Consider the configuration in Figure 5.11.1. There are two amplifiers in series, the output conductance of the first stage is G_I, and for the second it is G_{II}. The transconductances of the respective cases are indicated in the figure.

The total DC voltage gain is 7200 and the DC gain of the second stage is eight times the gain of the first stage.

a) What is the total transfer function of the system?

b) Assume well-separated poles: As a function of C_I, what values can the load capacitance C_{II} take to guarantee a 45-degree phase margin?

Your answers should of course be supported by diagrams as well as formulas.

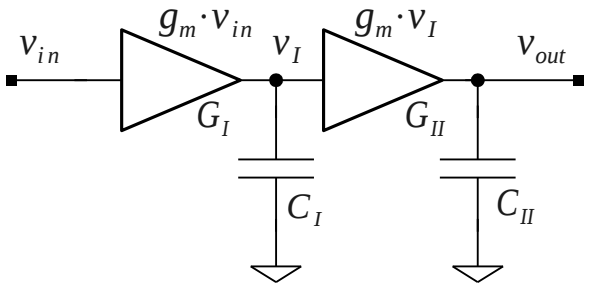


Figure 5.11.1: A two-stage amplifier.

EXERCISE SECTION 6: NOISE IN CMOS CIRCUITS

- If not stated otherwise, we use the process parameters given in Sec. 1 (Introduction), the power supply voltage is $V_{DD}=3.3$ V, the transistor lengths are $L=1$ um.

- If not stated otherwise, the bulks of the NMOS and PMOS transistors are connected to ground and positive supply, respectively.

6.1. Noise in a multi-stage amplifier

Consider the three cascoded common-source stages in Figure 6.1.1 where only the thermal noise generated in the transistor is of interest. The current sources are ideal and hence noiseless.

Let the output load capacitance be given by C_L and parasitic capacitances are only given by gate-source capacitances, C_{gs}. Further, $C_L \gg C_{gs}$ and $I_{b,1}=I_{b,2}=I_{b,3}$. All transistors are equally large and operate in the saturation region.

a) Derive the total output noise power.

b) Discuss what you should do to lower the total noise power and how it affects the DC gain and bandwidth of the circuit.

c) Assume that the widths of the transistors can be changed. Which stage should have the largest gain for a low output noise power given that the DC gain of the circuit should be maintained? Why?

d) What is the trade-off between speed (unity-gain) and noise of this type of circuit?

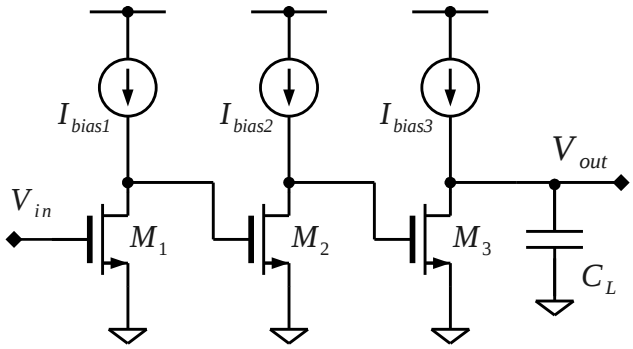


Figure 6.1.1: A noisy, multi-stage amplifier.

6.2. Noise in CMOS circuits

Consider the somewhat odd circuit in Figure 6.2.1.

a) Derive the equivalent output noise power due to the thermal noise generated by the transistors M_1 and M_2.

b) Describe two ways to decrease the equivalent output noise by changing relevant design parameters. What will happen to the DC gain, the unity-gain frequency and the slew rate of the circuit?

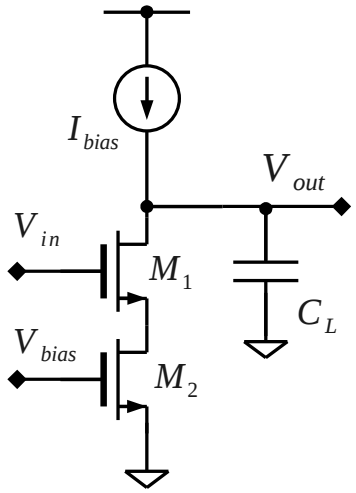


Figure 6.2.1: A noisy CMOS circuit.

6.3. Noise in an amplifier

Consider Figure 6.3.1 in which we assume that transistors M_1 and M_2 generate thermal noise only. Furthermore, I_{bias1} and I_{bias2} can be seen as DC current sources. Assume that $C_L \gg C_{gs}$.

a) Derive the total output noise power.

b) Derive the input-referred noise voltage.

c) Propose one way to increase the maximum signal-to-noise ratio, SNR. What will happen to the DC gain, unity-gain frequency, bandwidth, and the phase margin of the circuit?

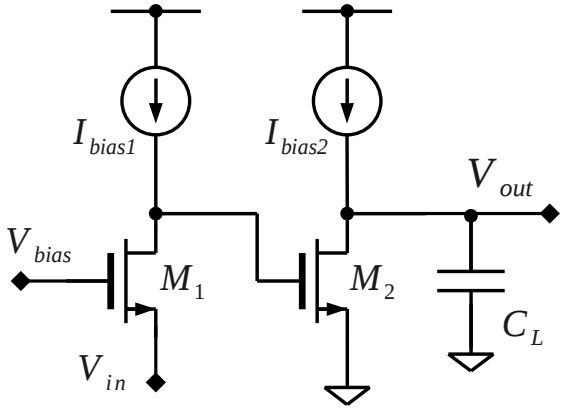


Figure 6.3.1: A noisy dual stage CMOS amplifier.

6.4. Noise in a common-source amplifier biased by a current mirror

A good model for the thermal noise in a transistor is to add a noise source in parallel with the transistor as shown in Figure 6.4.1. The noise current through the drain and source is given by

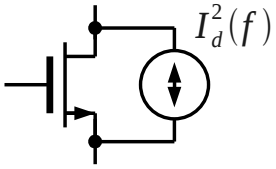


Figure 6.4.1: Noise model for a MOS transistor.

$$I_d^2(f)=4kT\gamma g_m \tag{21}$$

✗ Use this model in the exercise!

a) Derive the total thermal output noise power of the circuit shown in Figure . All capacitive parasitics are much smaller than C_L. The spectral density function for a parallel current source for the resistor is given by

$$I_r^2(f)=4kT/R \tag{22}$$

b) Describe two ways to decrease the thermal output noise power of the circuit shown in Figure by changing relevant design parameters. What will happen to the DC gain and the unity-gain frequency?

c) Add a large capacitor $C \gg C_L$ in parallel with the resistor. Furthermore assume that $1/R \ll g_{out}$. What will happen to the output noise power? What do you conclude of this?

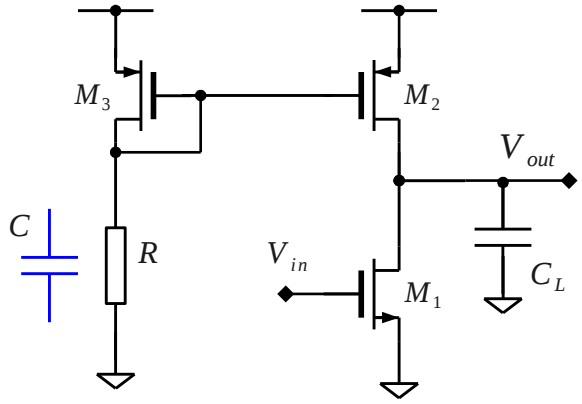


Figure 6.4.2: A noisy common-source gain stage.

6.5. Opamp noise (K6)

Calculate the equivalent input noise of the two-stage opamp as shown in Figure 5.3.2.

6.6. Opamp noise 1

Consider the operational amplifier in Figure 6.6.1. The top picture indicates noise from the opamp, which input-referred noise can be expressed by a constant noise PSD as $v_n^2(f)=v_{n0}^2$. The lower picture shows the noise from the resistors too.

Assume only thermal noise in the circuit and that the operational amplifier has a unity-gain bandwidth which is 20 times higher than the closed-loop bandwidth.

a) Derive the transfer function from v_1 to v_2.

b) What are the expressions on the noise from the resistors?

c) Calculate the equivalent opamp-input-referred noise.

d) Calculate the equivalent input-referred noise (to v_1).

e) Calculate the output-referred noise (to v_2).

f) Calculate the total output noise power.

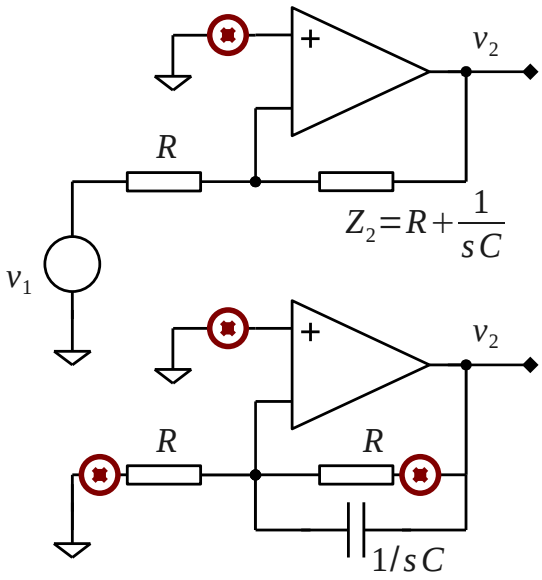


Figure 6.6.1: Example operational amplifier with noise sources indicated.

6.7. Opamp noise 2

Go back to Figure 6.6.1. Assume that the operational amplifier does not add any noise, but resistors still do. Assume that you apply an input sinusoidal signal with an amplitude of $A=1$ V.

a) What is the input signal power?

b) What is the closed-loop output signal power as function of signal frequency?

c) What is the total signal-to-noise ratio (SNR) at the output of the closed-loop system?

6.8. Opamp noise 3

Consider the two circuits in Figure 6.8.1. All components that can be noisy are noisy. The noise of the operational amplifier(s) has been indicated in the figure - assume it is a constant, $v_n^2(f)=v_{n0}^2$.

a) Derive compact expressions of the **total output noise power** for both circuits.

b) Which one of the two circuits is the **more noisy one**? What assumptions have you made in order to make the conclusion?

Make valid assumptions and motivate them well! Illustrate your results by sketching the corresponding PSD in different steps of your solutions.

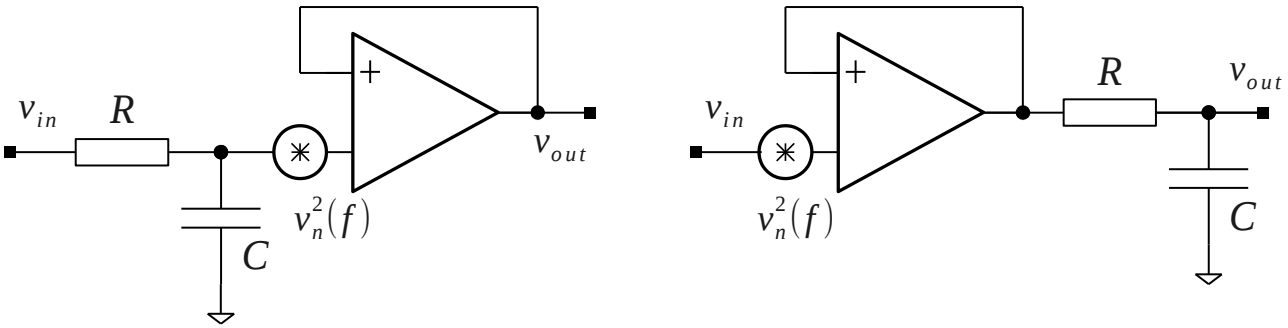


Figure 6.8.1: A buffer and some passive circuit.

EXERCISE SECTION 7: CONTINUOUS-TIME FILTERS

7.1. First-order filter (S)

Figure 7.1.1 shows a first-order passive RC filter circuit as well as an active realization. State at least four reasons why would you want to migrate towards an active filter implementation rather than a passive counterpart.

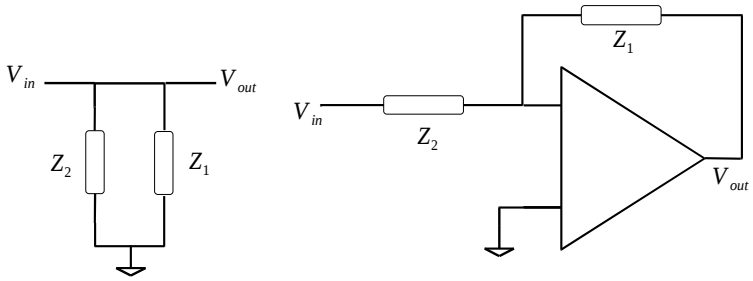


Figure 7.1.1: A passive and active circuit implementations of a first order filter.

7.2. Bilinear transfer functions (S)

The four op-amp circuits of Figure 7.2.1 show different alternatives to realize the bilinear transfer function.

a) Suppose you are asked to design a circuit with a zero at 1 kHz, and a pole at 10 kHz, and high frequency gain of 20 dB, which of these could you use and why?

b) Also suggest cases when the others might be of use!

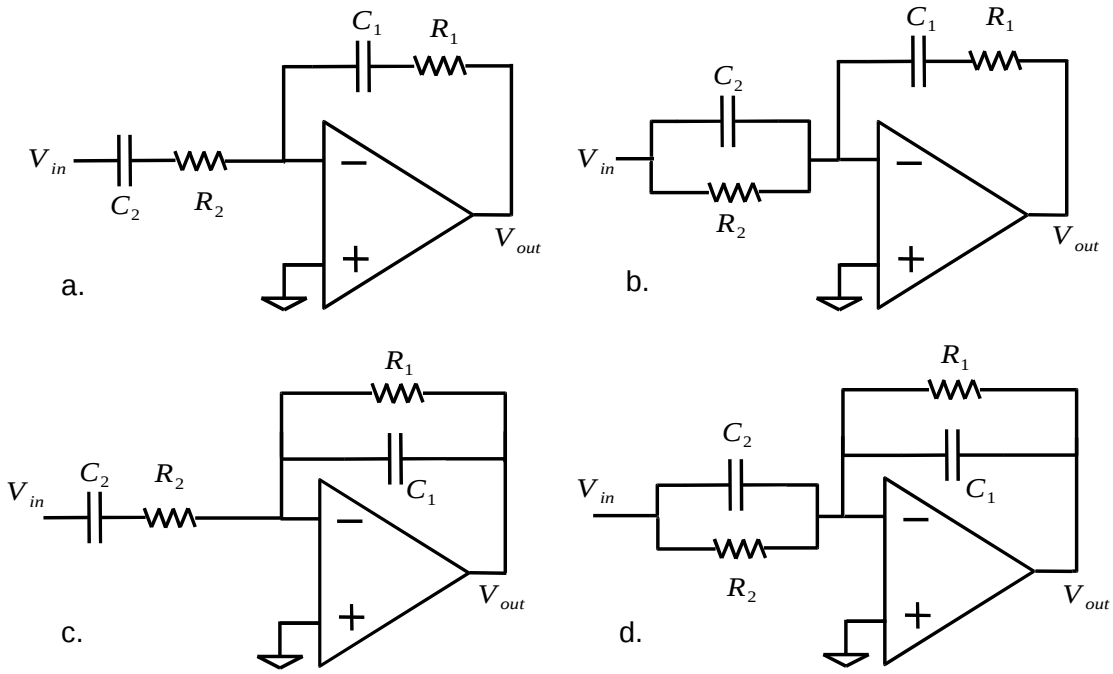


Figure 7.2.1: Four different options for realization the bilinear transfer function.

7.3. Higher-order filters starting point (S 5.3)

To realize higher order filters, one cascades two or more first order sections. However, an essential condition to realize cascaded filters is, that the following stage must not load its preceding stage.

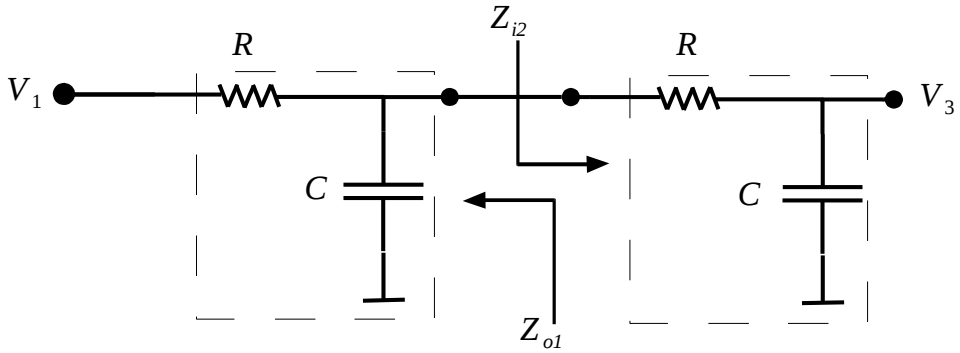


Figure 7.3.1: Cascaded passive RC filters

For example, consider a case with two single-pole low pass filters cascaded. Each one of them have a pole at $1/RC$. Multiplying the two transfer functions yields:

$$H(s)=\frac{1}{(sCR)^2+2sCR+1} \tag{23}$$

Now, consider the cascaded two RC links as in Figure 7.3.1.

a) Find the transfer function, V_3/V_1, to see how the desired transfer function changes compared to 23). Conclusions?

b) Assume you have two poles, R_1C_1 and R_2C_2 in these two cases. How should you choose the values for highest correspondence between 23) and Figure 7.3.1?

7.4. Biquads (S 5.4)

Second order filters, also referred to as Biquads, are very useful in any analog signal processing system. Their poles are complex conjugates in the left half of s-plane, whereas the zero complex conjugate pair may lie anywhere in the s-plane.

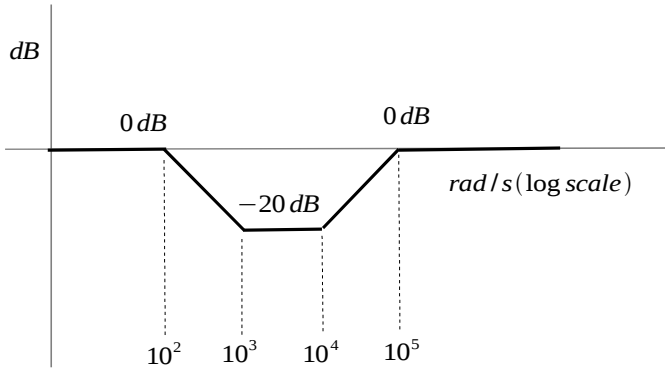


Figure 7.4.1: Asymptotic Bode plot for a bandstop filter.

A standard form of the second order transfer function may be written in terms of ω_0^2 and Q as:

$$T(s)=\frac{H\cdot\omega_0^2}{s^2+(\omega_0/Q)s+\omega_0^2} \quad (24)$$

where Q is the quality factor defined as

$$Q=\frac{\omega_0\cdot L}{R} \quad (25)$$

at the frequency $\omega=\omega_0$ and H is the DC gain. We can further normalize to obtain a standard form:

$$H(s)=\frac{V_L}{V_1}=\frac{-H}{s^2+(1/Q)s+1} \quad (26)$$

where we have stressed on the inverting properties of the realization.

Suppose you want to design a bandstop filter that satisfies the Bode-plot shown in Figure 7.4.1. The filter suppresses a band in the range $500\leq\omega\leq2500$ rad/s.

Derive your final transfer function and show your cascaded active filter implementation.

7.5. Tow-Thomas (S 5.6)

A double-integrator loop, utilized to realize second-order transfer functions, is shown in Figure 7.5.1.

The block diagram not only realizes the low-pass function T_L, but also the bandpass and highpass functions T_B and T_H. Their individual transfer function are thus:

$$V_L = \frac{-H}{s^2+(1/Q)s+1} V_1 = T_L \cdot V_1 \tag{27}$$

$$V_B = \frac{-H \cdot s}{s^2+(1/Q)s+1} V_1 = T_B \cdot V_1 \tag{28}$$

$$V_H = \frac{H \cdot s^2}{s^2+(1/Q)s+1} V_1 = T_H \cdot V_1 \tag{29}$$

The two integrator loop is realized as a Tow Thomas filter circuit, which can realize bandpass and lowpass functions.

a) Use inverting integrator, summer and normalized elements to implement the Tow-Thomas filter circuit.

b) Derive transfer function for bandpass and low pass functions.

c) Derive ω_o^2, Q, and H for the low-pass case.

d) Can you tune this circuit, if yes, how?

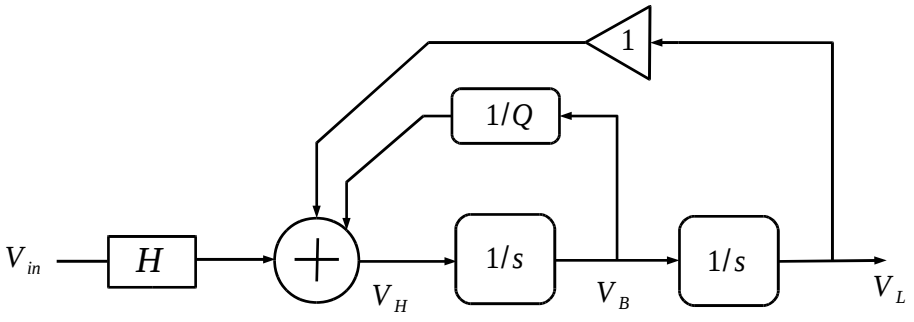


Figure 7.5.1: The block diagram of a two-integrator loop for a Tow-Thomas biquad circuit.

7.6. Sensitivity analysis (S 5.7)

The precise transfer functions of our filter implementations are mostly dependent upon the exact availability of component values, which – in the real world, can drift away from the desired numbers. This may be simple due to the unavailability of the desired component value, or otherwise, in case of integrated filters in the form of process variations.

An engineer would need a measure to predict the expected deviations in different circuits – as well as answering performance questions such as:

the circuit response to component tolerances

changes in filter specifications such as $\omega_0, Q,$ and H ?

which architectures suit most to the expected deviations ?

Notice also, that it is not sufficient as a rule to compute sensitivity to a single parameter since variations in all circuits cause the actual deviation. Hence one, eventually needs to check on the ”multiparameter sensitivity”, to get a more comprehensive estimate.

A Monte Carlo analysis is usually done to randomly specify the tolerances within an acceptance tolerance range of on all parameter set.

Apply sensitivity analysis to the filter building blocks illustrated in Figure 7.6.1

a) Passive low pass RLC
b) An inverting amplifier.
c) What are your conclusions when you compare these two cases?

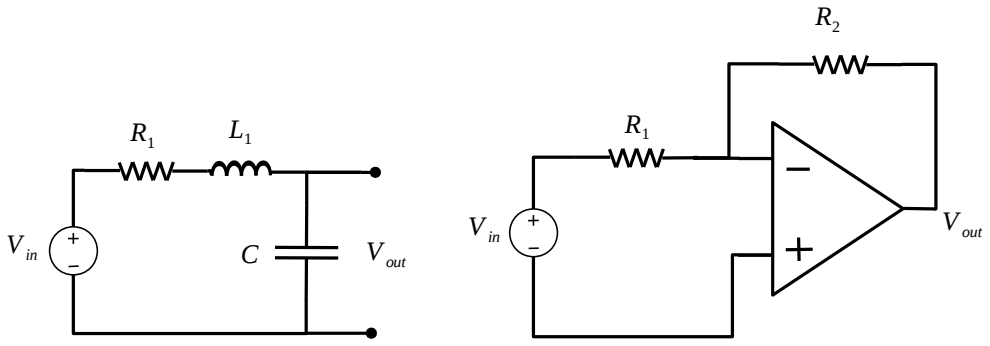


Figure 7.6.1: An RLC lowpass filter and an inverting amplifier.

7.7. Sallen-Key (S 4.11)

✗ Computer aided lessons!

Consider the circuit in Figure 7.7.1 showing a biquad implementation (Sallen Key) of an analog filter.

a) Derive the transfer function V_o/V_i

b) Derive the quality factor Q, ω_o and DC gain H

c) With your Q expression, comment on the sensitivity of the filter.

d) Why are Sallen-Keys suitable for low-Q implementations only?

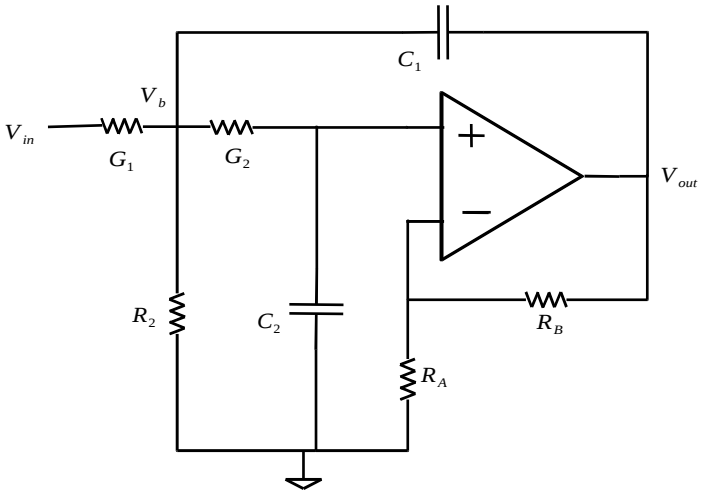


Figure 7.7.1: A Sallen and key biquad filter implementation.

7.8. Butterworth lowpass filter

Compute the component values L_1, L_3, and C_2 of the Butterworth LP filter in Figure 7.1.1 to have a cut-off frequency (when the signal is attenuated 3 dB) at $\omega_c=3.5$ kHz and an attenuation of at least 25 dB at 10 kHz.

The filter is terminated by input $R_i=1.2$ kOhm and load resistance, $R_L=0.6$ kOhm.

✗ Remember that this will give a DC gain of 1/3.

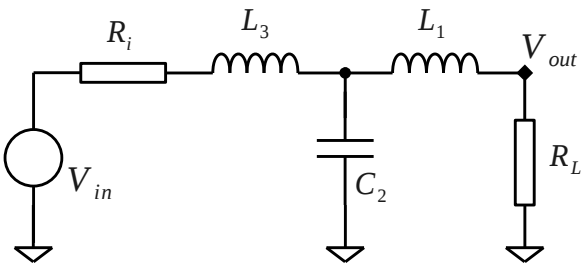


Figure 7.8.1: A doubly terminated reference ladder network.

7.9. Chebychev LP filter

Design a lowpass filter of Chebyshev I type using the following specifications:

Cut-off frequency of 1000 rad/s.

The ratio between the largest and the smallest value of the amplitude in the pass band shall be less than or equal to 1.2.

The ratio between the amplitude at 2000 rad/s and the maximum amplitude shall be at the most 0.1.

The load impedance is equal to 1 kOhm, and the generator impedance equal to 125 Ohm.

The filter shall be a current-mode filter and use RLC components.

7.10. Butterworth bandstop filter

Design a bandstop filter of Butterworth type meeting the following specification:

Pass band for $\omega<800$ rad/s and $\omega>4000$ rad/s.

In the stop band ($1600<\omega<2000$ rad/s) the attenuation should be at least 50 dB.

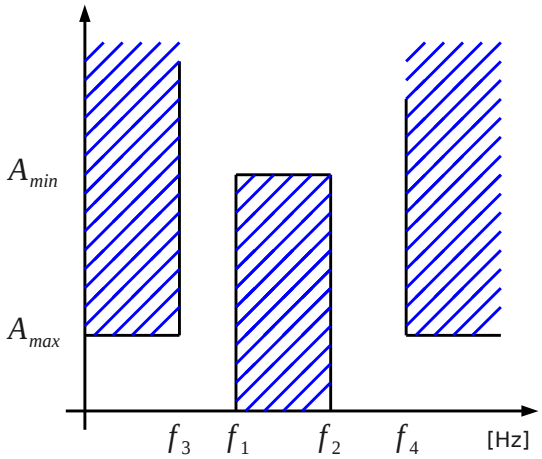
The filter shall be a voltage-mode filter having 100-Ohm loads on input and output.

Use RLC components only.

7.11. A doubly resistive terminated ladder network

Design a passive filter fulfilling the specification shown in Figure 7.11.1.

The filter shall be a voltage-mode filter with an input resistance $R_i=0$ Ohm and a load resistance of $R_L=10$ kOhm.



$f_1=1.8$ [kHz]
$f_2=4.5$ [kHz]
$f_3=0.9$ [kHz]
$f_4=9.0$ [kHz]
$A_{min}=40$ [dB]
$A_{max}=1$ [dB]

Figure 7.11.1: The specification of the bandstop filter.

7.12. First-order GmC filter (Ex. 15.2 J&M)

Based on Figure 7.12.1, find component values for a first-order filter with a DC gain of 0.5, a pole at 20 MHz, and a zero at 40 MHz. Assume the integrating capacitors are $C_A=2$ pF.

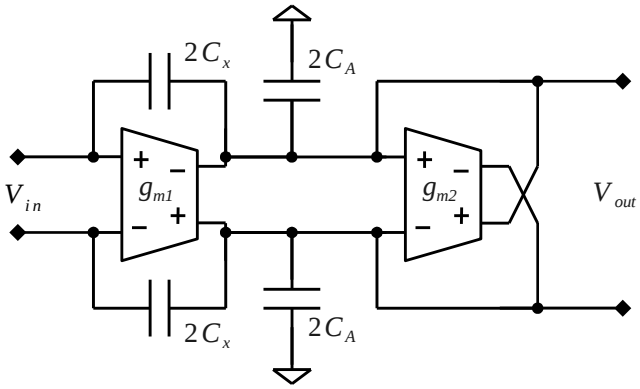


Figure 7.12.1: A fully differential general first-order Gm-C filter (J&M).

7.13. Second-order GmC filter (Ex. 15.3 J&M)

Find the transconductance and capacitor values for a second-order filter that has a bandpass response with a center frequency of 20 MHz, a Q value of 5, and a center frequency gain of 1.

Assume that $C_A=C_B=2$ pF.

7.14. Active filters (K11)

Realize the filter having the following transfer function

$$H(s)=\frac{10^6}{s^2+3\cdot10^5\cdot s+6\cdot10^{10}} \tag{30}$$

Use

a) Operational amplifiers

b) Gm-C elements.

Which solution gives you the most active components?

7.15. Active filters (K12)

Realize the filter having the transfer function

$$H(s)=\frac{-10^6\cdot(s-10^4)}{s^2+3\cdot10^5\cdot s+6\cdot10^{10}} \tag{31}$$

Use

a) Operational amplifiers
b) Gm-C elements.

Which solution gives you the most active components?

7.16. Active filters (K13)

Consider the filter in Figure 7.16.1.

a) Derive the transfer function for the circuit.
b) Sketch the signal flow chart using amplifiers, summations and integrators.
c) Also sketch the magnitude response.

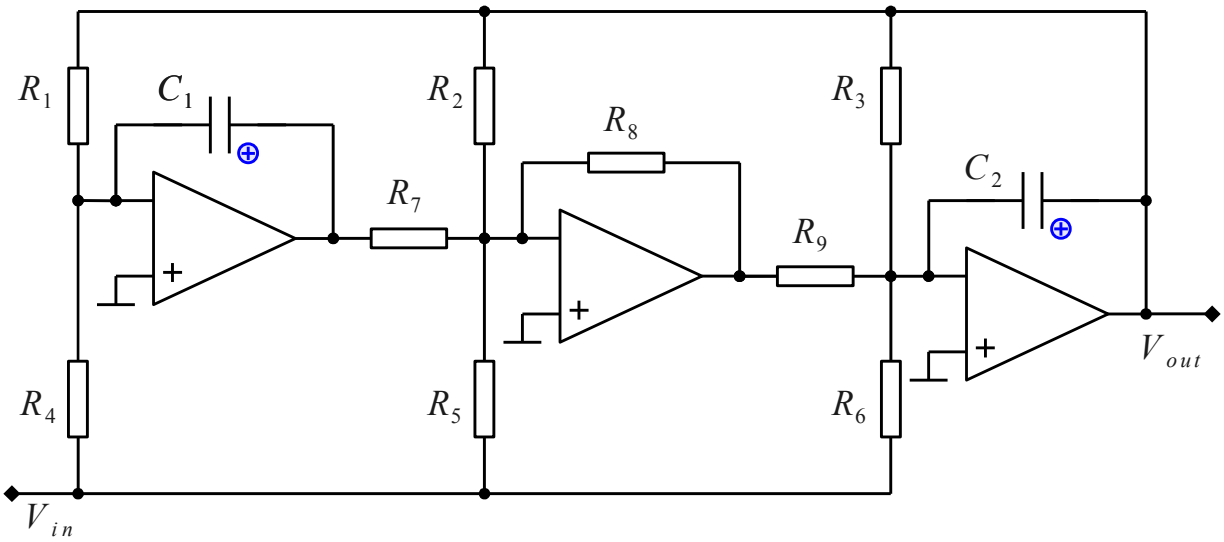


Figure 7.16.1: An active RC filter.

7.17. Active filters (K14)

Consider the filter in Figure 7.17.1.

a) Derive the transfer function for the circuit.

b) Sketch the signal flow chart using amplifiers, summations and integrators.

c) Also sketch the magnitude response.

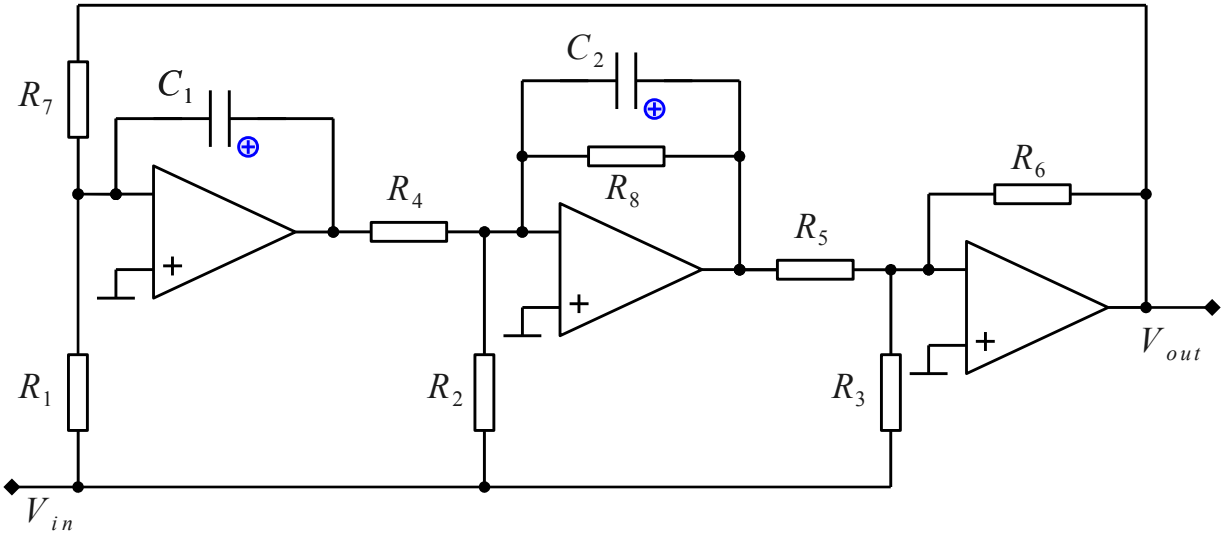


Figure 7.17.1: An active-RC filter.

7.18. Leapfrog filters (K15)

Design a continous-time Butterworth filter that meets the following specification:

Pass band: $0 \le f \le 3.5$ kHz, $A_{max} = 1$ dB

Cut-off band: $f \ge 10$ kHz, $A_{min} = 20$ dB

Use

a) RLC components

b) Active RC

c) MOSFET-C

d) Gm-C

Derive the values of all components and show the flow graphs you are using in each step. Termination resistances in corresponding passive RLC filter are supposed to be 1 kΩ. The order is found to be $N = 3$ and the normalized filter values are: $C_{3n} = 1$, $L_{2n} = 2$, and $C_{1n} = 1$.

7.19. Leapfrog filters (K16)

Design an active continuous-time elliptic leapfrogfilter with following specification:

Pass band: $0 \leq f \leq 1$ kHz, $A_{max} = 0.1$ dB

Cut-off band: $f \geq 2$ kHz, $A_{min} = 20$ dB

Use

a) RLC components
b) Active RC
c) MOSFET-C
d) Gm-C

Derive the values of all components and show the flow graphs you are using in each step. Termination resistances in corresponding passive RLC filter are supposed to be 1 kΩ. The order is found to be $N = 3$ and the normalized filter values are: $C_1' = C_3' = 0.8740$, $L_2' = 0.9083$, and $C_2' = 0.2411$.

7.20. Leapfrog filters (K17)

Synthesize a continuous-time lowpass butterworth filter of order $N = 2$ according to the following specification:

Pass band: $0 \leq f \leq 1$ kHz, $A_{max} = 1$ dB

Cut-off band: $f \geq 4$ kHz, $A_{min} = 12$ dB

Use

a) RLC components
b) Active RC
c) MOSFET-C
d) Gm-C

Derive the values of all components and show the flow graphs you are using in each step. Termination resistances in corresponding passive RLC filter are supposed to be 1 kΩ. The normalized filter values are: $C_1 = L_2 = 1.4142$.

7.21. Leapfrog filters (K18)

Synthesize a continuous-time lowpass elliptic filter of according to the specification:

Pass band: $0 \le f \le 1$ kHz, $A_{max} = 0.1$ dB

Cut-off band: $f \ge 2$ kHz, $A_{min} = 30$ dB

Use

a) RLC components

b) Active RC

c) MOSFET-C

d) Gm-C

Derive the values of all components and show the flow graphs you are using in each step. Termination resistances in corresponding passive RLC filter are supposed to be 1 kΩ. The order is found to be $N = 5$ and the normalized filter values are:

$C_{1n} = 1.05745$, $C_{2n} = 0.10836$, $L_{2n} = 1.25765$, $C_{3n} = 1.71457$,
$C_{4n} = 0.30465$, $L_{4n} = 1.04518$, $C_{5n} = 0.89926$.

7.22. Gyrators (K19)

Discuss the concept of gyrators.

a) Show some different ways to implement an inductor using active components.

b) Why don't you want to use passive inductors?

7.23. Gm-C filters (K20)

Discuss why floating resistors or capacitances should preferably not be used in a Gm-C filter.

7.24. Gm-C filter parasitics (K21)

How could the influence of parasitic capacitances in a Gm-C filter be reduced?

7.25. Gm-C filters (K22)

a) Determine the transfer function of the Gm-C circuit shown in Figure 7.25.1.

b) What is the cut-off frequency?

c) What is the Q factor of the circuit?

d) What are the disadvantages using this structure?

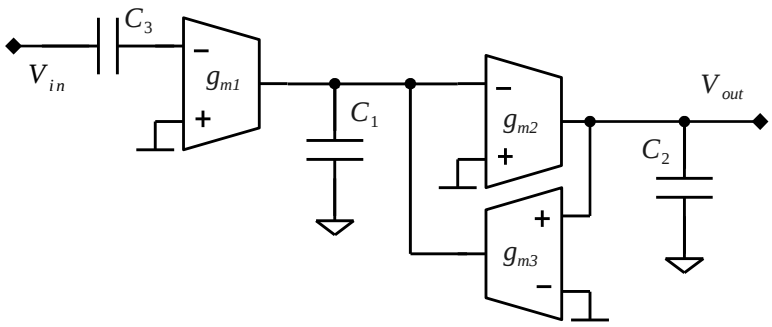


Figure 7.25.1: A Gm-C circuit.

EXERCISE SECTION 8: SWITCHED CAPACITOR CIRCUITS

✗ Notice that the "directions of the plates are only suggested.

8.1. Switched capacitor accumulator 1

Consider the switched capacitor circuit in Figure 8.1.1.

a) Derive the transfer function. Assume that the operational amplifier is ideal.

b) Is the circuit sensitive to parasitics? Why or why not?

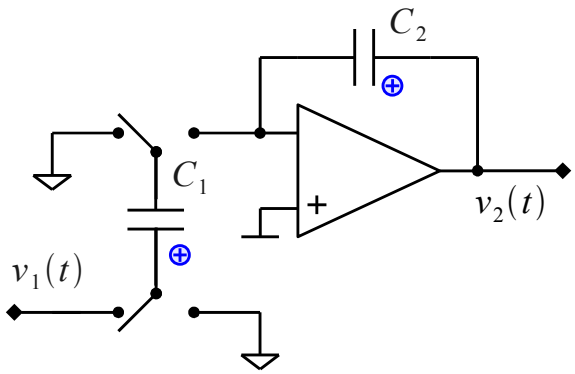


Figure 8.1.1: Switched capacitor circuit.

8.2. Switched capacitor accumulator 2

Consider the switched capacitor circuit in Figure 8.2.1.

a) Derive the transfer function of the circuit in Figure . Assume that the operational amplifier is ideal.

b) Is the circuit sensitive to parasitics? Why or why not?

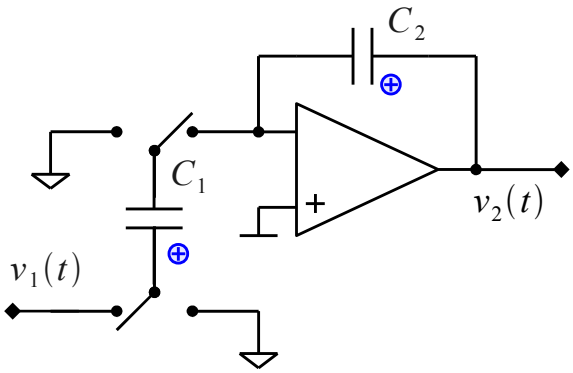


Figure 8.2.1: Switched capacitor circuit.

8.3. Switched capacitor circuit 1

Consider the switched capacitor circuit in Figure 8.3.1.

a) Derive the transfer function. Assume that the operational amplifier is ideal and that $C_3=2C_1$.

b) Is the circuit sensitive to parasitics? Why or why not?

c) What operation does the circuit perform?

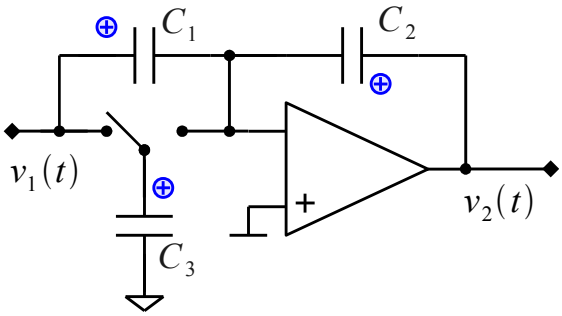


Figure 8.3.1: Switched capacitor circuit.

8.4. Switched capacitor circuit 2

a) Derive the transfer function of the switched capacitor circuit shown in Figure 8.4.1, i.e, $V_2(z)/V_1(z)$. Assume that the operational transconductance amplifier is ideal.

b) Is the circuit insensitive to parasitics? Motivate your answer clearly.

c) Assume that the operational transconductance amplifier suffers from finite gain, A, and input offset voltage, V_{os}. Derive the transfer function.

d) In general, what can you do to make the switched-capacitor circuit insensitive to offset errors?

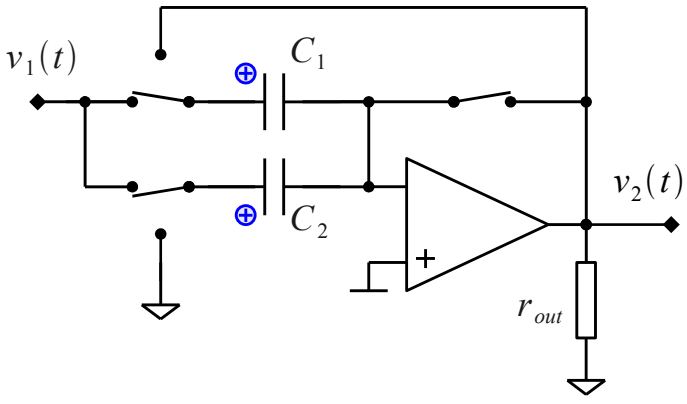


Figure 8.4.1: A switched capacitor circuit.

8.5. Switched capacitor circuit 3

The OTA (operational transconductance amplifier) in Figure 8.5.1 suffers from finite gain, A, and input offset voltage, V_{os}.

a) Derive the transfer function of the switched capacitor circuit shown in Figure , i.e., $V_2(z)/V_1(z)$.

b) Is the circuit insensitive to parasitics? Motivate your answer clearly.

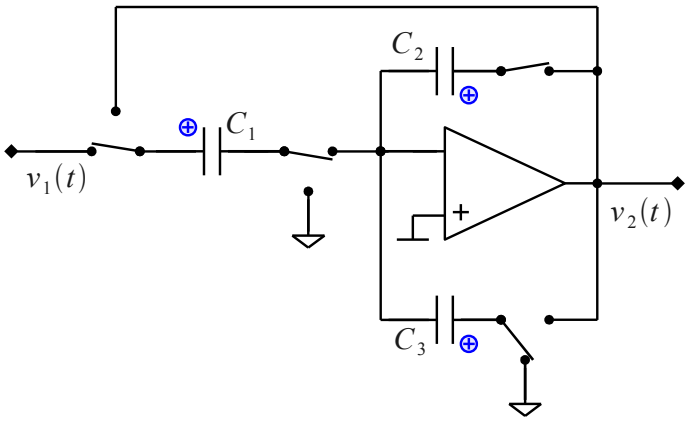


Figure 8.5.1: A switched capacitor circuit.

8.6. Switched capacitor circuit 4

Assume that the operational amplifier in Figure 8.6.1 is ideal except that it has an input offset voltage, V_{os}.

a) Derive the transfer function from V_1 to V_2 in Figure .

b) Is the circuit insensitive to parasitics?

c) Sketch a typical output voltage, $V_2(t)$, over five clock periods. Assume a DC-input voltage.

d) What will be the impact of the circuit if a capacitor is connected between the node to the right of capacitor C_3 and ground?

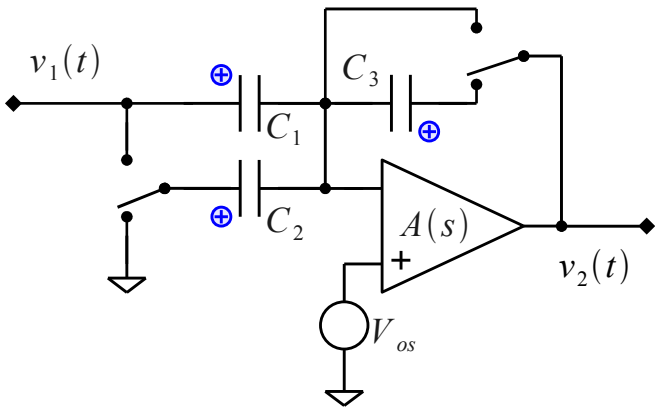


Figure 8.6.1: A switched capacitor circuit.

Assume that the operational amplifier is ideal except for a finite-gain, A, and an input offset voltage, V_{os}.

e) Derive the output voltage as a function of the amplifier parameters and the input voltage.

8.7. Switched capacitor circuit 5

Consider the switched capacitor circuit in Figure 8.7.1. The switches and OP are considered to be ideal.

a) Derive the transfer function of the circuit.

b) Investigate and explain if the circuit is parasitic insensitive or not.

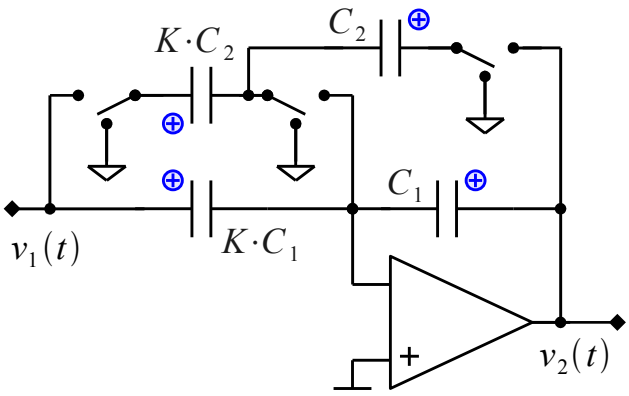


Figure 8.7.1: A switched capacitor circuit.

Still assume that the amplifier is ideal, but that the switches are MOS transistors. Further, assume that the circuit is to be used in a quantizing circuit (A/D converter).

c) How would the on-resistance of the transistors affect the transfer function? Which other parameters do you have to change to compensate for the limited on resistance?

8.8. SC circuit (K25)

Derive the transfer function for the SC circuit in Figure 8.8.1, when

a) $C_1 = C_2$

b) $C_1 = 1.12 \cdot C_2$ (Why is 1.12 selected?)

Then, for one of the cases, do the following:

c) Sketch the pole/zero placement and the amplitude characteristics.

d) What kind of a circuit is this?

e) Is the circuit sensitive to parasitics?

f) What will happen if the operational amplifier is nonideal?

g) Derive the feedback factor of both phases.

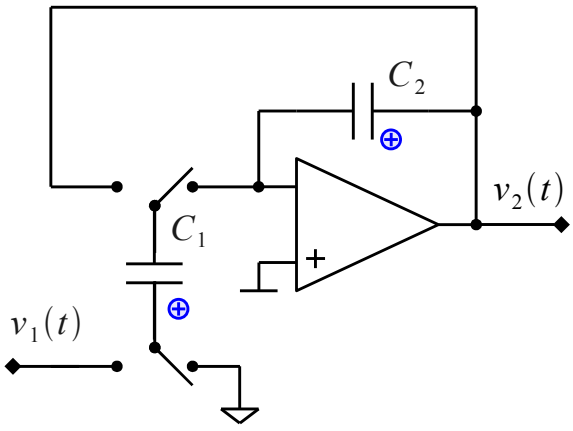


Figure 8.8.1: SC circuit.

8.9. SC circuit (K26)

a) Derive the transfer function for the SC circuit in Figure 8.9.1.

b) How should the capacitances be chosen if the circuit is to be used as a sample-and-hold circuit?

c) Is the circuit sensitive to parasitics?

d) What will happen if the operational amplifier is non-ideal?

e) Derive the feedback factor of both phases.

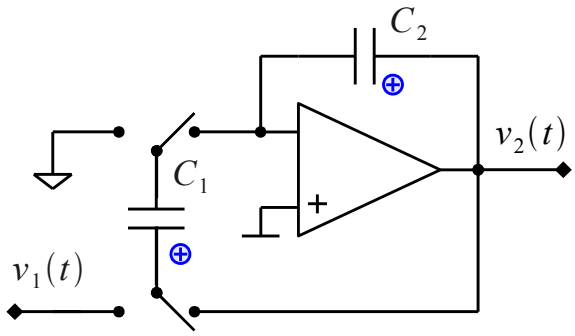


Figure 8.9.1: SC circuit.

8.10. SC circuit (K27)

a) Derive the transfer function for the SC circuit in Figure 8.10.1.

b) How should the capacitances and the input voltage v_1 be chosen if the circuit is to be used as an all-pass filter?

c) Is the circuit sensitive to parasitics?

d) What will happen if the operational amplifier is non-ideal?

e) Derive the feedback factor of both phases.

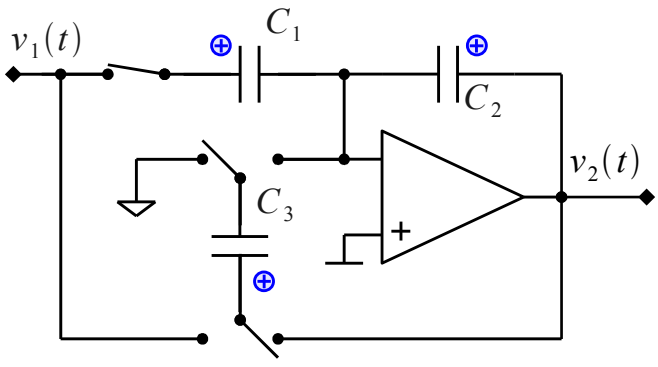


Figure 8.10.1: SC circuit.

8.11. SC circuit (K28)

a) Derive the transfer function for the SC circuit in Figure 8.11.1.

b) Which operation does the circuit perform?

c) Why is the value sampled over two equally large capacitances?

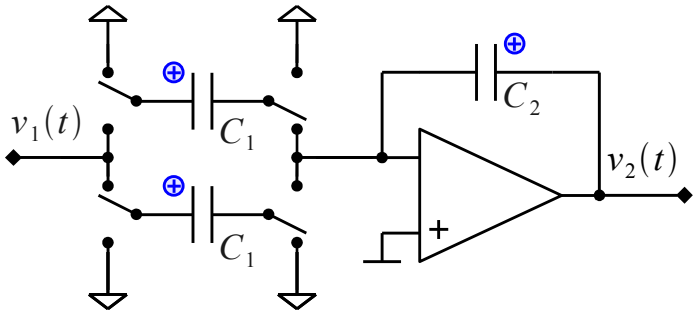


Figure 8.11.1: SC circuit.

8.12. Clock feedthrough (K29)

a) Discuss what techniques to use to minimize the influence of CFT, clock feedthrough. What advantages and disadvantages can be found with these techniques?

b) Also explain how different clock phases should be chosen in a SC circuit.

c) Why do they have to be non-overlapping?

8.13. Switch sharing (K30)

Discuss the concept of switch sharing in switched-capacitor circuits.

8.14. SC circuit (K37)

Consider the switched-capacitor circuit in Figure 8.14.1.

a) What dependence is there between the input and output signal?

b) How is the transfer function depending on the input signal?

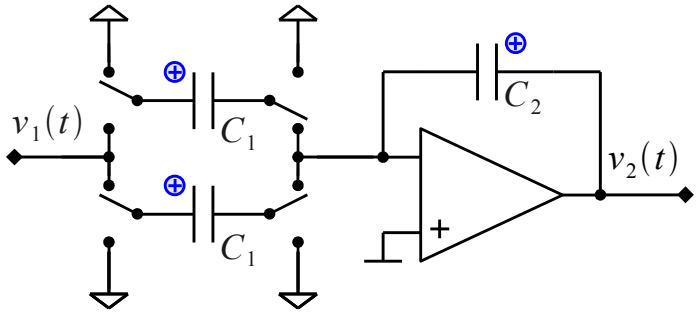


Figure 8.14.1: An SC circuit.

8.15. Signal switching (K39)

Concludingly, how should the signals be switched to minimize the influence of parasitic capacitances (in the switches) for a switched-capacitor circuit?

8.16. Sampled noise (K24)

Noise in switched-capacitor circuits is a tricky problem...

a) Discuss how sampled noise can be modelled.

b) What specific phenomenon occur when considering the $1/f$ noise?

EXERCISE SECTION 9: SC FILTERS

✗ Designing the SC filter is a bit of a tedious exercise and hence we only provide one master template. The idea follows the continuous-time approach where you replace the active components with discrete-time integrators or corresponding SC simulation of resistors. Further on, the transfer characteristics and the component values are fine tuned using an optimization software.

9.1. SC filter building blocks (K36)

a) Derive the transfer function for the SC circuit in Figure 9.1.

b) Sketch the amplitude characteristics.

c) What operation does the circuit perform?

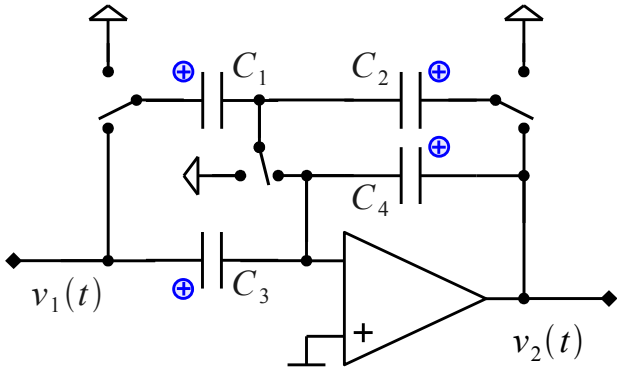


Figure 9.1: SC circuit.

9.2. Bilinear integrator (K38)

What conditions must be fulfilled when the circuit in Figure 9.2.1 can be used as a bilinear integrator? A bilinear relation is given by

$$s=\gamma\cdot\frac{z-1}{z+1} \tag{32}$$

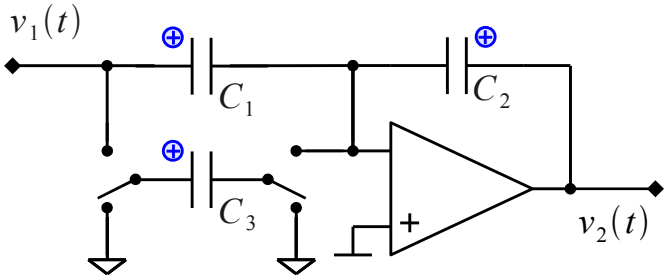


Figure 9.2.1: An SC circuit.

9.3. LDI transform (K31)

Suppose that for the LDI transformation the following expression is used

$$s = z^{0.5} - z^{-0.5} = \frac{1 - z^{-1}}{z^{-0.5}} \tag{33}$$

The constant s_0 is set to unity.

> How should a reference filter in this case be (frequency) scaled to get the wanted mapping from the s-plane to the z-plane.

9.4. LDI transform (K32)

What properties must a filter have if the LDI transform shall be used.

9.5. SC filter 1

Design a third-order LP filter with a cut off angle $\omega_c T = \pi/30$. Use a Chebychev I type approximation with $A_{max} = 0.1$ dB. Use the LDI-transformation.

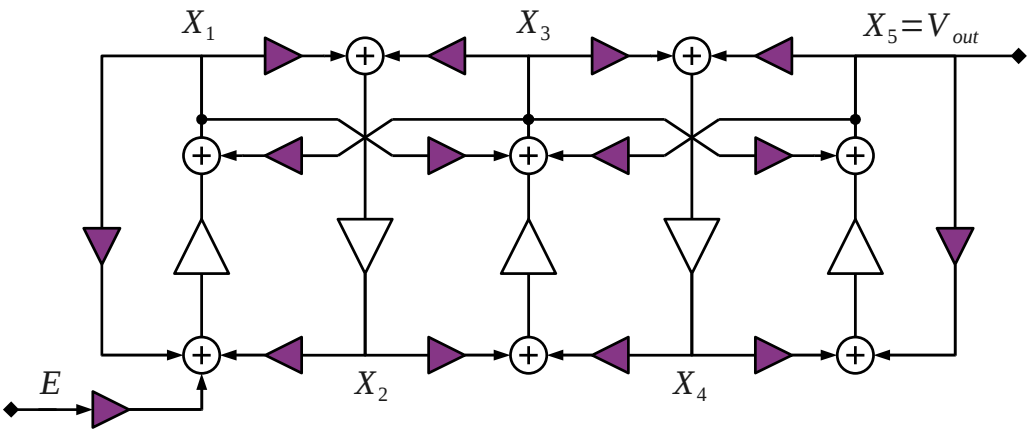


Figure 9.5.1: A fifth-order elliptic leapfrog filter.

9.6. Filter scaling (K23)

Scale the filter in Figure 9.5.1 such that $|X_i / E|_{max} = 1$ for each node X_i. Find the scaling parameters.

The (nominally) measured maximum values are:

$|X_1 / E|_{max} = 0.92$ for $\omega T = 41^o$, $|X_2 / E|_{max} = 1.33$ for $\omega T = 39^o$
$|X_3 / E|_{max} = 0.86$ for $\omega T = 37^o$, $|X_4 / E|_{max} = 1.25$ for $\omega T = 37^o$
and $|X_5 / E|_{max} = 0.50$ for $\omega T = 0^o$

9.7. LDI SC filter (K33)

Design an LDI filter that fulfills the attenuation specification according to Figure 9.7.1. Choose a Butterworth reference filter. Compensate the filter so that errors due to transformation approximations are minimized.

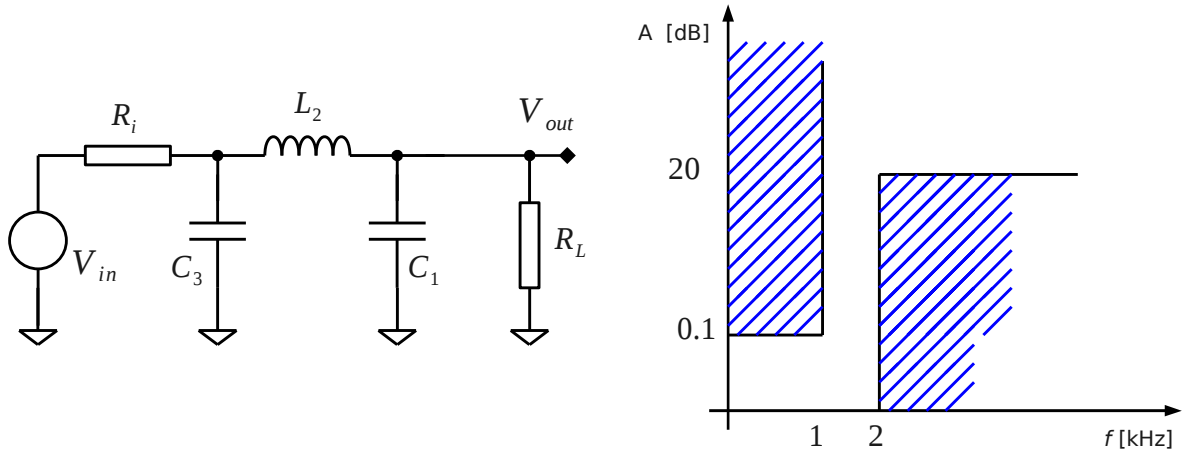


Figure 9.7.1: An LP filter prototype and specification.

Scale the internal nodes of the filter.

The order is found to be $N=3$. The normalized values found from a table are $C_{3n}=1$, $L_{2n}=2$, $C_{1n}=1$, and $R_i=R_L=1$ kOhm.

9.8. SC elliptic filter (K34)

The SC-filter in Figure 9.8.1 simulates an elliptic reference filter. The filter is not scaled and the gain is not at its maximum of 0 dB.

a) How large is the gain?

b) What components in the circuit should be changed (and how much) to achieve a maximum gain?

The values are given by:

$$\alpha_1=C_1+C_2-\frac{1}{2\,s_0 R_i},\quad \alpha_2=C_2+C_3-\frac{1}{2\,s_0 R_L}$$

$$a_0=a_1=a_2=\frac{1}{s_0 R\,\alpha_1},\quad a_5=a_6=\frac{1}{s_0 R\,\alpha_2},\quad a_3=a_4=\frac{R}{s_0 L_2} \qquad (34)$$

$$b_1=\frac{C_2}{\alpha_1},\quad b_2=\frac{C_2}{\alpha_2},\quad R=R_i=R_L$$

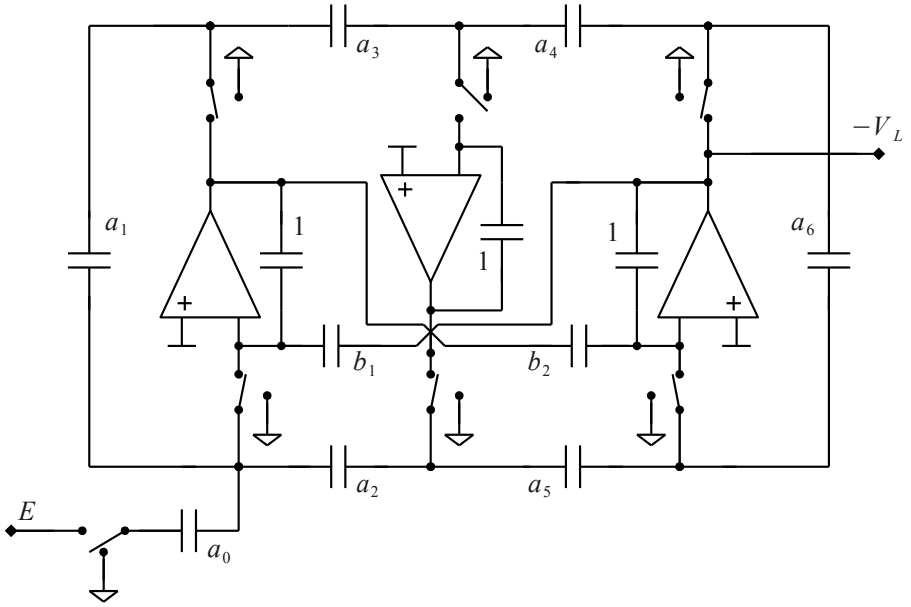


Figure 9.8.1: An SC filter.

9.9. SC filter (K35)

Design a third order SC low pass filter with cut- off frequency $f_c=3.4$ kHz and sampling frequency $f_s=128$ kHz. The ripple in the pass band is less than 0.02 dB.

Choose an elliptic reference filter with modular angle 20° . Design a leapfrog scheme that is mapped to the discrete-time domain using the LDI transformation. Compensate the filter so that errors due to transformation approximations are minimized. Normalized values from table are:

$$R_i=R_0=1 \text{ kOhm},\ C_{1n}=C_{3n}=0.5275,\ C_{2n}=0.1921,\ L_{2n}=0.7700 \quad (35)$$

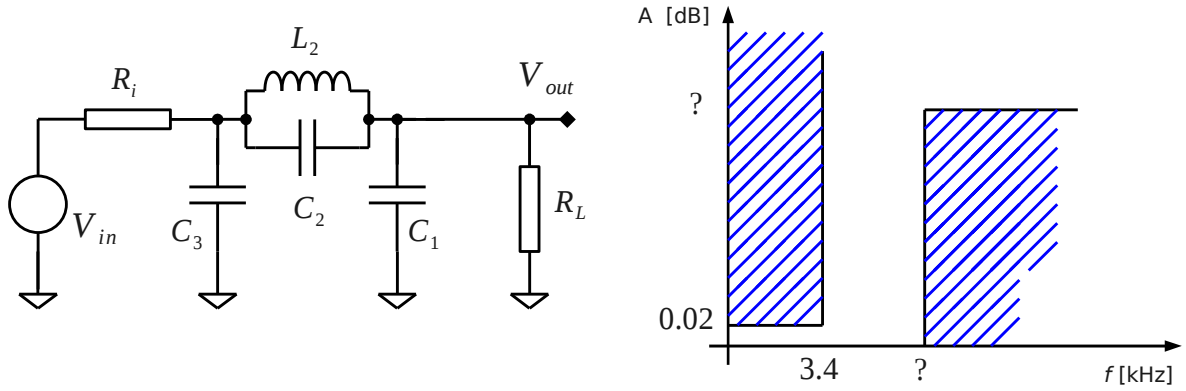


Figure 9.9.1: An SC filter.

9.10. SC filter (K40)

Synthesize an LDI filter that fulfils the specification. Choose an elliptic reference filter.

Compensate the filter so that errors due to transformation approximations are minimized.

a) Describe how the filter can be scaled, and why.

Values found from table are:

Order $N=3$,
$\kappa^2=1$, hence $R_i=R_0=1$ kOhm (36)

Normalized component values are:

$C_{1n}=C_{3n}=1.9314$, $C_{2n}=0.3781$, and
$L_{2n}=0.7571$. (37)

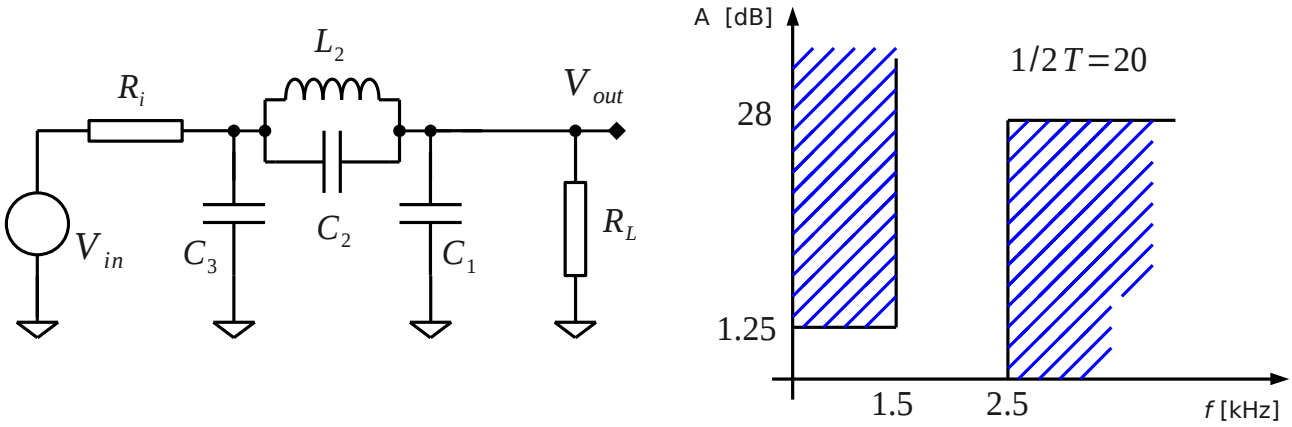


Figure 9.10.1: An SC filter prototype and specification.

EXERCISE SECTION 10: DATA CONVERTERS, FUNDAMENTAL

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10.1. D/A swing (Q 11.1 J&M)

For an ideal 10-bit, unipolar D/A converter with the $V_{LSB}=1$ mV, what is the largest possible output swing?

10.2. SNR (Q 11.2 J&M)

Consider an analog-to-digital converter.

a) What is the signal-to-noise ratio (SNR) for an ideal 12-bit unipolar A/D converter with $V_{ref}=3$ V, when a sinusoidal input of 1 V (peak-to-peak) is applied?

b) What size input would result in an SNR of 0 dB?

10.3. Coding (Q 11.3 J&M)

For an offset binary D/A converter, the output voltage would be given by

$$V_{out}=V_{ref}\cdot\left(b_1\cdot 2^{-1}+b_2\cdot 2^{-2}+\ldots+b_N\cdot 2^{-N}\right)-0.5\,V_{ref} \tag{38}$$

Find the equivalent of 38) for 2's complement coding.

10.4. Word length effects (Q 11.4 J&M)

Show that, by using 4-bit 2's-complement words, the correct final sum is obtained when the numbers +5, -5, and -7 are added together while any overflow effects are ignored.

10.5. Sign extension (Q 11.5 J&M)

Starting with two 5-bit 2's -complement words, we want to add +5 and +7 to obtain the correct answer of +12 with a 5-bit word.

Show how an extra bit can be added at the "left" of each of the 5-bit words such that numbers up to +/- 15 can be represented.

✗ This approach is called sign extension and can be used to increase the word size of any number.

10.6. Representation (Q 11.6 J&M)

What is the representation of +8 and -8 in 5-bit 2's complement?

Assuming a circuit added only one of these two numbers to an arbitrary 5-bit word, show a simple logic circuit (i.e., NAND, NOR, XNOR, etc.) that would accomplish such an addition.

> ✗ Note that the four LSBs in +8 and -8 are all 0 and thus do not need to be added.

10.7. INL/DNL (Q 11.7 J&M)

The following measurements are found from a three-bit unipolar D/A converter with $V_{ref}=8$ V:

-0.01, 1.03, 2.02, 2.96, 3.95, 5.02, 6.00, 7.08 V

In units of LSBs, find the offset error, gain error, maximum DNL, and maximum INL.

10.8. (Q 11.8 J&M)

How many bits of **absolute accuracy** does the converter in Exercise 10.7 have? How many bits of **relative accuracy** does it have?

10.9. (Q 11.9 J&M)

A 10-bit A/D converter has a reference voltage, V_{ref}, tuned to 10.24 V at room temperature. Find the maximum allowable temperature coefficient in terms of microVolts per centigrade for the reference voltage if the reference voltage is allowed to cause a maximum error of +/- 0.5 LSB oevr the temperature range of 0 to 50 degrees.

10.10. (Q 11.10 J&M)

Consider the following measured voltages for a 2-bit D/A with a reference voltage of 4 V:

00: 0.01 V, 01: 1.02 V, 10: 1.97 V, 11: 3.02 V.

In units of LSBs, find the offset error, gain error, worst absolute and relative accuracies, and worst differential nonlinearity. Restate the relative accuracy in terms of an N-bit accuracy.

10.11. (Q 11.11 J&M)

Find the maximum magnitude of quantization error for a 12-bit A/D converter having V_{ref} equal to 5 V and 0.5-LSB absolute accuracy.

EXERCISE SECTION 11: DATA CONVERTERS, DAC

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11.1. Resistor-string DAC (Q 12.2 J&M)

Assume that an 8-bit resistor-string D/A converter with digital decoding **(see Figure 11.1.1)** has a total resistor-string resistance of 400 Ohms, that is pass transistors have an on-resistance of 400 Ohms, and that the drain-source capacitances to ground of its pass transistors are 0.1 pF.

Ignoring all other effects and using the open-circuit time-constant approach, estimate the worst-case settling time to 0.1 percent.

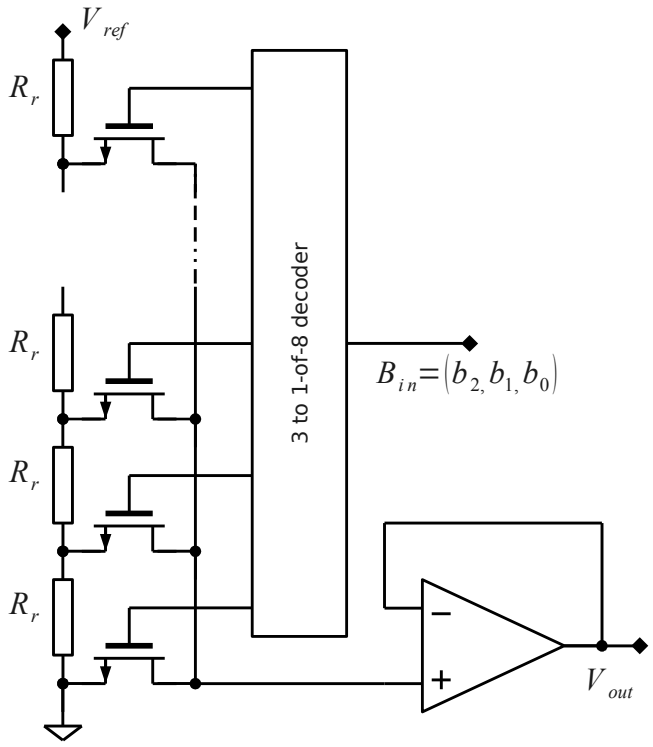


Figure 11.1.1: Resistor-string three-bit D/A converter with digital decoding.

11.2. Multiple resistor-string DAC (Q 12.4 J&M)

Assume that the first resistors string of a 10-bit multiple-R-string D/A converter (see Figure 11.2.1) must match to 0.1 percent whereas the second string must match to 1.6 percent since the converters realize the top four bits and lower six bits, respectively.

For $V_{ref}=5$ V. how much offsets in the opamps can be tolerated?

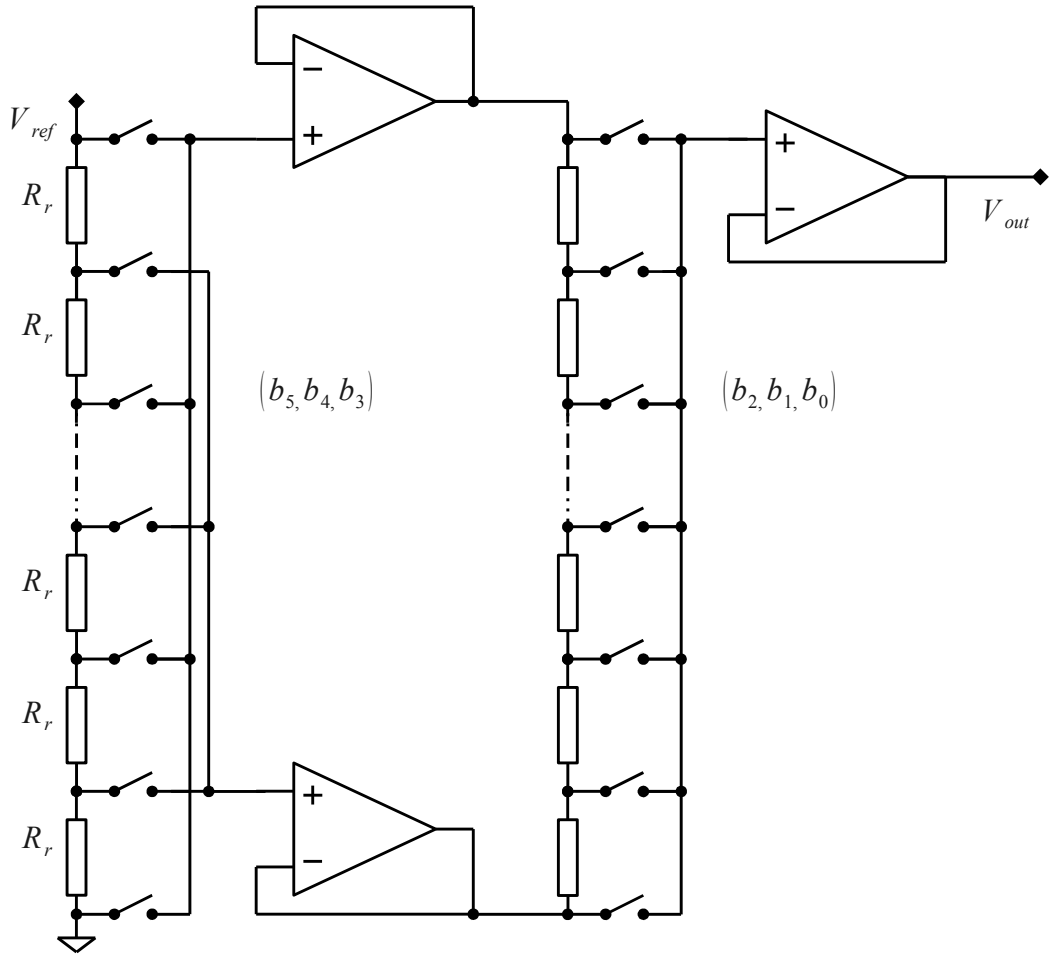


Figure 11.2.1: Multiple R-string 6-bit D/A converter.

11.3. Binary-weighted DAC (Q 12.5 J&M)

For a binary-weighted 10-bit resistor D/A converter (see a 4-bit example in Figure 11.3.1), assume that R_F is chosen such that the output goes from 0 to $V_{ref} - V_{LSB}$.

What is the resistor ratio between the largest and smallest resistors?

What is the ratio between the currents through the switches for b_1 and b_{10}?

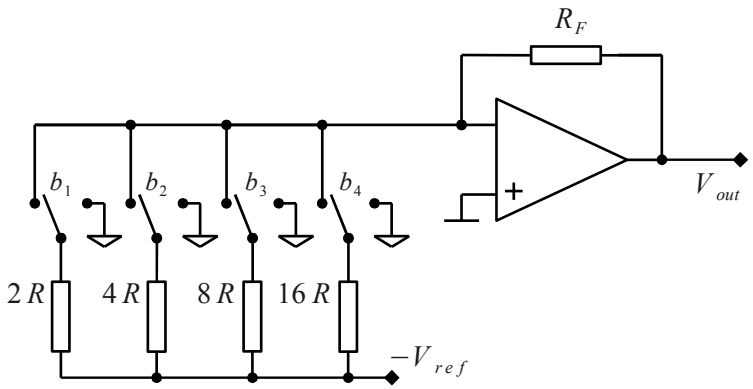


Figure 11.3.1: Binary-weighted 4-bit resistor D/A converetr.

11.4. R-2R ladder DAC (Q 12.11 J&M)

For the 4-bit R-2R-ladder D/A converter shown in **Figure 11.4.1**, what is the output error (in LSBs) when $R_A = 2.01 \cdot R_B$?

What is the output error when $R_C = 2.01 \cdot R$?

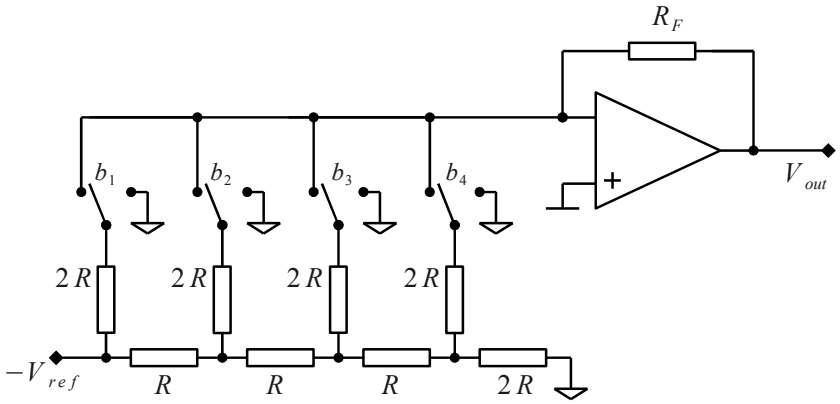


Figure 11.4.1: Four-bit R-2R ladder D/A converter.

11.5. Current-steering DAC (Q 12.17 J&M)

A D/A converter is realized using dynamically matched current sources, as shown in Figure 11.5.1. Assuming all the transistors are ideal, find W/L for the Q_1 needed to set $V_{GS}=3$ V when $I_{ref}=50$ uA, $V_t=1$ V and $\mu_n C_{ox}=93$ uA/V.

If switch S_1 causes a random charge injection voltage of 1 mV what is the expected percentage of random variation of the current being held on Q_1?

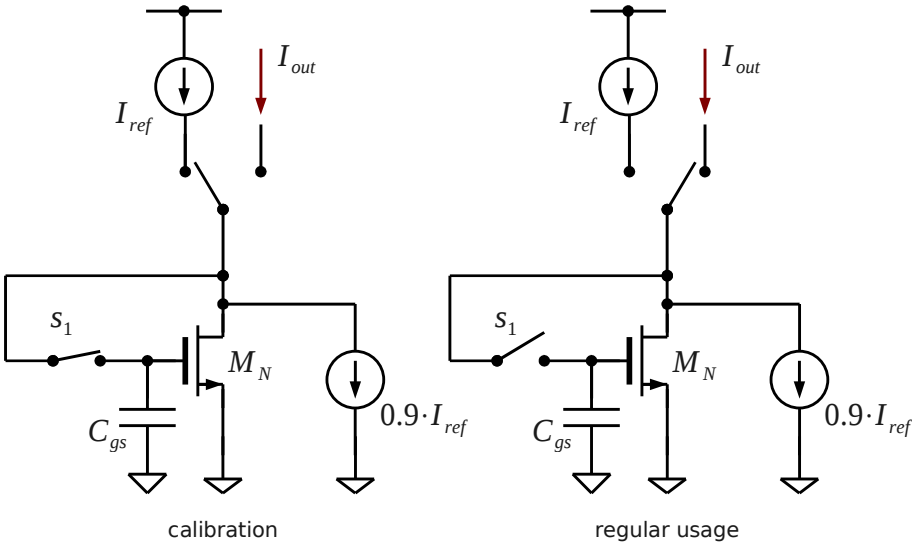


Figure 11.5.1: Dynamically setting a current source, I_{dI}.

EXERCISE SECTION 12: DATA CONVERTERS, ADC

x Covered by the course book. Notice that this is copyright material! I am here stressing that the exercises are copied (sometimes with minor modifications) from the Johns and Martin book. The local distribution (this material is not found on the web) is legal according to the copyright laws (number of pages sufficiently low and material used for educational purposes).

12.1. Integrating ADC 1 (Q 13.1 J&M)

What is the worst-case conversion time for an 18-bit dual-slope integrating A/D converter (as shown in Figure 12.1.1), when the clock rate is 5 MHz?

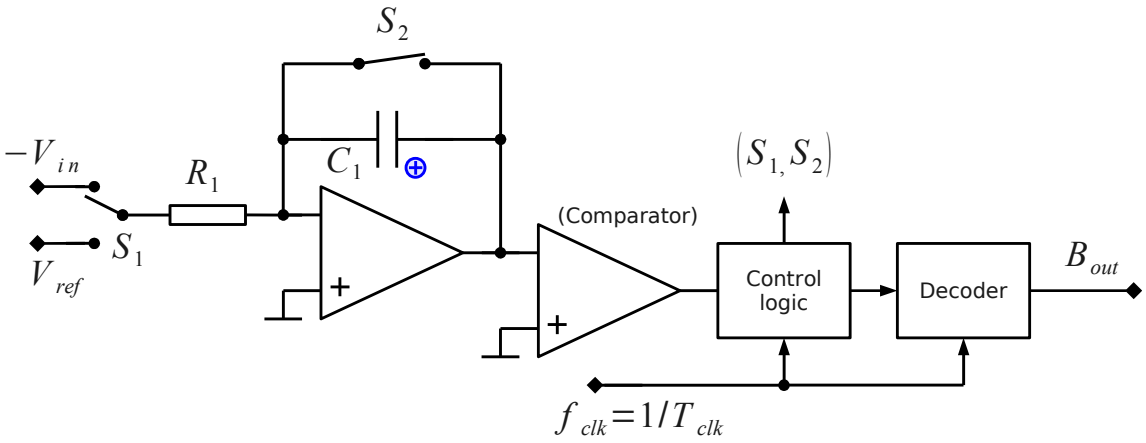


Figure 12.1.1: Integrating (dual slope) A/D converter.

12.2. Integrating ADC 2 (Q 13.2 J&M)

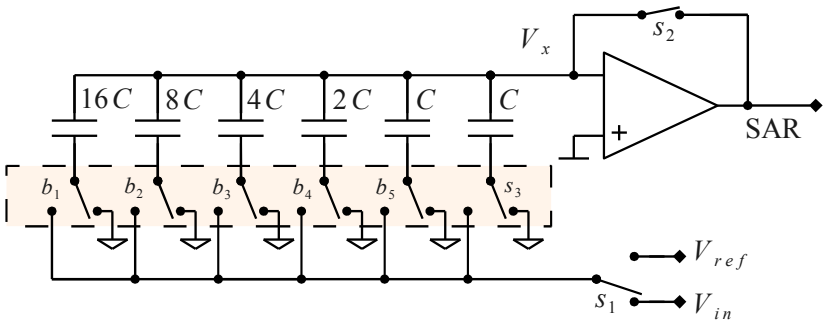
Consider an 18-bit integrating A/D converter, as shown in Figure 12.1.1, where V_ref equals 10 V. C_1 = 100 pF, and a clock frequency of 1 MHz is used.

What value of R_1 should be chosen such that the opamp output never exceeds 10 V when $0 < V_{in} < 10$ V?

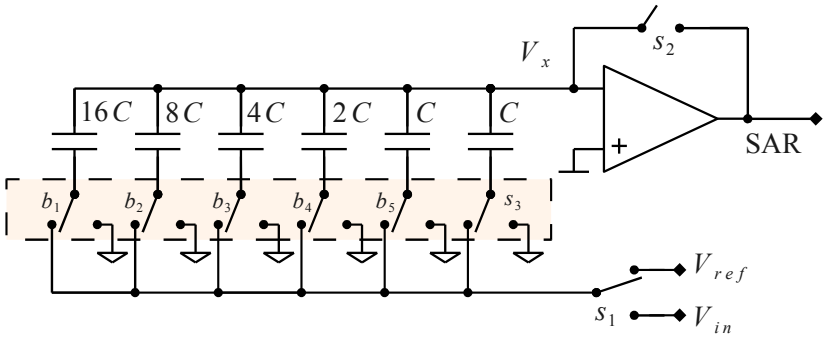
12.3. Charge redistribution DAC (Ex. 13.3 J&M)

Find the intermediate node voltage at V_x during the operation of the 5-bit charge-redistribution converter shown in Figure 12.3.1 when $V_{in} = 1.23$ V and $V_{ref} = 5$ V.

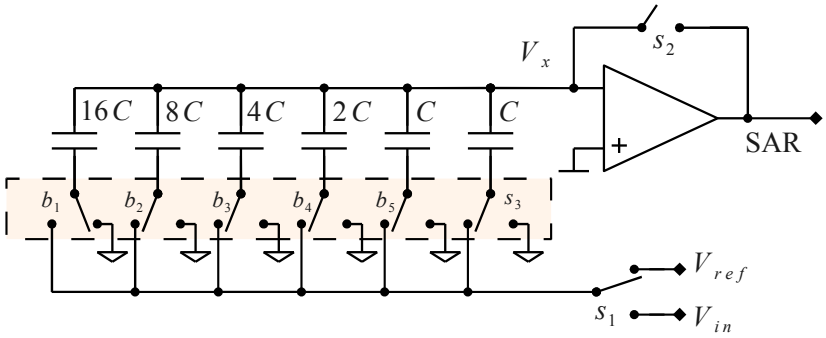
Assume a parasitic capacitance of $C_p = 8C$ exists on the node at V_x.



Sample mode



Hold mode



Bit cycling

Figure 12.3.1: A 5-bit unipolar charge-redistribution A/D converter.

12.4. Oversampling 1 (Q 14.1 J&M)

Assuming oversampling with no noise shaping and using equation 39) below, find the approximate sampling rate required to obtain a maximum SNR of 80 dB on a signal with a 1-kHz bandwidth using a 1-bit quantizer.

$$\mathrm{SNR}=6.02\cdot N+1.76+10\cdot\log_{10}(\mathrm{OSR}) \tag{39}$$

12.5. Oversampling 2 (Ex. 14.3 J&M)

Given that a 1-bit A/D converter has a 6-dB SNR, what sample rate is required using oversampling (no noise shaping) to obtain a 96-dB SNR (i.e., 16 bits) if $f_0=25$ kHz.

✗ The input into the A/D converter has to be very active for the white-noise quantization model to be valid - a difficult arrangement when using a 1-bit quantizer with oversampling without noise shaping!

12.6. Modulators 1 (Ex. 14.4 J&M)

Find the output sequence and state values for a DC input, $u(n)$, of 1/3 when a two-level quantizer of ± 1.0 is used (threshold at zero) and the initial state for $x(n)$ is 0.1. Use the modulator model as in Figure 12.6.1.

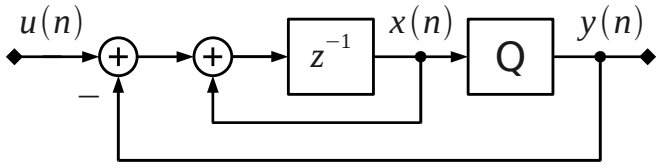


Figure 12.6.1: A first-order noise-shaped interpolative modulator.

12.7. Modulators 2 (Q 14.4 J&M)

Repeat exercise 12.6, except use an input sequence of (10, -10, 10, -10, 10, -10, ...) to see if the internal state of the modulator saturates.

✗ This problem demonstrates that a large level input signal can be applied to a modulator if its signal power resides at a frequency where the gain of $H(z)$ is low.

12.8. Oversampling 3 (Ex 14.5 J&M)

Given that a 1-bit A/D converter has a 6-dB SNR, what sample rate is required to obtain a 96-dB SNR (or 16 bits) if $f_0 = 25$ kHz for straight oversampling, as well as first- and second-order noise shaping?

EXERCISE SECTION 13: TRANSMISSION LINES

13.1. Transmission line basics

A transmission line of length L connects a load to a sinusoidal voltage source with an oscillation frequency f. Assuming that the velocity of wave propagation on the line is c.

For which of the following situations is it reasonable to ignore the presence of the transmission line in the solution of the circuit (and why? Figure 13.1.1 might help you.).

a) $L=20$ cm, $f=20$ kHz

b) $L=50$ km, $f=60$ Hz

c) $L=20$ cm, $f=600$ MHz

d) $L=1$ mm, $f=100$ GHz

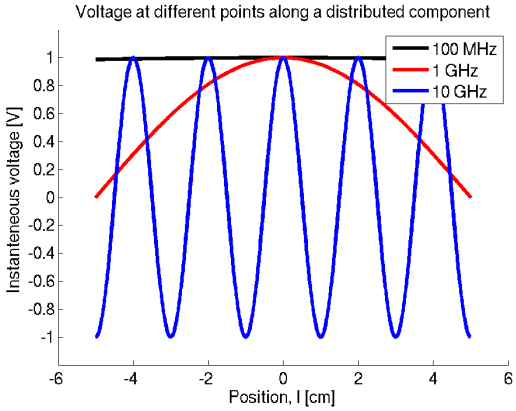


Figure 13.1.1: Example of a (normalized) wave through a physical distance.

13.2. Reflections

✗ This exercise also exists in the andaLectureTest lab library.

Assume a transmission line with characteristic impedance of

$Z_0=50$ Ω and source resistance of $R_S=1$ Ω.

The load resistance is $R_L=1000$ Ω and the input voltage describes a step function from 0 to 5 Volts at $t=0$.

The speed-of-propagation is u =20 cm/ns. The transmission line is 20 cm long.

a) What are the reflection coefficients at both ends?

b) Find the voltage across the load resistor as a function of time.

c) What is the final voltage at the load resistor.

13.3. Matched loads

✗ This exercise also exists in the andaLectureTest lab library.

Assume a transmission line with characteristic impedance of

$Z_0=50$ Ω, and source resistance of $R_S=25$ Ω.

The load resistance is $R_L=50$ Ω and the input voltage describes a step function from 0 to 5 Volts at $t=0$.

The speed-of-propagation is u =20 cm/ns. The transmission line is 20 cm long.

a) What are the reflection coefficients at both ends?

b) Find the voltage across the load resistor as a function of time.

c) What is the final voltage at the load resistor.

13.4. DC termination

Assume you have a transmission line with a characteristic impedance of

$Z_0=50$ Ω, and source resistance of $R_S=67$ Ω

The termination load consists of two resistors, one from supply to the end point and one to ground from the end point. Call them R_1 and R_2, respectively. The input describes a step from 0 to 3.3 Volts at $t=0$.

a) Dimension R_1 and R_2 to provide matched load and a DC voltage of 0.75 V.

b) Calculate the current through the driver for the high and low states.

c) With the "traditional" termination (only resistor R_2), what would be the current through the driver for high and low states?

d) Which configuration, b or c, consumes most power?

13.5. Series termination

Consider the scenario in Figure 13.5.1. You have a transmisssion line connecting from the “left” and another one connecting from the “right” to a small resistive network.

a) From each side of this whole system – what are the reflection coefficients?

b) How much power is transferred from the left-hand side?

If you need to, you might have to assume something about the termination of the transmission lines in their respective ends.

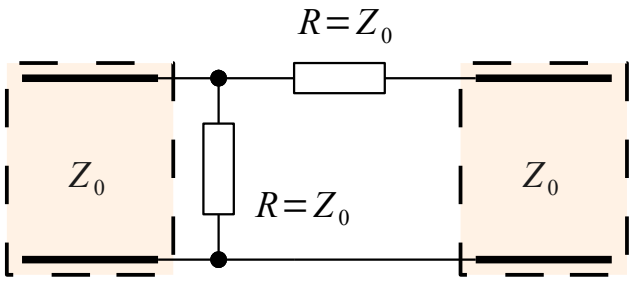


Figure 13.5.1: Parallel/series termination of a transmission line.

13.6. Splitted transmission lines

Consider the scenario in Figure 13.6.1. There are two transmission lines connecting to one point. This would for example be a wire distributed to two different chips at two different

places on the PCB. One of them has a characteristic impedance of 50 Ohms, the other 75 Ohms and they are of different length. L corresponds to the wavelength of your signal, from which you can also derive the frequency of operation. The load impedance in one end is open-circuit and in the other end it is a 70-resistance and some capacitive part (10j).

a) Derive the input impedance to the network such that you can dimension the source termination.

b) Suggest a termination for the currently unterminated wire to possibly improve the scenario. Explain and how.

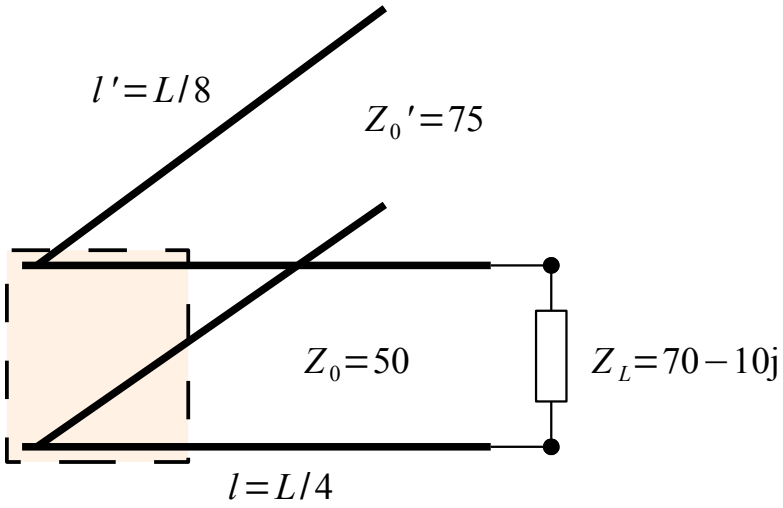


Figure 13.6.1: Example of a splitted wire.

13.7. Termination

Consider the circuit in Figure 13.7.1. It has a transmitter and a receiver on two chips. The transmission line is on a PCB with a good ground plane. The transmitter has an output resistance of R_{out} and the receiver has an input resistance of R_{in}. The transmission line has a characteristic impedance of Z_0. The length of the line is 5 cm, and the propagation speed through the line is $v = 2 \cdot 10^8$ m/s.

Further on, we also know that: $R_{out} = 25$ Ohm, $Z_0 = 50$ Ohm, and $R_{in} = 75$ Ohm. The transmitter will ideally output 1-V voltage pulses with a very short rise/fall time, internally.

a) Once the pulses start to be transmitted over the line, sketch the diagram showing the voltage at the receiver input **as function of time.**

b) What are the reflection constants at the receiver and transmitter?

✗ You are allowed to modify the PCB in a way that you can add termination in series and parallel.

c) Modify the PCB such that you have maximum power transfer from the transmitter to the receiver.

d) Modify the PCB such that you have a minimum number of reflected waves traveling back-and-forth.

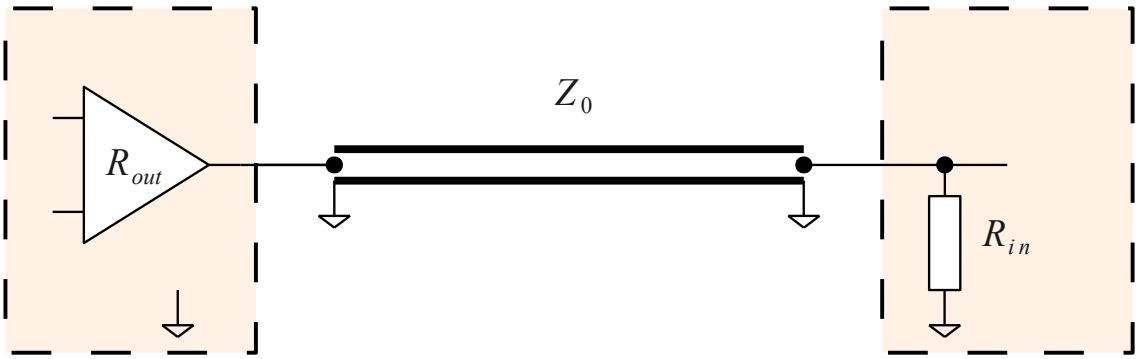


Figure 13.7.1: A circuit communicating with another circuit over a transmission line.

EXERCISE SECTION 14: DECOUPLING CAPACITORS AND POWER SYSTEMS

14.1. Board-level bypass capacitor

Assume a CMOS PCB having 100 gates each switching 10 -pF loads in 5 ns between ground and supply. The power supply inductance is 100 nH.

Find the right value of a bypass capacitor such that the power supply noise is kept below 0.1 V.

14.2. Highest effective frequency of a bypass “decap” (decoupling capacitor)

From the previous exercise (14.2), assume that a 10-uF “decap” (decoupling capacitor) has a series inductance of $L_{c2}=5$ nH. We were working to achieve a reactance of $X_{max}=0.1\,\Omega$.

Find the maximum frequency at which the decap is still effective.

14.3. Non-ideal decaps

Consider the two decoupling (bypass) capacitors in Figure 14.3.1. They are typically used to filter out any high-frequency noisy signals along the supply wire. In the figure, we also see the model of the decoupling capacitor with the nonideal components ESR and ESL.

Assume that the nominal capacitance values, C0 and C1, can be different, but that the ESR and ESL are the same for the two capacitors.

a) Sketch the impedance of one capacitor, for example C0, as a function of frequency. Identify any extreme points/characteristics along the curve and explain them.

b) Sketch the impedance of the combined pair of capacitors, i.e., C0 and C1, as a function of frequency. In this part, assume the capacitance in C0 is much smaller than that of C1. Identify any extreme points/characteristics along the curve and explain them.

c) Calculate the resonance frequency of two non-ideal decaps in parallel.

d) What is the minimum impedance between ground and supply that can be obtained with the two capacitors? When does this happen?

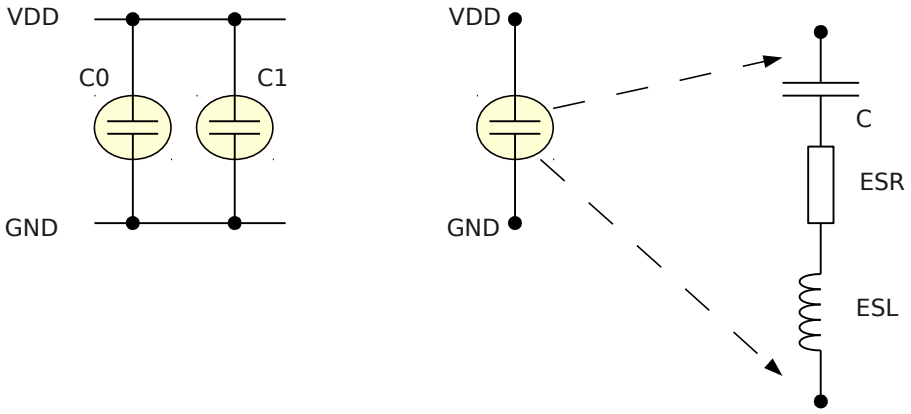


Figure 14.3.1: Two decoupling capacitors in parallel (left) and their model (right).

14.4. To be added

✗ To be added. Ta från tentan.

14.5. To be added

✗ To be added. Ta från tentan.

EXERCISE SECTION 15: TIMING AND MISCELLANEOUS

✗ Fråga Reza vad han tänkt sig här?

15.1. Loop filter of a PLL

Find the loop filter gain constant K_{lp} and ω_z for the circuit with a C_2 in parallel with R_1 and C_1 which are in series. $R_1=10\ k$, $C_1=0.1\mu F$, $C_2=0.01\mu F$.

15.2. Sources of Jitter and skew

a. A balanced clock distribution scheme is shown in Figure 0.2. For each source of variation, identify if it contributes to skew or jitter. Circle your answer in Table 0.1

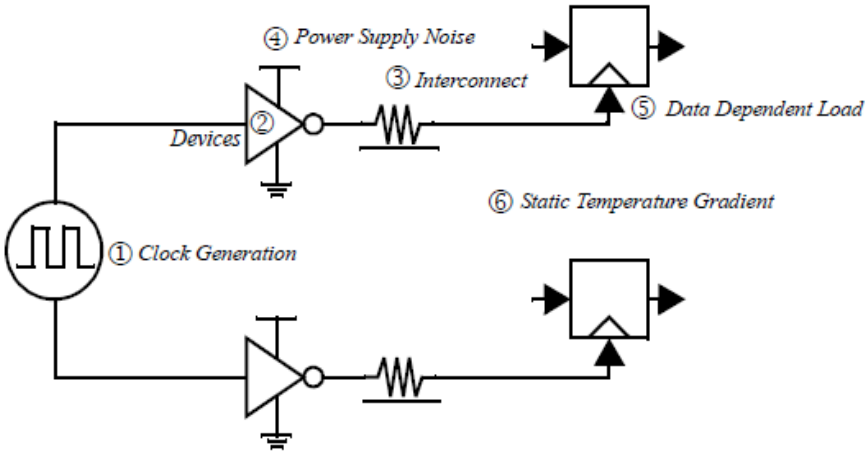


Figure 0.2 Sources of Skew and Jitter in Clock Distribution.

Figure 15.2.1: Copy - to be updated.

1) Uncertainty in the clock generation circuit	Skew	Jitter
2) Process variation in devices	Skew	Jitter
3) Interconnect variation	Skew	Jitter
4) Power Supply Noise	Skew	Jitter
5) Data Dependent Load Capacitance	Skew	Jitter
6) Static Temperature Gradient	Skew	Jitter

Table 0.1 Sources os Skew and Jitter

Figure 15.3.1: Copy ::

15.3. En till, PLL beräkna delningsfaktorn

15.4. En till, PLL jitter

15.5. En till, klockdrivare

EXERCISE SECTION 16: COMPUTER-AIDED LESSONS

- If you start the ANTIK project on your lab computer and launch MATLAB (type mlabjava) and Cadence (type cad), you will find some prepared files for this session.

- In Cadence, look for the files in the `andaLesson` library. In MATLAB, look for the files/functions starting with `anda*`

16.1. Amplifier stages

See `exercise_3p6` in the database. Identify how the small-signal schematics is built up in the CAD tool. In this way, you can replace your transmitter with a corresponding small-signal equivalent circuit (click on the symbol and descend into it).

This is a practical way of keeping your schematics as they are, but quickly go to a small-signal equivalent schematic without having to consider the DC operating points.

a) Solve Exercise 3.6.

b) Solve Exercise 3.5, but in a more heuristical way.

16.2. Opamp application 1

See `exercise_5p9` in the database which examplifies Exercise 5.9. It shows an impedance converter. We want to simulate an inductor. Inductors are normally very bulky and if they can be replaced by active counterparts, they should. Not shown in the exercise is the load required on the "other side" of the circuit. Call it for example Z.

You should now find which configurations that could give you an inductance. Compare with the lab, where we introduced boolean variables for switching in regulator, ground plane, etc. This could be done here too, for example switch resistance or capacitance.

```
R5 = 1k * resCap5 + 1G * (1-resCap5)
C5 = 100p * resCap5
```

etc. Now, you can use the tool to explore the solutions. Given the suggested network:

a) how many solutions do you find that give you approximate inductive behavior?

b) Is there any common setting for all?

c) If you do not want to have two capacitors or more in "series" - how many solutions do you have then?

16.3. Opamp application 2

You have three signals, for example,

$$x_1(t)=\sin\omega_1 t\,,\quad x_2(t)=\sin\omega_2 t\,,\quad x_3(t)=\sin\omega_3 t \tag{40}$$

with three different frequencies:

$$\omega_1=1 \text{ krad/s},\quad \omega_2=10 \text{ krad/s},\quad \omega_3=100 \text{ krad/s} \tag{41}$$

Create a circuit that at DC produces the following signal:

$$y(t)=1\cdot x_1(t)+2\cdot x_2(t)+3\cdot x_3(t) \tag{42}$$

At 100 krad/s it should produce the following:

$$Y(j\omega_3)\approx 1\cdot X_1(j\omega_3)+2\cdot X_2(j\omega_3)+2.1\cdot X_3(j\omega_3) \tag{43}$$

i.e., the higher frequency component is damped.

a) Dimension the RC components, and use ideal opamp(s).

16.4. Compensation of opamps

In exercise 5.7 you are asked to understand the properties of the compensation network in a two-stage amplifier.

One question, as a designer, is how to find the best capacitance and resistance of the compensation network. Most of the design variables are parameterized in the testbench and you can take a look at the compensation table at:

`ANTIK_0NNN_LN_opampCompensationTable_A.pdf`

in the download area:

`http://www.es.isy.liu.se/courses/ATIK/download/opampRef/`

for more guidance on compensation.

So, what configurations give you a phase margin more than 45 degrees? Only change the R and C values of the compensation network.

16.5. Filters

In exercise 7.7 you find a Sallen-Key filter. The exercise is "simple" since a bit of googling might help you. For example use

`http://sim.okawa-denshi.jp/en/OPseikiLowkeisan.htm`

to find some start values for your filter components.

a) Find the values on the discrete components that give you a bandwidth of 5 MHz.

b) Vary the gain of the opamp and see what happens with the filter response. Formulate some rule of thumb guidance on the opamp gain.

16.6. Non-ideal decoupling capacitors 1

Similar to what we did in the lab, we have in exercise 14.3 looked at a pair of decoupling capacitors in parallel and we are asked to find the resonance peaks.

Run the simulation with Cadence and observe the peaks for some different capacitances.

a) What happens when the capacitances are similar in size? Why?

b) What happens when one of the capacitances is small compared to the other? Why?

16.7. Non-ideal decoupling capacitors 2

Use MATLAB for symbolic manipulation of the expressions. See for example the function

`andaLessonSymbolic`

which enables you to define a symbolic expression. MATLAB then enables you to solve the equations with for example:

```
solve(Ztot,f)
```

By interpreting the expressions on `Ztot` you can also identify the values of `f` for which the `Ztot` will take infinite large values. Perhaps the obvious one is $f=0$.

a) What are the other values on f that gives you an infinite Z_{tot}, i.e., your resonance frequencies?

16.8. INL/DNL

Mätdata från ADC / DAC

Karaktärisera...