EXERCISE SECTION 14: DECOUPLING CAPACITORS AND POWER SYSTEMS

14.1. Board-level bypass capacitor

Assume a CMOS PCB having 100 gates each switching $10-pF$ loads in $5\ ns$. The power supply inductance is $100-nH$. Find the right value of bypass capacitor such that the power supply noise is kept below 0.1 volts.

14.2. Highest effective frequency of a bypass decap

From previous exercise, assume the $10-\mu F$ decap, has a series inductance of $L_{c2}=5\ nH$. We were working to achieve an X_{max} of $0.1\ \Omega$. Find the maximum frequency at which it is effective.

14.3. Non-ideal decaps

Calculate the resonance frequency of two non-ideal decaps in parallel, with parasitic inductance.