



Lecture 7, Timing, clocking

Differential signaling schemes
Timing and clocking

What did we do last time?

Filters

Choose second-order links and cascade them

Select filter components using software

Requirements on unity-gain frequency and slew rate

Supply filters

Decoupling capacitors (revisited today and in lab)

What will we do today?

Supply filters

Recapturing the decoupling capacitor

Signal distribution

Differential signalling

Signalling formats

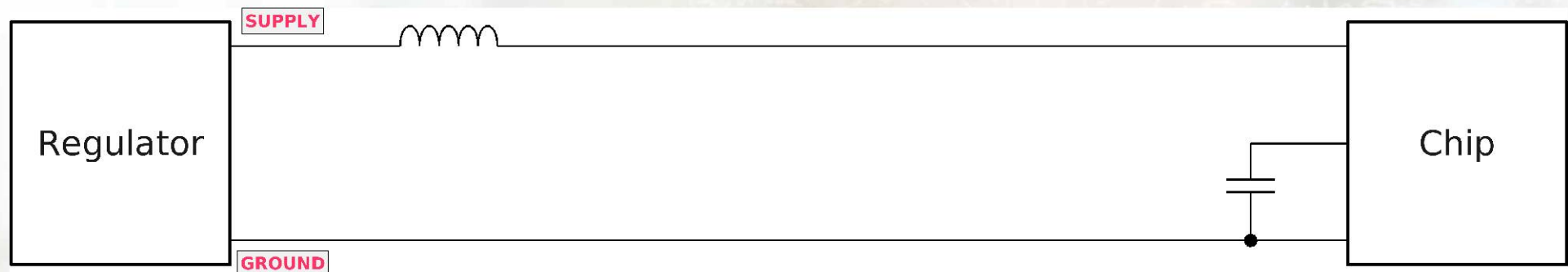
Timing and clocking

Skew and clock tree structures

A first glance at the PLL and clocking scenarios between chips

The power net impedance

Remember the situation with the inductance of supply wire

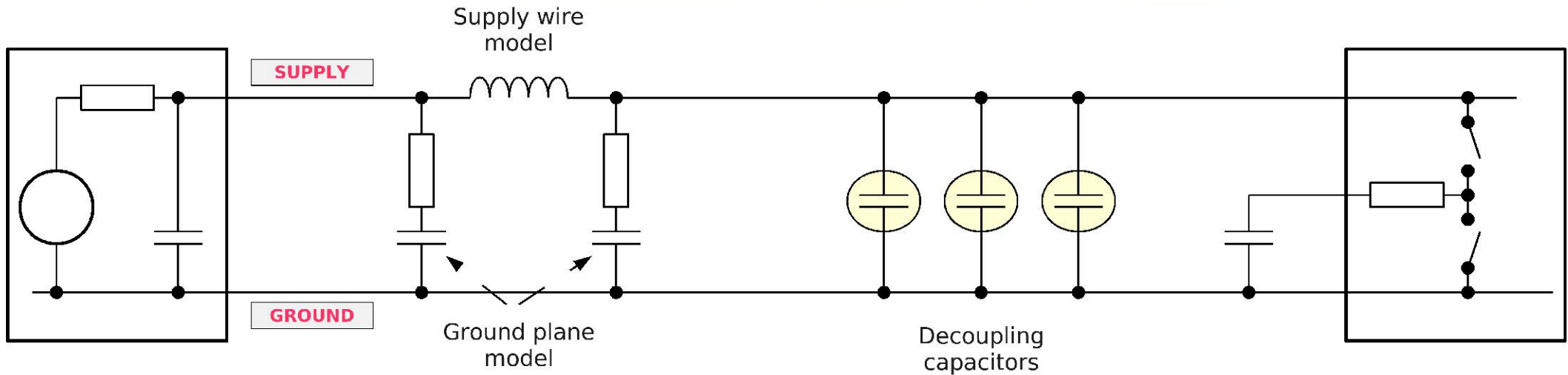


Current spike through inductor causes voltage drop

Current spike generated due to switching of capacitor in load

Voltage generated by regulator/battery/voltage source

The power net impedance, cont'd



Investigating the supply in the supply node (at the receiver chip)

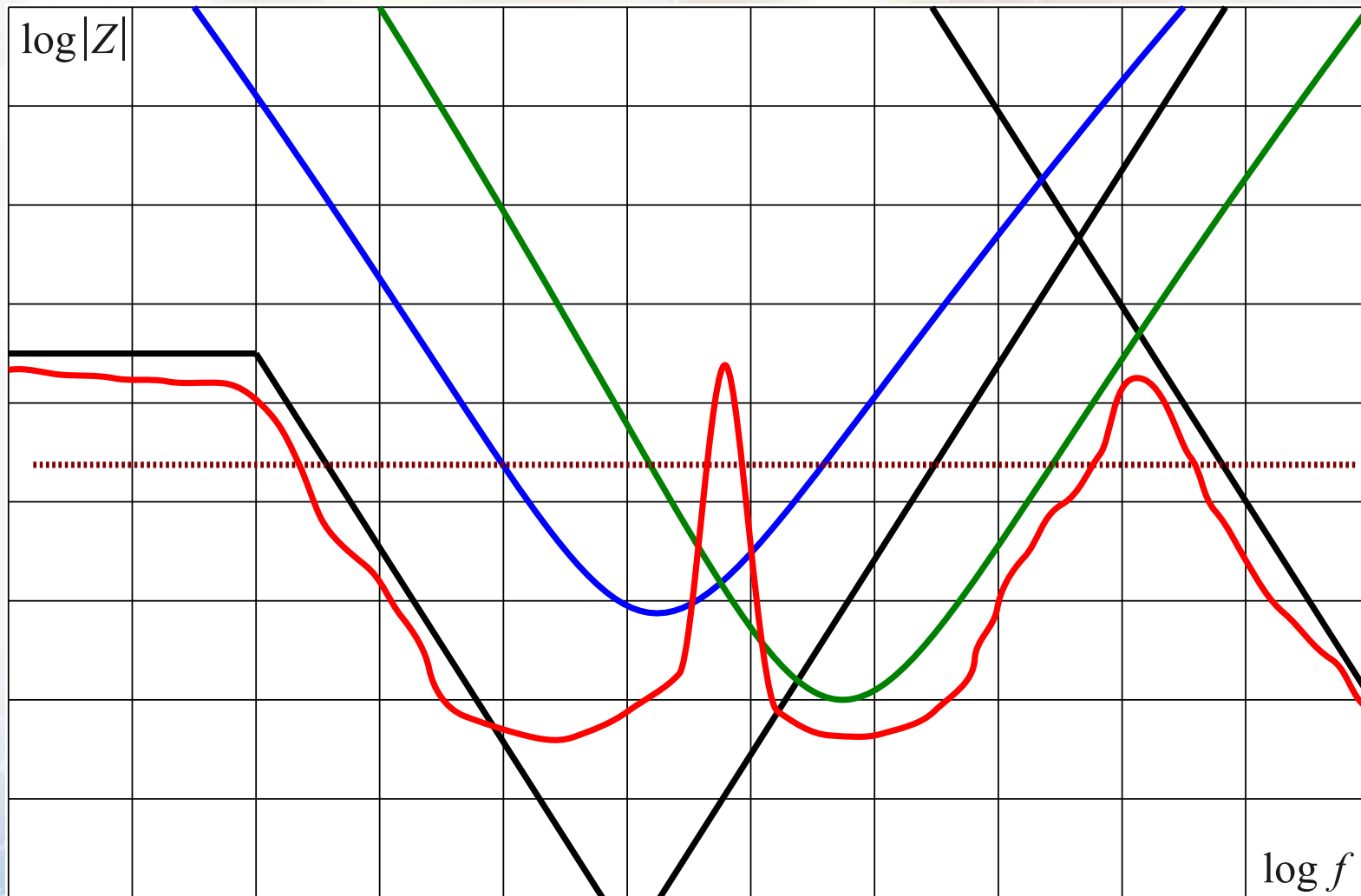
Regulator bandwidth

Ground plane (mainly capacitive)

Supply wire (mainly inductive)

Decoupling capacitors to further reduce impedance

The impedance diagram



Ground planes, towards differential signals

Minimizes the need for well-defined common reference

For example the ground

Improves the signal-to-noise ratio (by some 3 dB)

Single-ended signal power: $P_{s,s} = \frac{V_s^2}{2}$ and noise power: $P_{n,s} = V_n^2$

Differential signal power: $P_{s,d} = \frac{(V_s - (-V_s))^2}{2} = 2 \cdot V_s^2 = 4 \cdot P_{s,s}$ and noise

power $P_{n,d} = (V_{np} + V_{nn})^2 = V_{np}^2 + V_{nn}^2 = 2 \cdot P_{n,s}$

Differential signals

Differential signals

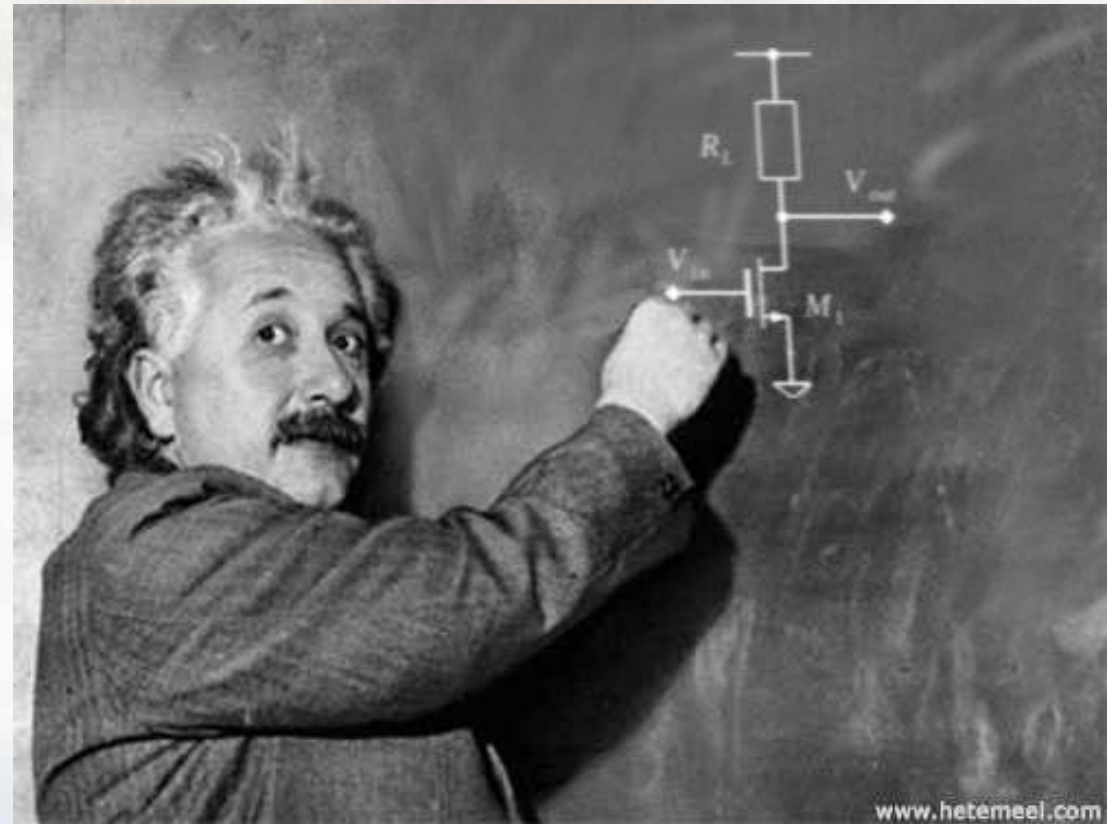
$$\Delta V = V_p - V_n$$

Common-mode signal

$$\nabla V = \frac{V_p + V_n}{2}$$

Common-mode suppression

The matrix



Differential signals, the matrix compiled

Compile the transfer functions into a handy matrix

$$\begin{bmatrix} \Delta V_{out} \\ \nabla V_{out} \end{bmatrix} = \begin{bmatrix} A_{df} & A_{df,cm} \\ A_{cm,df} & A_{cm} \end{bmatrix} \begin{bmatrix} \Delta V_{in} \\ \nabla V_{in} \end{bmatrix}$$

Common-mode rejection ratio

$$\text{CMRR} = \frac{A_{df}}{A_{cm}}$$

Design targets

Maximize the differential gain, Minimize the common-mode gain

Differential signals, two CS stages

Common-mode range (CMR)

Common-mode levels for which the transistors operate in saturation

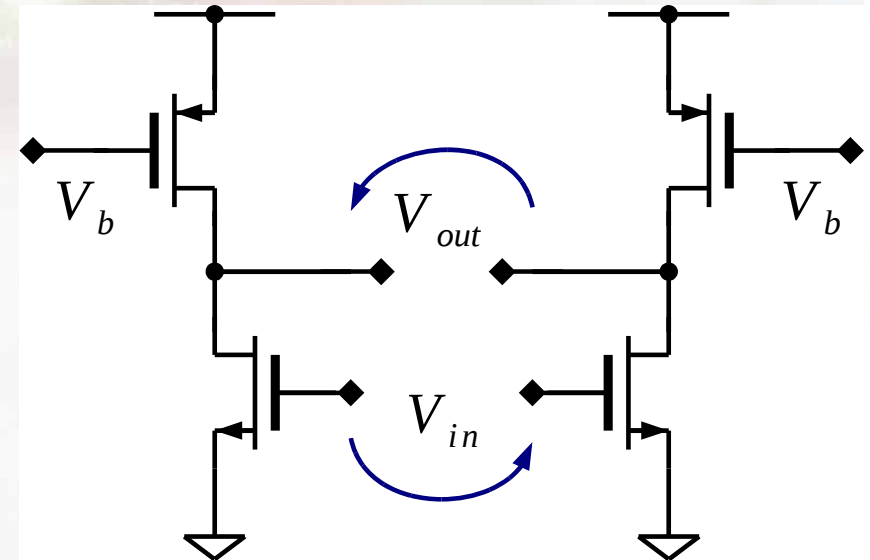
What about rejection?

If there is no rejection, the voltage headroom might be severely affected.

Without rejection, no real use (except for the slight gain in SNR)

Effectively there is no rejection in this configuration!

Some kind of "glue" is needed.



Differential signals, cont'd

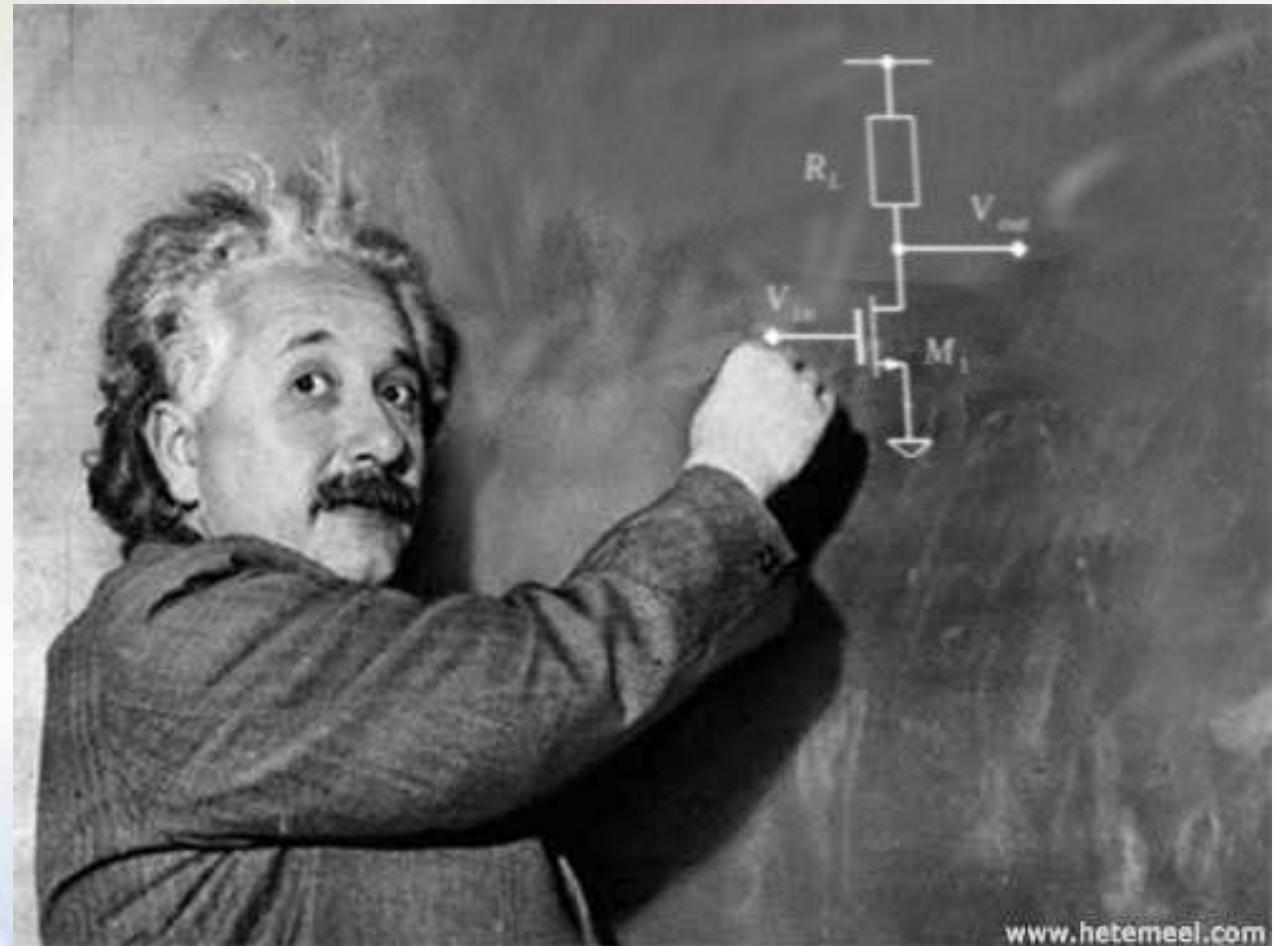
Two common-source stages in parallel

$$\text{CMRR} = \frac{A_{df}}{A_{cm}}$$

The differential pair

Tail source

$$\text{CMRR} = \infty$$



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Differential signals, differential pair

Improved (infinite) CMRR to cost of CMR

$$\Delta I = 4\alpha \cdot V_{eff} \cdot \Delta V \text{ and } \nabla I = I_0/2 \text{ (!)}$$

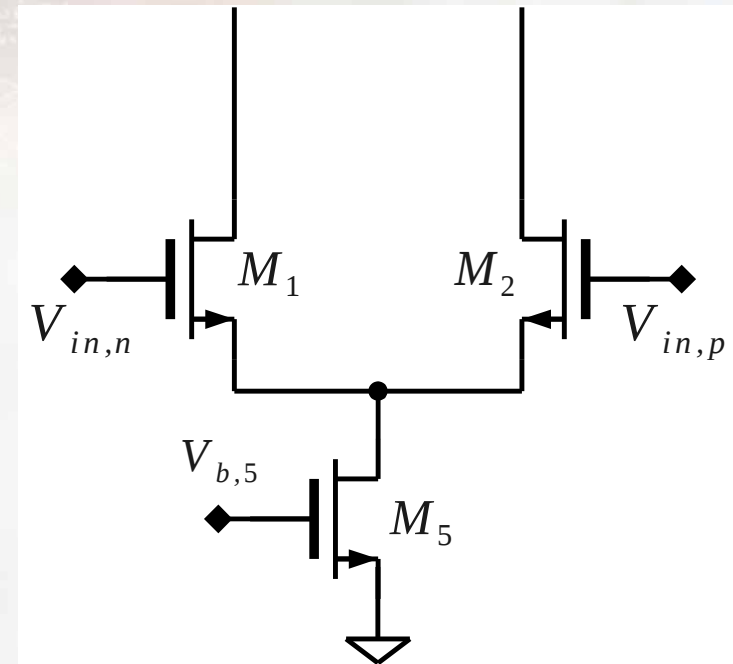
Further on

$$I_0 = 2\alpha \cdot (V_{eff}^2 + \Delta V^2)$$

combines into

$$\Delta I = 4\alpha \cdot \Delta V \cdot \sqrt{\frac{I_0}{2\alpha} - \Delta V^2} \text{ (!)}$$

$$\frac{d\Delta I}{d\Delta V} = 4\alpha \cdot \sqrt{\frac{I_0}{2\alpha}} = 4\alpha V_{eff} = \frac{2I_0}{V_{eff}} \text{ and } \frac{d\nabla I}{d\nabla V} = 0$$



Clock distribution, brute-force

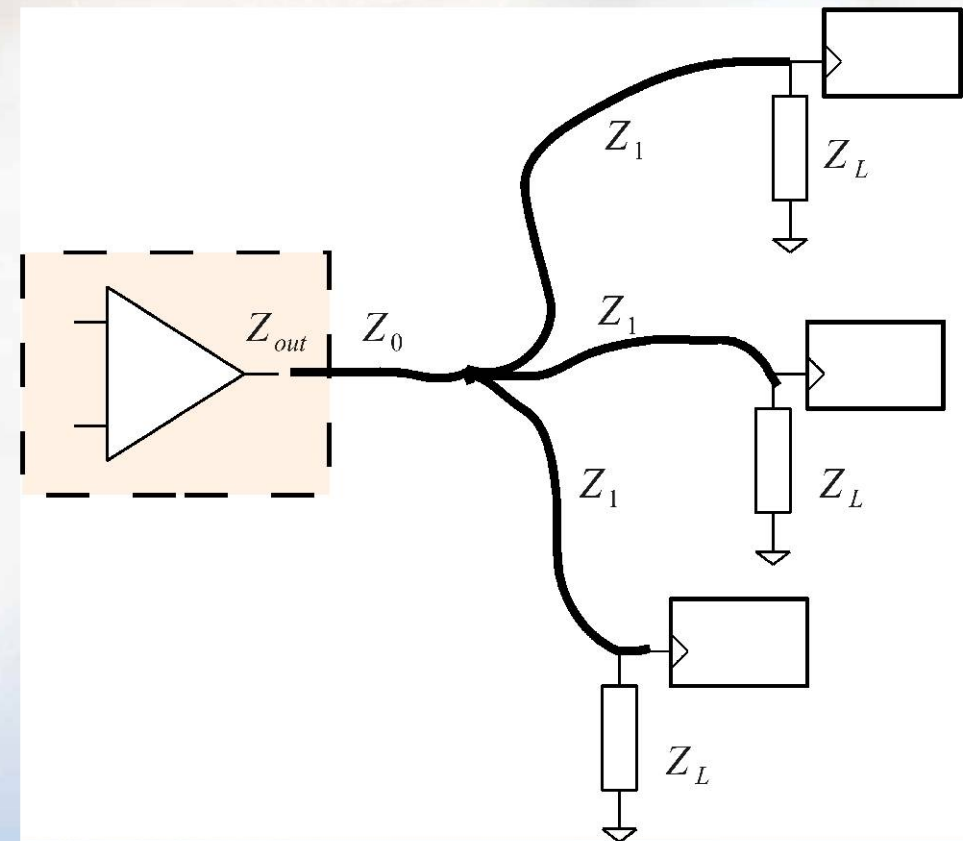
Assuming low-impedance driver ($Z_{out} \approx 0$)

Locate recipients close to each other

Wave absorbed by the termination at receiver

Drivers cannot drive too many loads

Put drivers in parallel



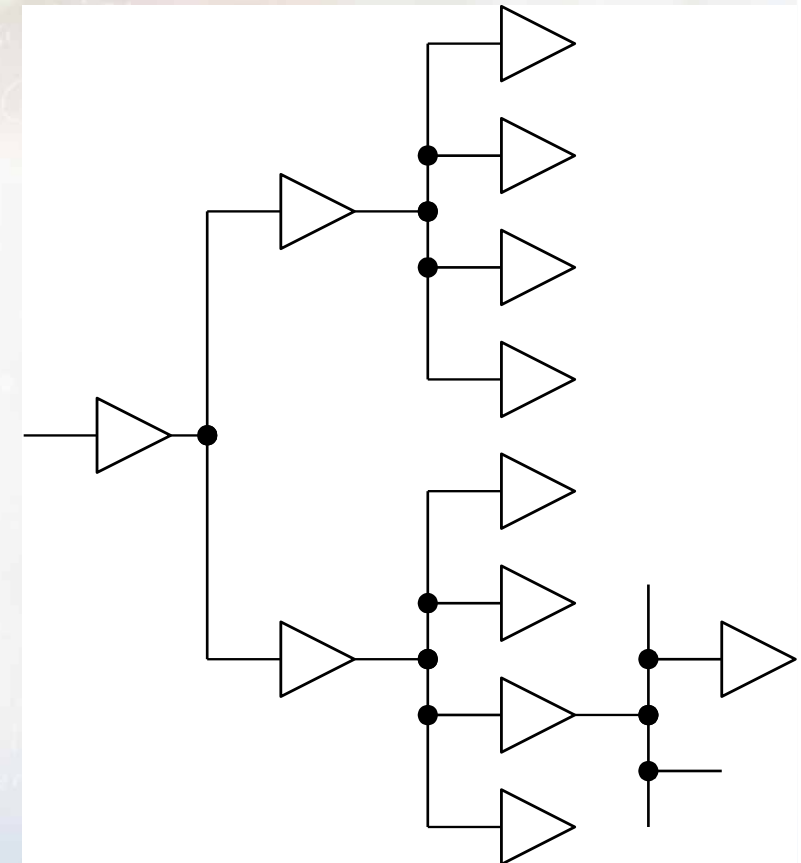
Clock distribution, clock tree

Assuming low-impedance driver ($Z_{out} \approx 0$)

Minimizes skew (if properly matched)

Intermediate points can be "brute-force"

Tapering factor is lower and less strict requirements on drivers



Clock distribution, lines

Assuming low-impedance driver ($Z_{out} \approx 0$)

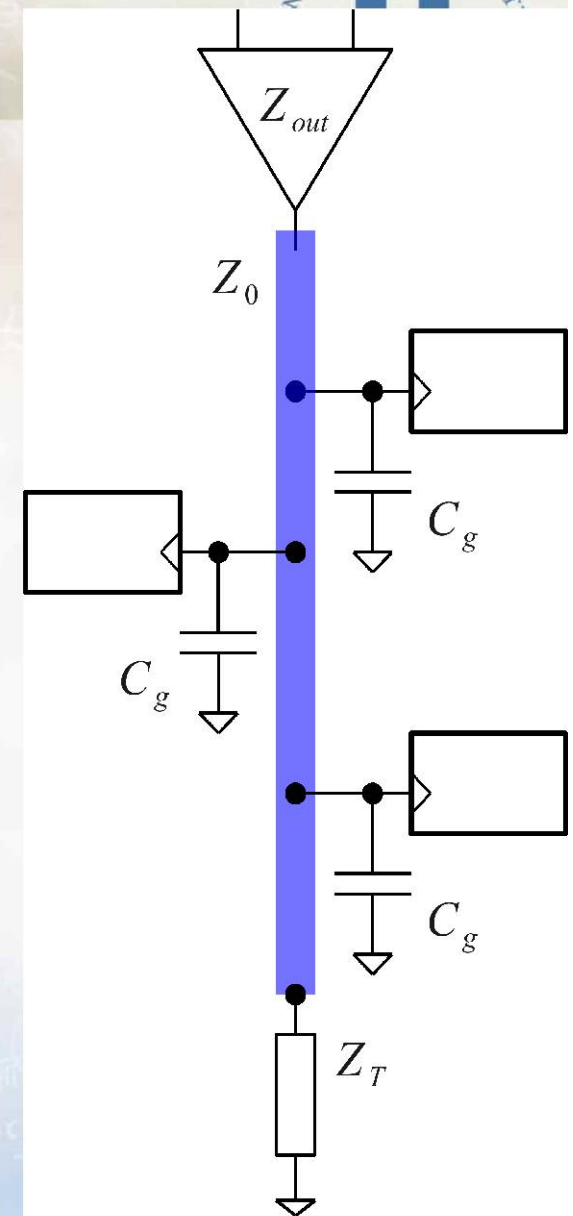
Reflected wave at each chip: $-C_g Z_0 / 2$ and given by the slope of the pulse, c.f., $i \sim C_g \cdot dV / dt$

This implies

Reduce the rise/fall times

Minimize the capacitance at each node

Reduce the Z_0, Z_T .



Clock distribution, source termination

Assuming "high"-impedance driver, ($Z_{out} > 0$)

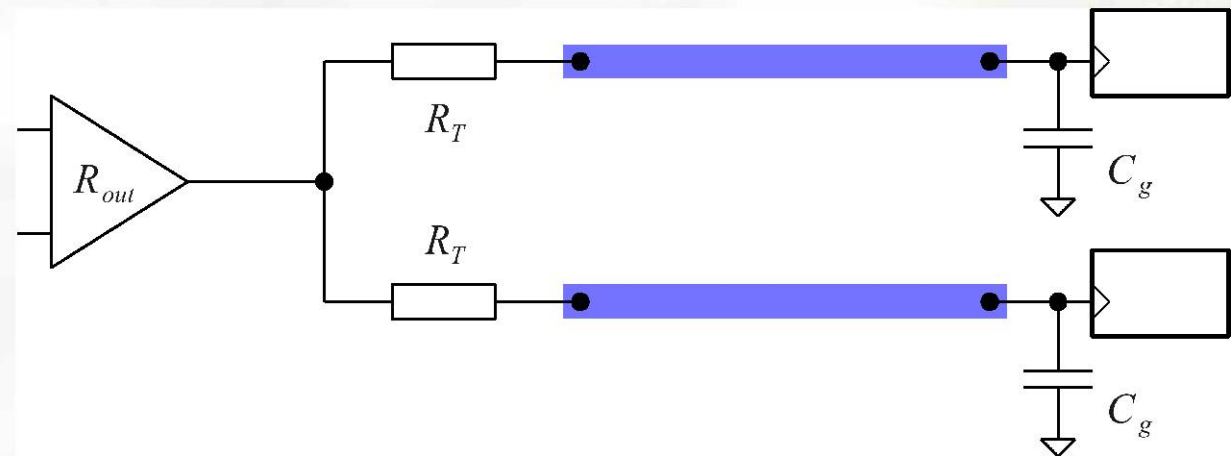
Driving N loads without far-end (resistive) termination.

Important (c.f. the lab)

Equal delay required

Equal load required

Choose $R_T = Z_0 - R_{out} \cdot N$



Maximum R_{out} cannot be too large!

Delay adjustments

Why?

Due to skew and matching (!) we need to guarantee equal length and equal delay

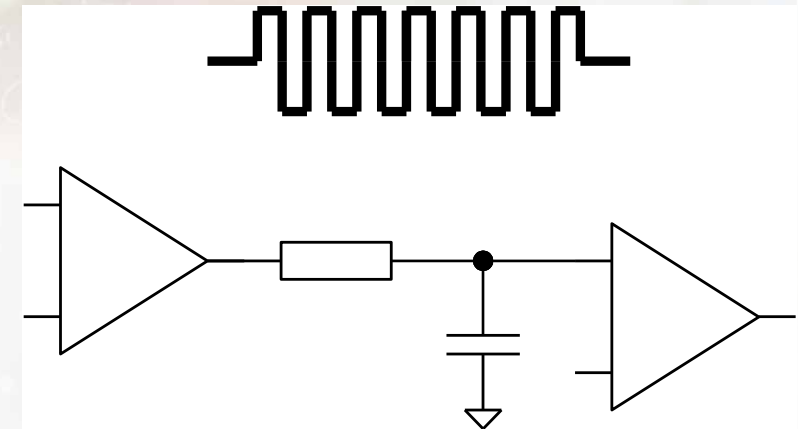
Examples of solutions

Increase length of wires

Introduce extra RC delay

Active tuning of delay

PLL/DLL



Oscillators

Voltage controlled oscillators (VCO)

Frequency controlled by an externally applied voltage.
Continuous-operation over a certain range.

Fixed-frequency oscillators (crystal)

The frequency is tuned to a fixed value (within tolerances).

Digitally controlled oscillators (NCO)

Frequency controlled by an externally applied control word. Output frequency is given by multiples of a fixed frequency (quantized).

Oscillators, stability

Different types of sources might influence the frequency

Temperature and voltage dependency

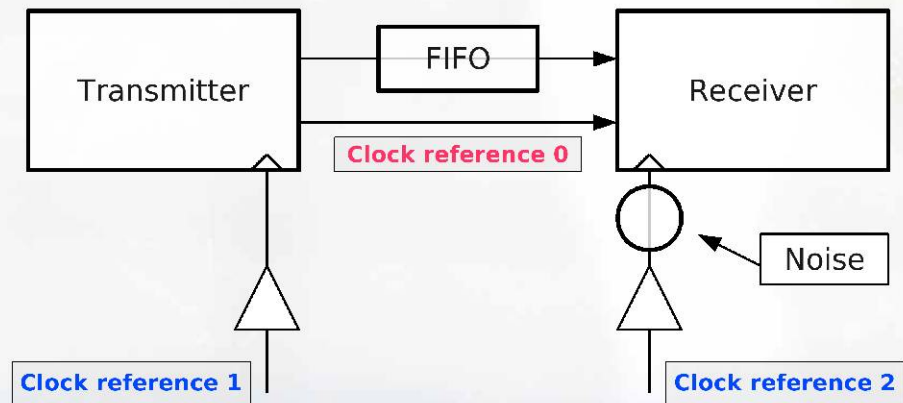
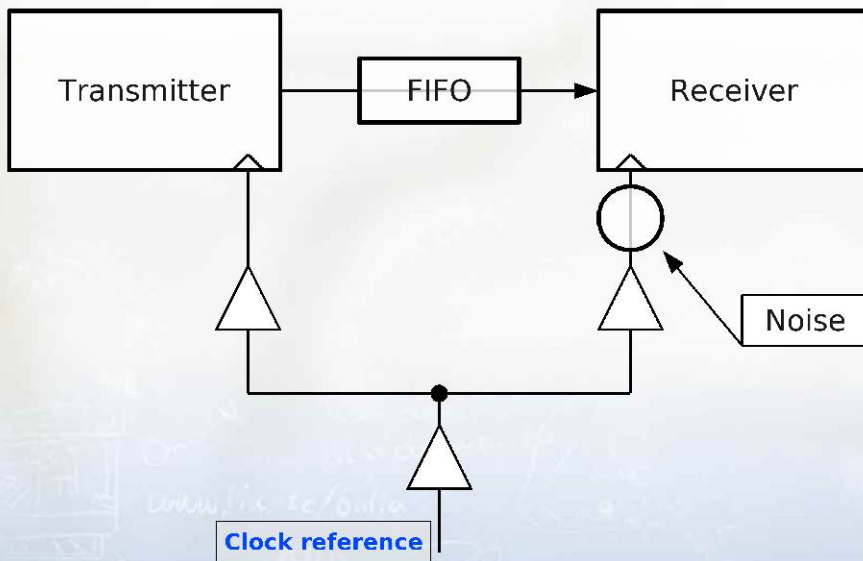
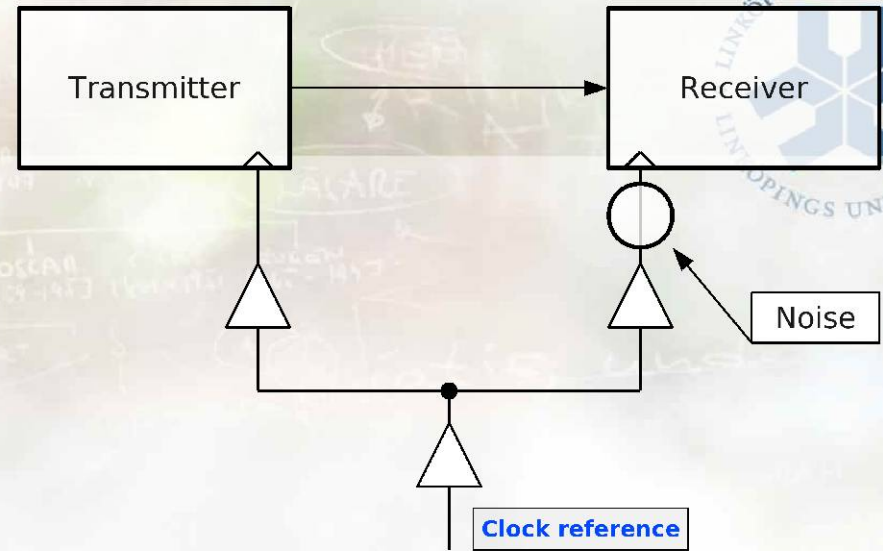
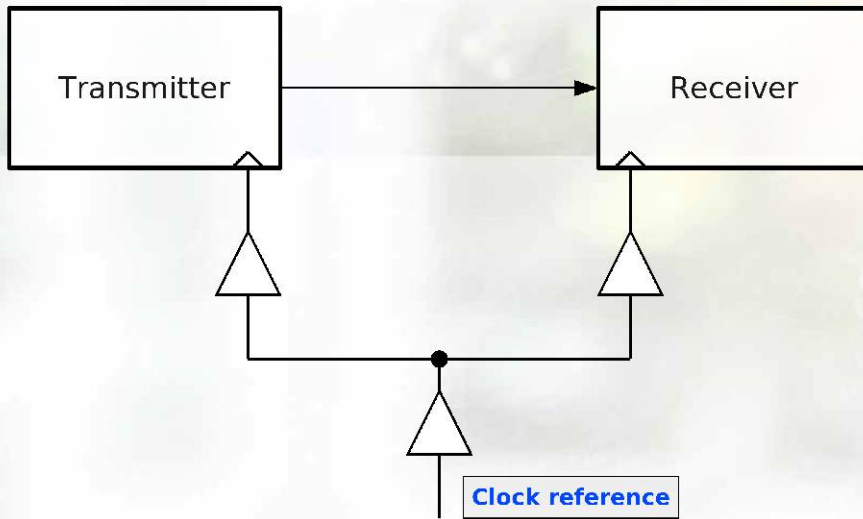
Supply noise and step functions on references

Results in (for example)

Jitter

Drift

A shift in nominal frequency



Signalling

A set of different signalling standards between chips

CMOS, TTL, ECL, CML, LVDS

Can be in different flavours

Swings, supply levels, current levels, etc.

Can have additional twists

Coding schemes

Some single-ended formats have differential modes.

CMOS (Complementary MOS)

Single-ended, CMOS

Voltage-driven

Maximum speed (on board) ~ 500 MHz

Toggles from supply to ground.

"Simple"

Power consumption is increasing with frequency and has a high impact on the chip IO ring (large switches and high di/dt)

Infinite input impedance

Low output impedance

TTL (Transistor-transistor logic)

Single-ended, bipolar

Current-driven. "Current-sink logic", i.e., current pulls down. No current implies that receiver pulls-up "by itself".

Maximum speed (on board) \sim 200 MHz

Toggles from supply to ground.

"Simple"

Power consumption high

Low input impedance

High output impedance (for high state). Low impedance for low state.

ECL (Emitter-coupled logic)

Single-ended, bipolar

Current-driven. "Current-sink logic", i.e., current pulls down. No current implies that receiver pulls-up "by itself".

Maximum speed (on board) ~ 1 GHz

Limited swing (negative levels and second termination rail).

"Simple/complex"

Power consumption high in quiescent operation

High input impedance

Low output impedance

CML (Current-mode logic)

Differential, bipolar, CMOS

Current-driven, AC coupled

Maximum speed (on board) ~ 10 GHz

Limited swing: 800 mV terminated to VDD.

Complex.

Power consumption is increasing with frequency and has a high impact on the chip IO ring (large switches and high di/dt)

→ Infinite input impedance

Low output impedance

LVDS (Low-voltage differential signalling)

Differential, CMOS

Current-driven. Max current of 3.5 mA.

Maximum speed (on board) 2.5 GHz

Limited swing: 350 mV around a center point ~ 1.25 V

Complex

Comparatively low power for the speed.

Infinite input impedance

100-Ohm output impedance ($100 \times 3.5 \text{ m} \sim 350 \text{ mV}$)

What did we do today?

Quick recapture on decoupling capacitors

Impedance of the supply net

Signal and clock distribution

Three different ways

Use differential signals!

Balance the paths

Oscillators

PLL next time.

What will we do next time?

Miscellaneous blocks

PLL and DLL

Regulators