Lecture 5, PCB vs Si

Basic components and structures of PCBs
Transmission lines

What did we do last time?

Noise

Thermal noise, an operational amplifier example

Flicker noise (1/f-noise)

Noise brickwall bandwidth: $\dfrac{p_1}{4}$

Distortion (pushed out to a lesson)

What sets the (non)linearity in our CMOS devices?

LiU EXPANDING REALITY

What will we do today?

PCB vs silicon

What are the differences when scaling up the geometries?

PCB specifics

A quick glance at different components (surface-mounted components)

Transmission lines

Termination techniques

LiU EXPANDING REALITY

Printed Circuit Board (PCB)

Layer stack

Up to some 30 layers and beyond (the more, the more expensive)

Number of layers reduces due to the higher silicon (SOC) integration, i.e., less need for interconnects. Nvidia uses some 10 layers or so.

Material

Aluminium, Copper, 10 um thick, 60 um wide (example values!)

Generically

Larger, cm-scale

Limited options for selecting sizes, driving capability, etc.

Silicon

Layer stack

Up to some 10,12 layers
Number of layers increases due to higher integration.

Material

Aluminium, Copper, 300 nm thick, 200 nm wide (example values!)

Generically

Smaller, 25x25 mm -> 3.000.000.000 transistors (!!!)
"Any" option for selecting sizes, driving capability, etc.

Transmission line effects become more and more important!

PCB vs. Silicon

Different nomenclature
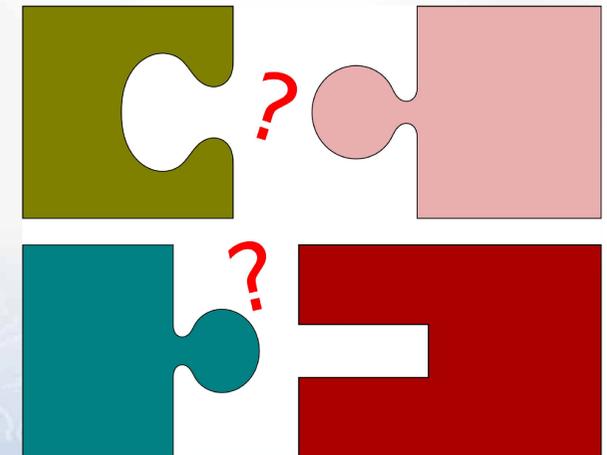
Different tools and designers

Different ways to verify, simulate, fabricate

Heat, mechanical stress, etc., for example

... but essentially doing the same thing

Due to IP development (soft and hard subcells
bought off-the-shelf) in CMOS design, the
assembly off the chip starts to resemble the
PCB design more and more.

More of an interconnect problem!

LiU EXPANDING REALITY

Surface-mount technology (SMx)

Old days

Hole through the entire PCB stack, effectively creating a large keep out in all layers.

Current trend

Smaller and smaller components (0.4 x 0.2 mm, "0402"). The smaller they get, the less power they tolerate, the smaller capacitors, inductors (< mH), etc.

A 0.4x0.2 resistor is rated for some 30 mW, **1 kOhm ~> 6 mA.**

Capacitor can be found in the **uF range.**

Implications of "size"

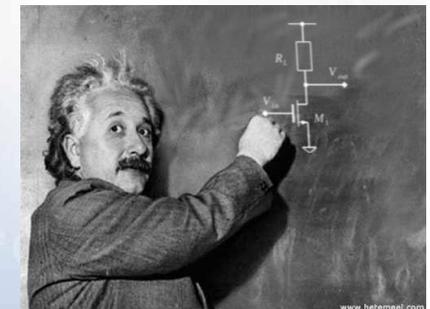Large size implies physical components, wires, etc. behave as distributed components and not lumped (one "point")

Distributed vs Lumped

t_r, t_f are the rise, fall times of a "digital" signal

t_d is the delay time through a wire, i.e., $t_d = \dfrac{l}{v} = \dfrac{l}{c/\sqrt{\epsilon_r}}$

Lumped elements: $t_r > 6 \cdot t_d$ **and** $t_f > 6 \cdot t_d$

Distributed elements: $t_r < 2.5 \cdot t_d$

LiU EXPANDING REALITY

Implications of "size", cont'd

Notice!

Rise/fall time! Not only the frequency of the signal as such!

What about sinusoids?

"Mathematically":
$$l < 0.1 \cdot \lambda = 0.1 \cdot \frac{v}{f} = 0.1 \cdot \frac{c / \sqrt{\epsilon_r}}{f}$$

Practically:
$$l < 0.01 \cdot \lambda = 0.01 \cdot \frac{v}{f} = 0.01 \cdot \frac{c / \sqrt{\epsilon_r}}{f}$$

At 2-GHz, the length must be > **1 cm/1 mm (!)** to be lumped!

More implications

Cross-talk

Wires will run a "long" distance next to each other and be sensitive to considerable mutual inductance.

Return paths

With every voltage (current) in one direction, there has to be a return current. That return path could be different compared to the wire. (The return current takes the past of least inductance).

Ringing and reflections

Due to the long wires, additional inductance, return paths, many more second-order effects are more visible

Implications of "size", cont'd

Voltage at different points along a distributed component
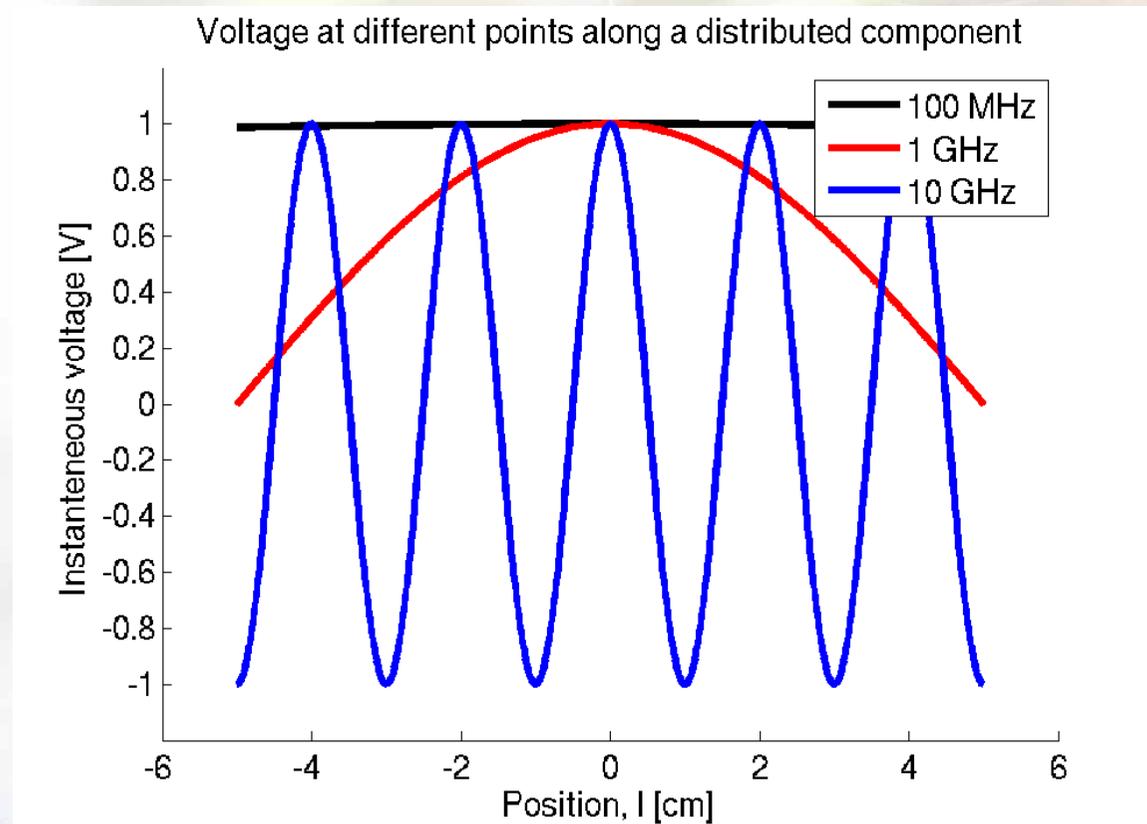
Cross-section must also be smaller than the wavelength (otherwise we get more prominent 3D-effects)

Transmission lines

Traveling wave

Consider the previous figure: the signal carrier (voltage, current, etc.) will travel as a wave over a surface.

This also holds for a pulsed waveform (i.e., not only the transient sinusoid). If we inject a pulse in one end, it will literally travel from one end to the other (and then?)
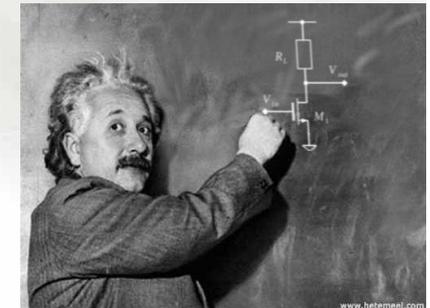
LiU EXPANDING REALITY
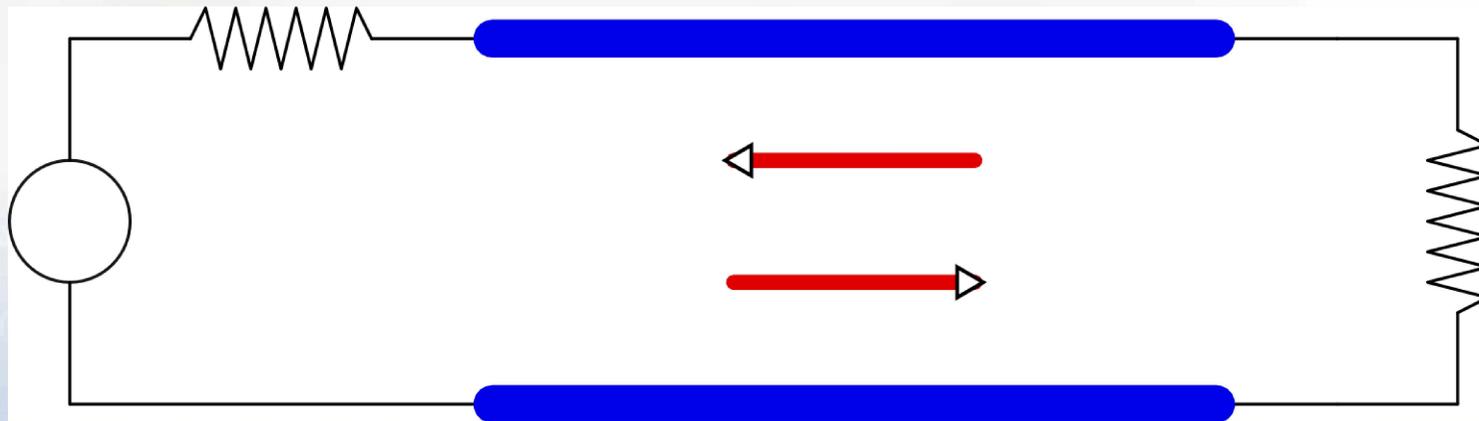
Transmission lines, cont'd

The Telegrapher's equations

Introduce direction and voltage/current at a given position:

$$\frac{d^2 V(x)}{d x^2} = -(R + j\omega L)\cdot\frac{d I(x)}{d x} \quad \text{and} \quad \frac{d I(x)}{d x} = -(G + j\omega C)\cdot V(x),$$

Solutions

$$\frac{d^2 V(x)}{d x^2} = \gamma^2 \cdot V(x), \quad \gamma^2 = (R + j\omega L)\cdot(G + j\omega C)$$

$$V(x) = V_{0p}\cdot e^{-\gamma x} + V_{0n}\cdot e^{\gamma x} \quad \text{and} \quad I(x) = I_{0p}\cdot e^{-\gamma x} + I_{0n}\cdot e^{\gamma x}$$
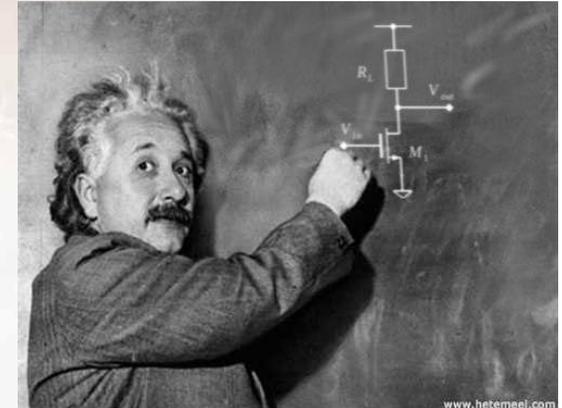
R is the sheet resistance, G is the dielectric loss,
L and C are the inductance and capacitance.

Transmission lines, cont'd

Boundary conditions

$V_{0p}, V_{0n}, I_{0p}, I_{0n}$ determined by (e.g.) boundaries:

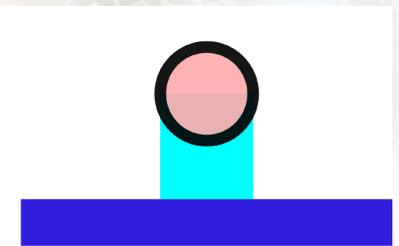$V(0) = V_{0p} + V_{0n}$ and $I(0) = I_{0p} + I_{0n}$.

The characteristic impedance

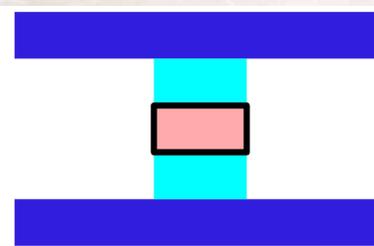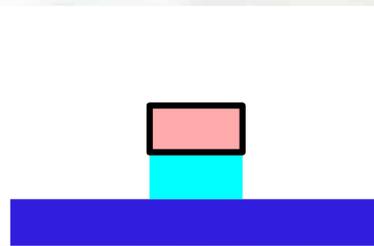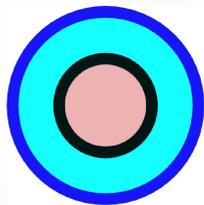$$Z_0 = \sqrt{\frac{R + j\omega L}{G + j\omega C}}$$ (independent on the wire length!)

$$Z_0 \approx \sqrt{\frac{L}{C}}$$ (lossless, often assumed for short wire/tracks)

C, L given by permeability between wire and shield, and inductance.

Examples of transmission lines

Examples

A transmission line is created in any environment.

The intersection of the wire(s) define the properties of the transmission line. (Still, the wire can be tapered, i.e., intersection changes with length).

The choice of width, dielectric, height, width, etc., enables the designer to adjust the characteristic impedance.

Effects of source and load impedance

Reflections

Due to the impedance levels, a wave will be dependent on the impedance it sees in every node.

Reflection coefficient

$$\Gamma(x) = \frac{Z(x) - Z_0}{Z(x) + Z_0}$$

At the boundaries

$$\Gamma(0) = \frac{Z_S - Z_0}{Z_S + Z_0}$$ (looking "left")

$$\Gamma(l) = \frac{Z_T - Z_0}{Z_T + Z_0}$$ (looking "right")

Effects of source and load impedance

Examples of "extreme" cases:

$Z_{T,S}=0$, short-circuit. $\Gamma=-1$. Full reflection with negative phase.

$Z_{T,S}=\infty$, open-circuit. $\Gamma=+1$. Full reflection with positive phase.

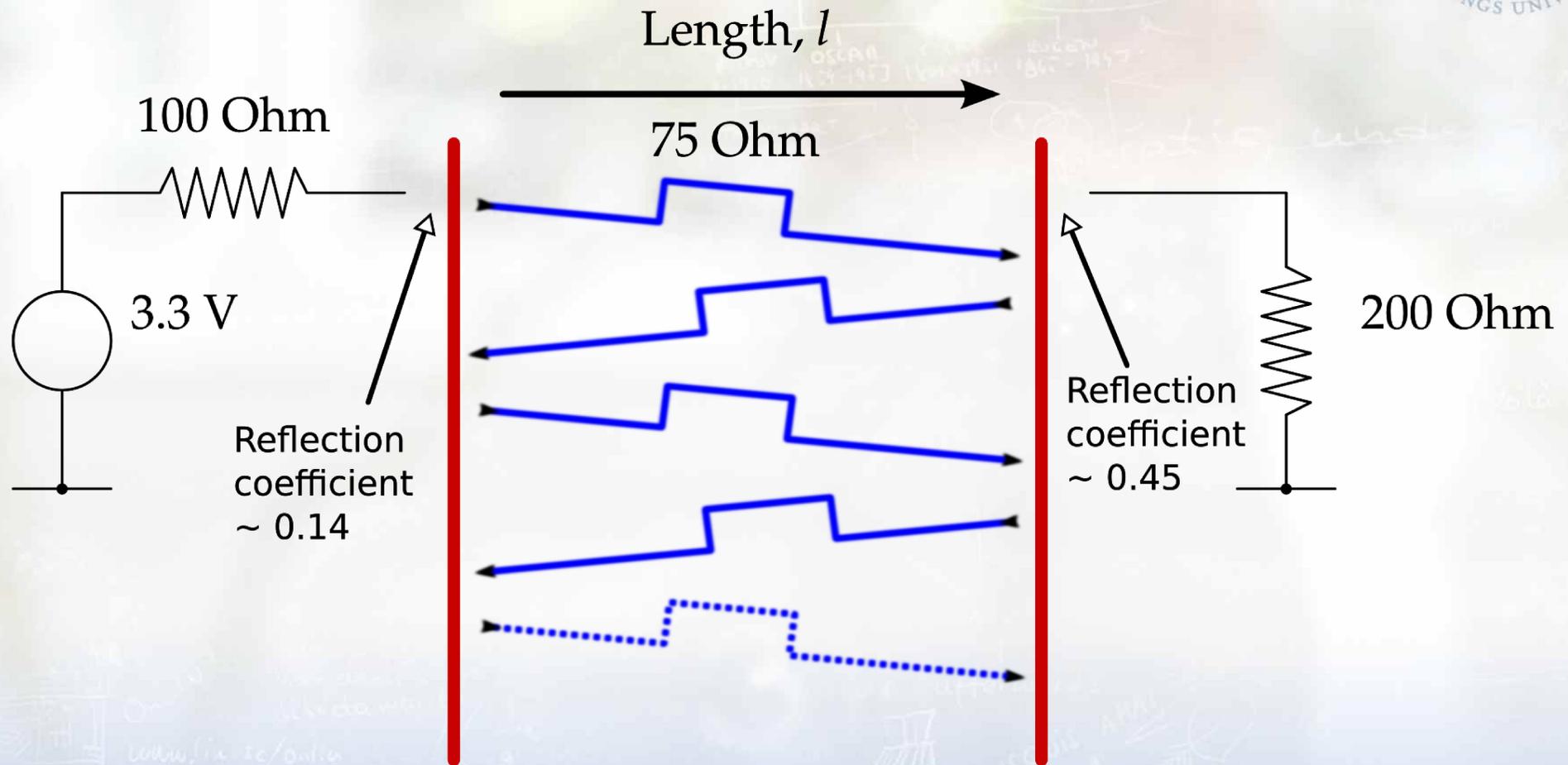$Z_{T,S}=Z_0$, "perfect" termination. $\Gamma=0$. Full absorption, no reflection.

Others

We can terminate with e.g. a capacitor too - a complex coefficient would give a phase shift.

Normally, the driver is assumed to have very low impedance.

Reflection diagram

Length, *l*

100 Ohm

75 Ohm

3.3 V

200 Ohm

Reflection
coefficient
~ 0.14

Reflection
coefficient
~ 0.45

Reflection diagram, cont'd

First outgoing wave amplitude is: $V_{out} = 3.3 \cdot \dfrac{75}{75+100} \approx 1.41$

This wave arrives at load and is also reflected.

First returning wave amplitude is: $0.45 \cdot 1.41 \approx 0.64$.

We get at the load: $V_l = 1.41 + 0.64 \approx 2.06$

Wave goes back to source and is reflected: $0.14 \cdot 0.64 \approx 0.21$.

Reflected at receiver: $0.45 \cdot 0.21 \approx 0.091$.

We get $V_l = 2.06 + (1 + 0.45) \cdot 0.091 \approx 2.19$

etc. until we end up at $V_l = 3.3 \cdot \dfrac{200}{200+100} = 2.2$

LiU EXPANDING REALITY

Splitted (bifurcated) wires

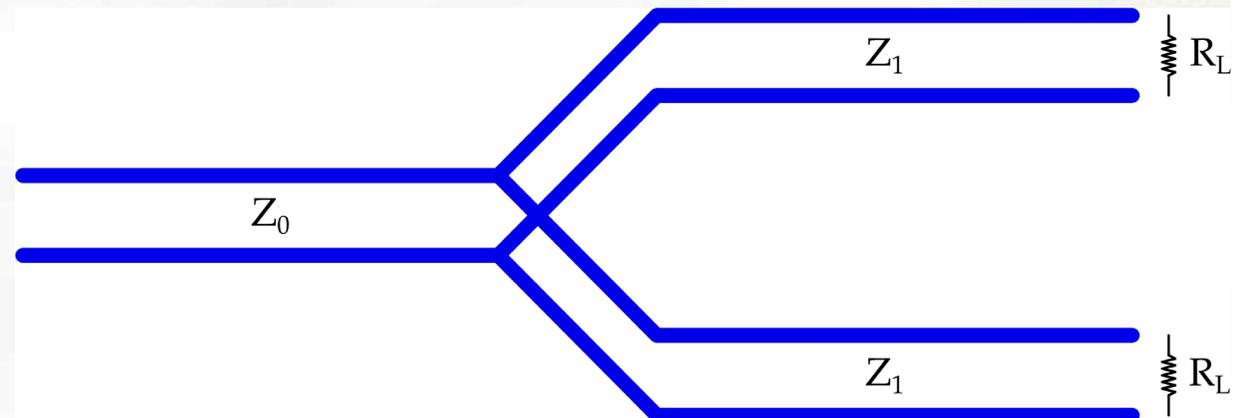**Special care needed at the interface between the wires**

$Z_0=Z_1$ yields reflections regardless of R_L

Taper the impedance!

$$Z_1=2Z_0$$

Use for termination

$$R_L=Z_1=2Z_0$$

Impedances must match at the fork!

Unterminated lines, some comments

Low source impedance

At the load, we will see an accumulation of the amplitude, effectively higher than the drive voltage (!).

Similar to ringing (undamped settling behavior).

High source impedance

Small incremental steps settling towards the end value.

Similar to a damped settling behavior (in some sense).

Source, series termination (back-matching)

Can be used together with open-circuit receivers

Serie resistor between driver output and transmission line

Cuts amplitude to 50% before "entering" transmission line

Full reflection at end, +1 due to the open circuit. This will effectively form a full swing at the receiver (!)

Reflected wave?

Absorbed at the source due to the source termination

Driver output current goes to zero when reflected wave arrives

Source termination, cont'd

Cascaded internal and series resistance must equal Z_0!

How close must source termination be?

Stub (inductive!, e.g. bonding wires + pcb strips) between driver and termination will produce reflection

Comparison end vs source termination

Source usually resistive (plus inductance), end usually capacitive

Mismatch between characteristic impedance and capacitive load generally worse than the series resistor mismatch

Usually less reflections in source termination

DC biasing of end termination

Termination resistor only to ground

Driver has to deliver a very high current when switching high.

Termination resistor between ground and supply

Select R_1 and R_2 such that $Z_0 = R_1 \| R_2$, i.e., $R_1 = \dfrac{R_2 Z_0}{R_2 - Z_0}$

Lower current for the driver, but both when switching low and high

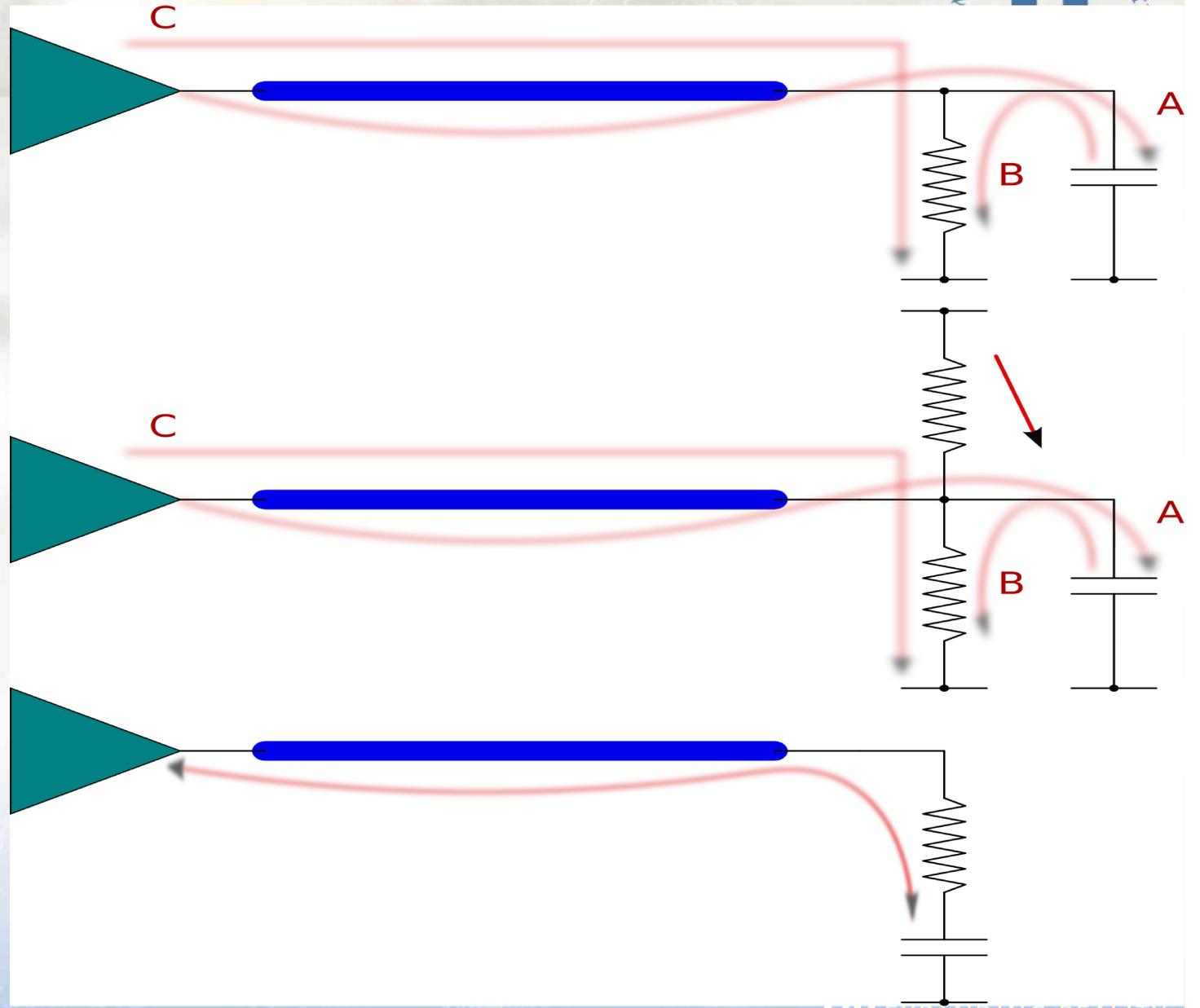A DC current $I_{avg} = \dfrac{V_{DD}}{R_1 + R_2}$ will be "wasted"

AC biasing of end termination

Use a capacitance in series with the termination resistance $(R=Z_0)$

Wastes less current compared to the DC biasing scheme (no current consumed at "DC")

But - must have a DC balanced signal, i.e., 50-% duty cycle, i.e., suitable for a clock driver.

DC/AC biasing of end termination

Short transmission lines

Very short strips

From e.g. chip to bypass capacitor must also be considered

Vias

A via will effectively form a short stub, and will have a characteristic impedance

Avoid vias on sensitive wires!

What did we do today?

PCB vs silicon

What are the differences when scaling up the geometries?

A quick glance at different components

Surface-mounted components

PCB

Some PCB specifics

Transmission lines

Termination and other properties

What will we do next time?

Filters

Supply filters

Data converters

LiU EXPANDING REALITY