Lecture 3, Opamps

Operational amplifiers, high-gain, high-speed

LiU EXPANDING REALITY

What did we do last time?

Multi-stage amplifiers

- Increases gain
- Increases number of poles

Frequency domain

- Stability
- Phase margin

What will we do today?

Wrap-up the discussion on compensation and stability

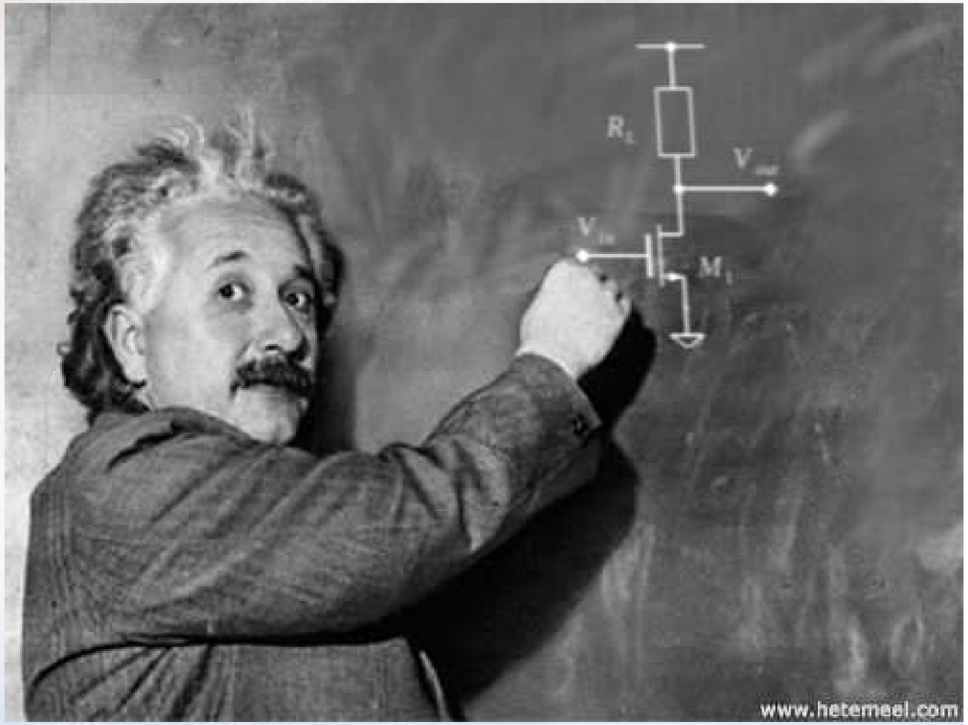
- Two-stage amplifiers
- Three compensation methods

Operational amplifiers

- Characteristics
- Operation

The problem: Stability, cont'd

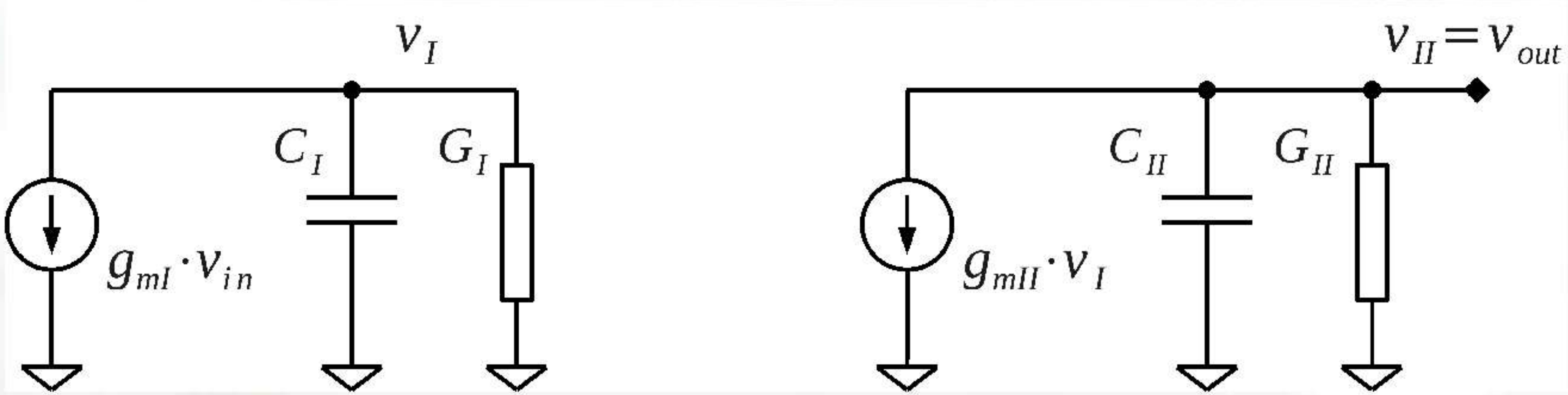
- **Bode plot**
  - What happens to the transfer characteristics?
  - Phase margin
  - Feedback factor
- **Step response**
  - Settling
  - Oscillations



Critically damped at 70 degrees

We need to be a bit more systematic

One model (high-impedance load) and focus on two-pole



$$p_1 = \frac{G_I}{C_I}, \quad p_2 = \frac{G_{II}}{C_{II}}, \quad A_1 = \frac{g_{mI}}{G_I}, \quad A_2 = \frac{g_{mII}}{G_{II}}$$

Dominant pole assumption (output)

Assuming pole splitting, $p_2 \gg p_1$, gives us

$$A(s) = \frac{A_1 \cdot A_2}{\left(1 + \frac{s}{p_{11}}\right) \cdot \left(1 + \frac{s}{p_{12}}\right)} \approx \frac{A_1 \cdot A_2}{1 + \frac{s}{p_1} + \frac{s^2}{p_1 \cdot p_2}}$$

This implies: $\omega_{ug} \approx A_1 \cdot A_2 \cdot p_1$ **and**

$$\phi_m = 180 - arg\, A(j\omega_{ug}) = 180 - atan\frac{\omega_{ug}}{p_1} - atan\frac{\omega_{ug}}{p_2} \approx 90 - atan\frac{\omega_{ug}}{p_2}$$

$$\phi_m \approx 90 - atan\left(A_0 \cdot \frac{p_1}{p_2}\right)$$

The formulas (dominant load!)

Unity-gain frequency

$$\omega_{ug} \approx \frac{g_{mI} \cdot g_{mII}}{G_I \cdot G_{II}} \cdot \frac{G_{II}}{C_{II}} = \frac{g_{mI} \cdot g_{mII}}{G_I \cdot C_{II}}$$

Phase margin

$$\phi_m \approx 90 - atan\frac{\omega_{ug}}{p_2} = 90 - atan\frac{\dfrac{g_{mI} \cdot g_{mII}}{G_I \cdot C_{II}}}{\dfrac{G_I}{C_I}} = 90 - atan\frac{g_{mI} \cdot g_{mII} \cdot C_I}{G_I^2 \cdot C_{II}}$$

etc., etc., etc. -- We need to be a bit more organized...

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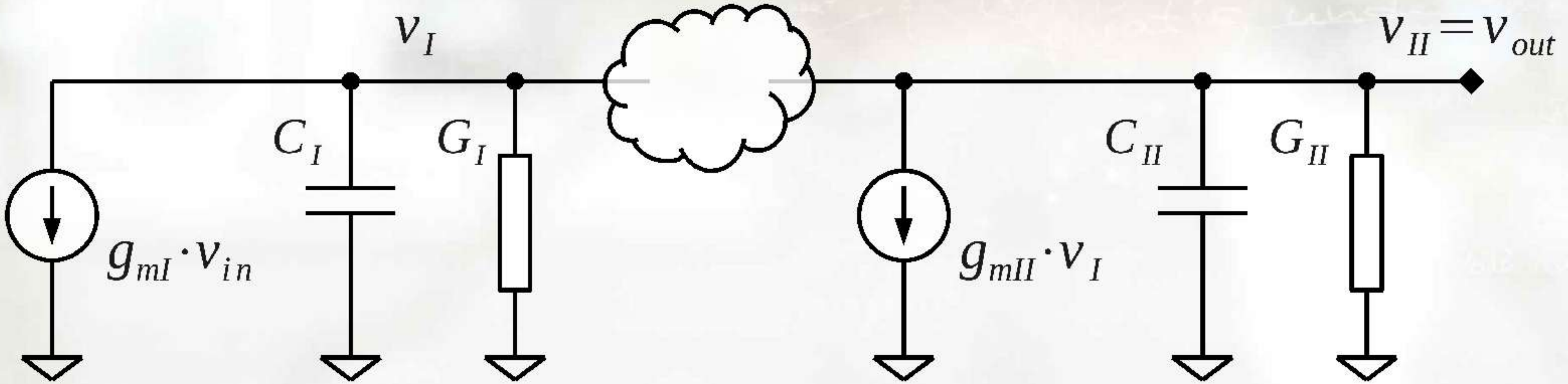
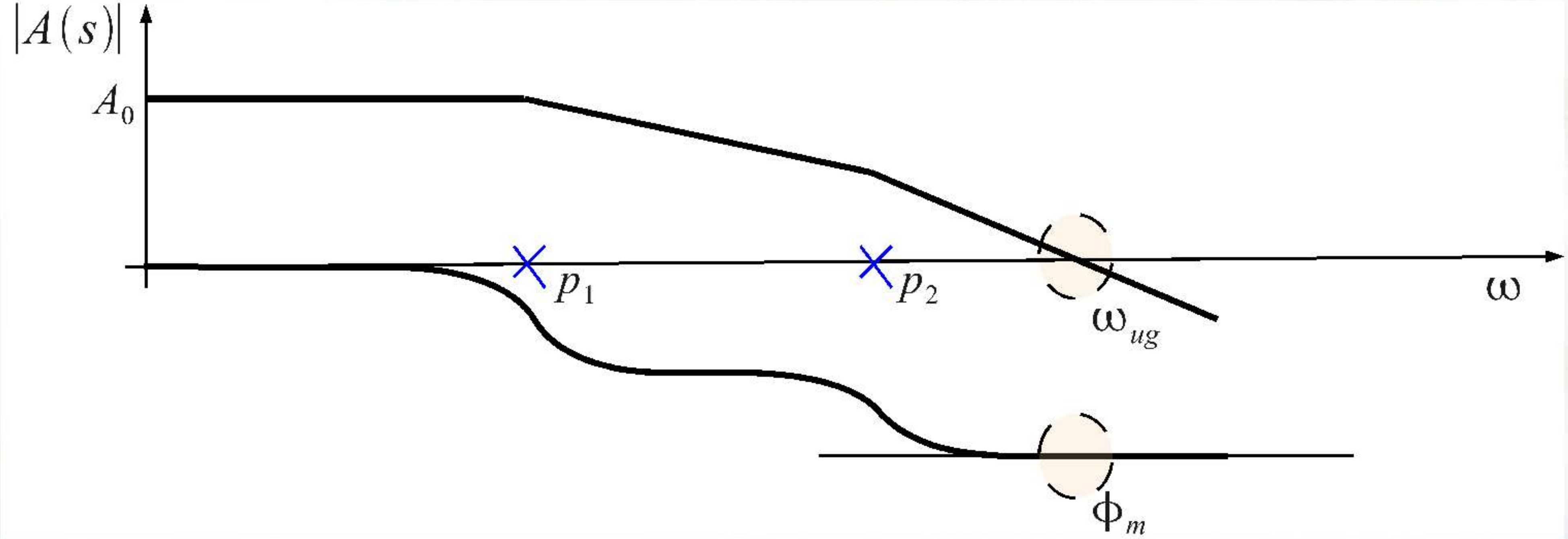
Compensation, poles are too close



The "cloud" could be a capacitor or series resistor-capacitor.

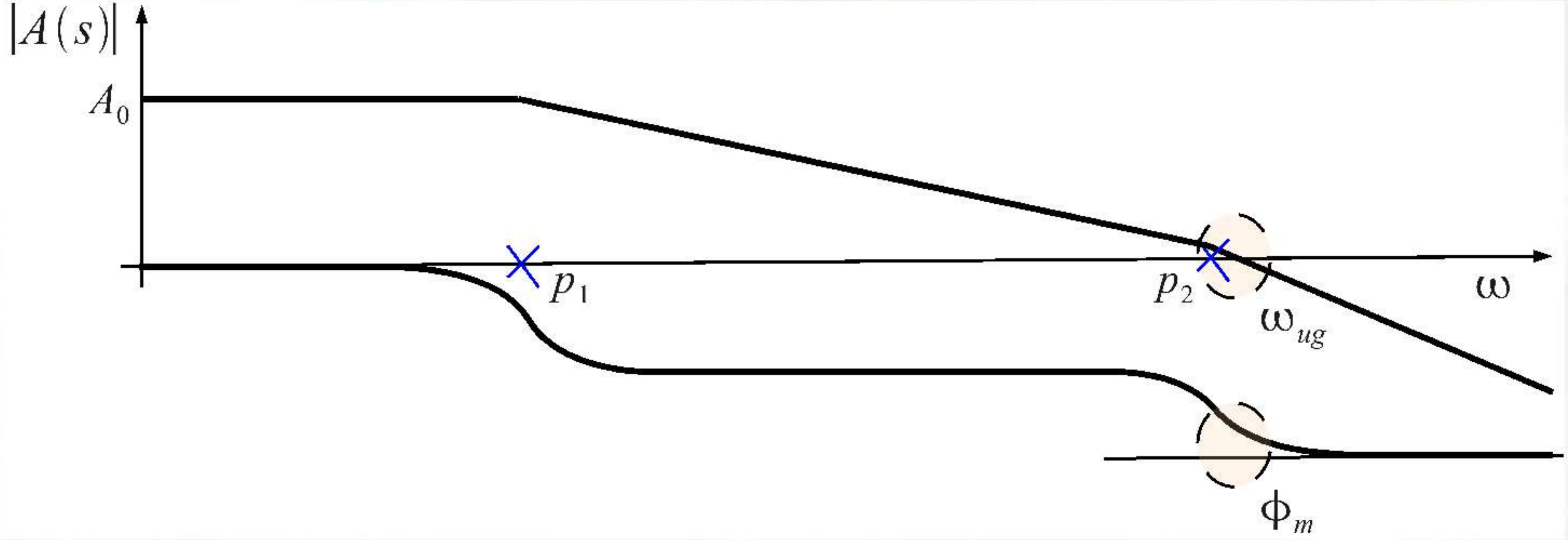
Poles and zeros 1

Stable?



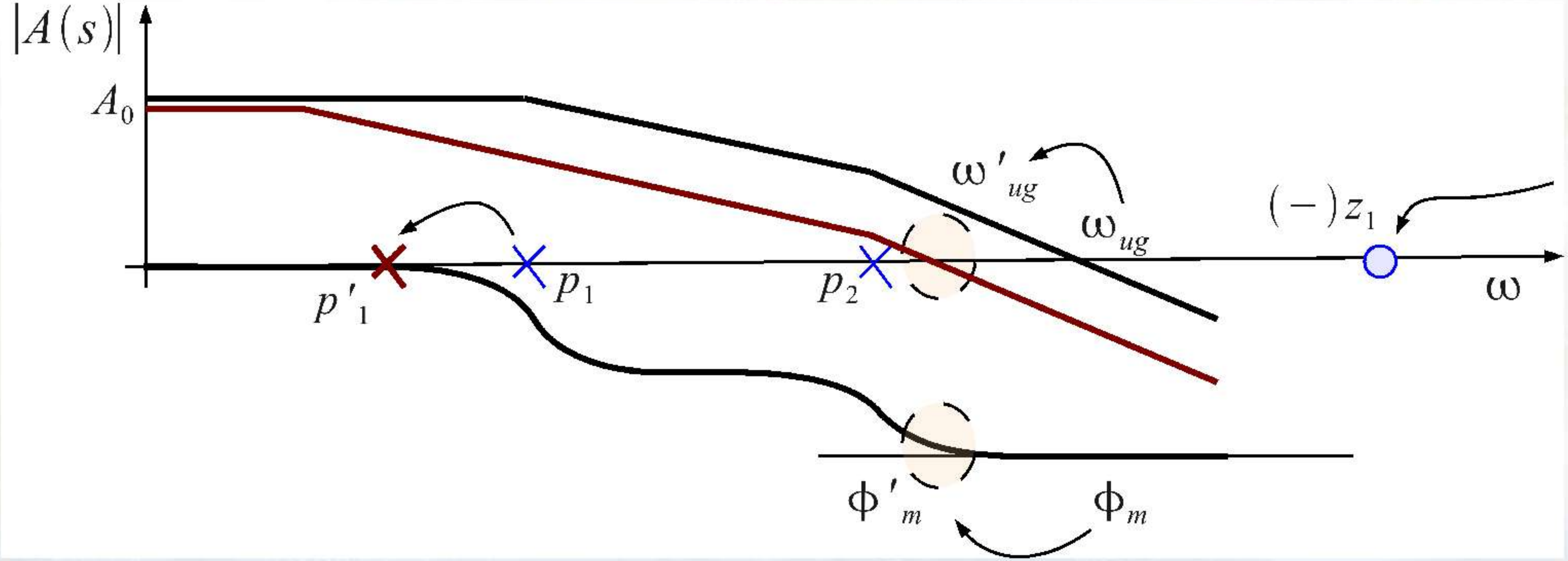
Poles and zeros 2

Stable?



Compensation

What is the cost associated with compensation?



Compensation, two cases:

1) "Internal" node sees a low-impedance node

Typically: output load dominates, drive a capacitive load

Load-compensation, i.e., increase cap externally

2) "Internal" node sees a high-impedance node

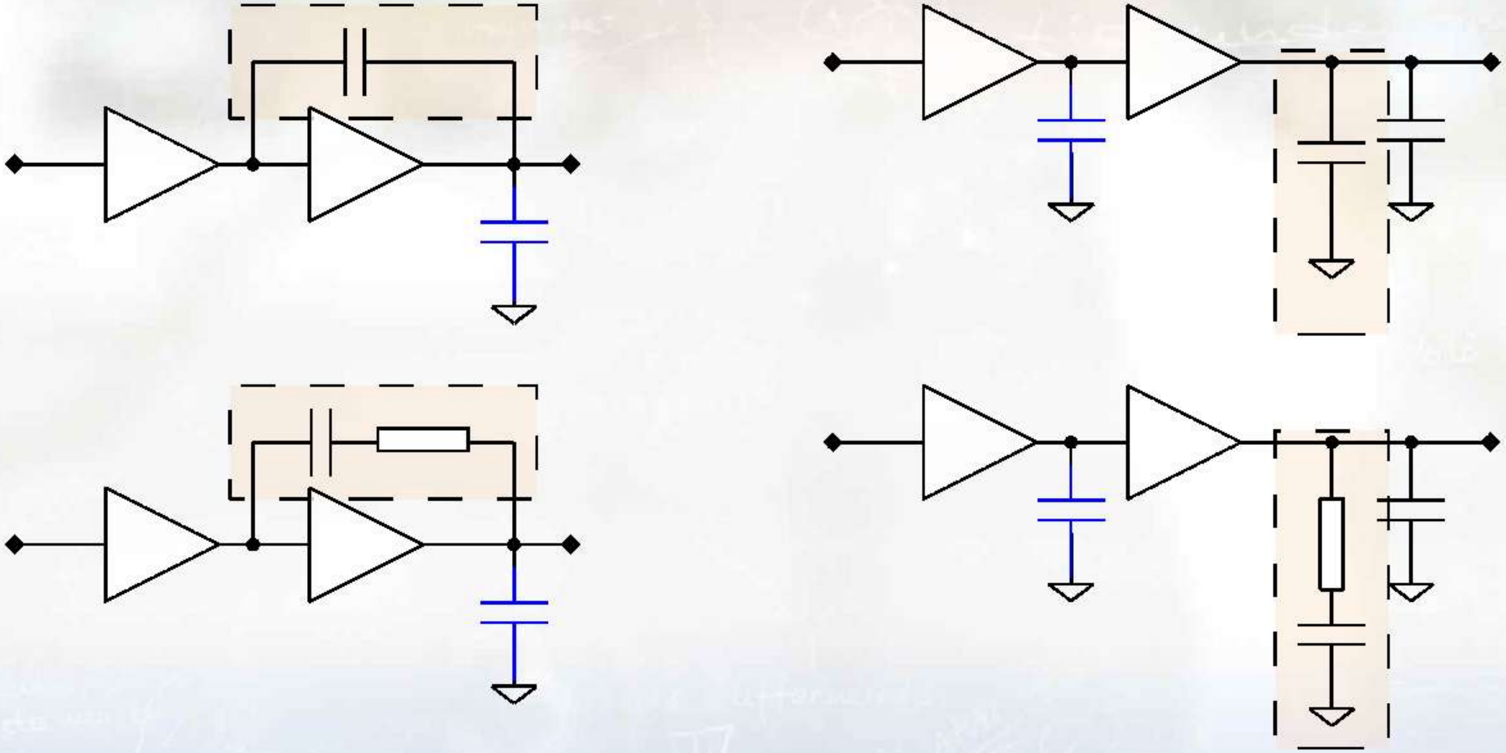
Typically: internal load dominates, drive a resistive load

Miller-compensation, i.e., utilize the second-stage gain to multiply C_C

As always, some exceptions to the rule:

Nested compensation, active compensation, ... and more ...

Compensation compiled:



Miller

Load compensation

Cap

Cap + Res

Compensation, Miller capacitance

Introduced zero	Parasitic pole	Dominant pole	Unity-gain
$z_1 = \frac{g_{mII}}{C_C}$	$p_2 = \frac{-g_{mII}}{C_{II}}$	$p_1 = \frac{-G_I \cdot G_{II}}{g_{mII} \cdot C_C}$	$\omega_{ug} = \frac{g_{mI}}{C_C}$

Introduced zero	Parasitic pole	Phase margin
$z_1 \approx 10 \cdot \omega_{ug}$	$p_2 \approx 2.2 \cdot \omega_{ug}$	≈ 60

Dominant pole moves "down", parasitic pole moves "up"

Parasitic zero added (harmful for phase margin)

Compensation, Nulling resistor 1

Introduced zero	Parasitic poles	Dominant pole	Unity-gain
$z_1 = \frac{g_{mII}}{C_C} \cdot \frac{1}{1 - R_Z \cdot g_{mII}}$	$p_2 = \frac{-g_{mII}}{C_{II}}$, $p_3 = \frac{-1}{R_Z \cdot C_{II}}$	$p_1 = \frac{-G_I \cdot G_{II}}{g_{mII} \cdot C_C}$	$\omega_{ug} = \frac{g_{mI}}{C_C}$

$$R_Z = \frac{1}{g_{mII}} \cdot \left(1 + \frac{C_{II}}{C_C} \right)$$

Introduced zero	Parasitic pole	Phase margin
$z_1 \rightarrow p_2$	$p_3 \approx 1.73 \cdot \omega_{ug}$	≈ 60

Compensation, Nulling resistor 2

Introduced zero	Parasitic poles	Dominant pole	Unity-gain
$z_1=\frac{g_{mII}}{C_C}\cdot\frac{1}{1-R_Z\cdot g_{mII}}$	$p_2=\frac{-g_{mII}}{C_{II}}$, $p_3=\frac{-1}{R_Z\cdot C_{II}}$	$p_1=\frac{-G_I\cdot G_{II}}{g_{mII}\cdot C_C}$	$\omega_{ug}=\frac{g_{mI}}{C_C}$

$$R_Z=\frac{1}{g_{mII}}$$

Introduced zero	Parasitic pole	Phase margin
$z_1\rightarrow\infty$	$p_2\approx 1.73\cdot\omega_{ug}$, $p_3>10\cdot\omega_{ug}$	≈ 60

Rule-of-thumbs for hand-calculation

Use e.g. MATLAB to support calculations for understanding

```
/site/edu/es/ANTIK/antikLab/m/antikPoleZero.m
```

```
/site/edu/es/ANTIK/antikLab/m/antikSettling.m
```

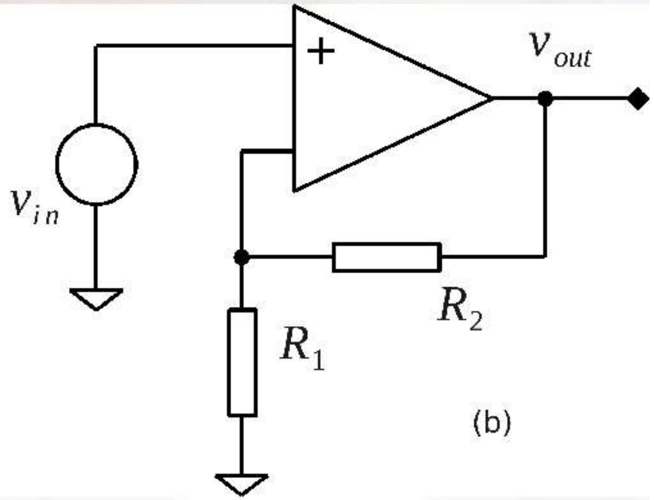
In the end, use the simulator.

- It has to be robust over temperature and other variations.
- Hand calculations are incorrect per definition

Model corresponds quite well with circuit once you have identified the different stages

- See for example exercises

Operational amplifiers



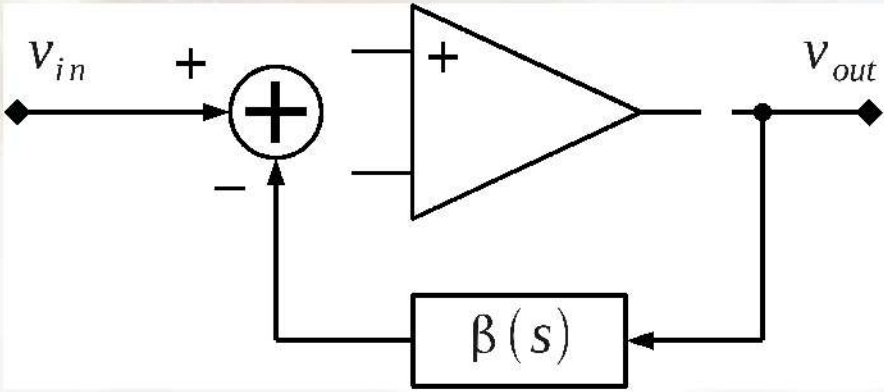
Operational amplifiers (OP)

- drive resistive loads
- have zero output impedance, zero input impedance, infinite gain
- act like a voltage source

Operational transconductance amplifiers (OTA)

- drive capacitive loads
- have infinite output impedance, zero input impedance, infinite gain
- act like a current source

Why do you want controlled feedback?



Gain is now under control!

No variation with gm/gds, instead it is given by passive components

"Unlimited" drive capability

Isolation of input and output

Linearization

Remember, it is a regulation loop. It is designed to track the changes, anything added in the loop will be supressed.

Practical concerns

Limited gain

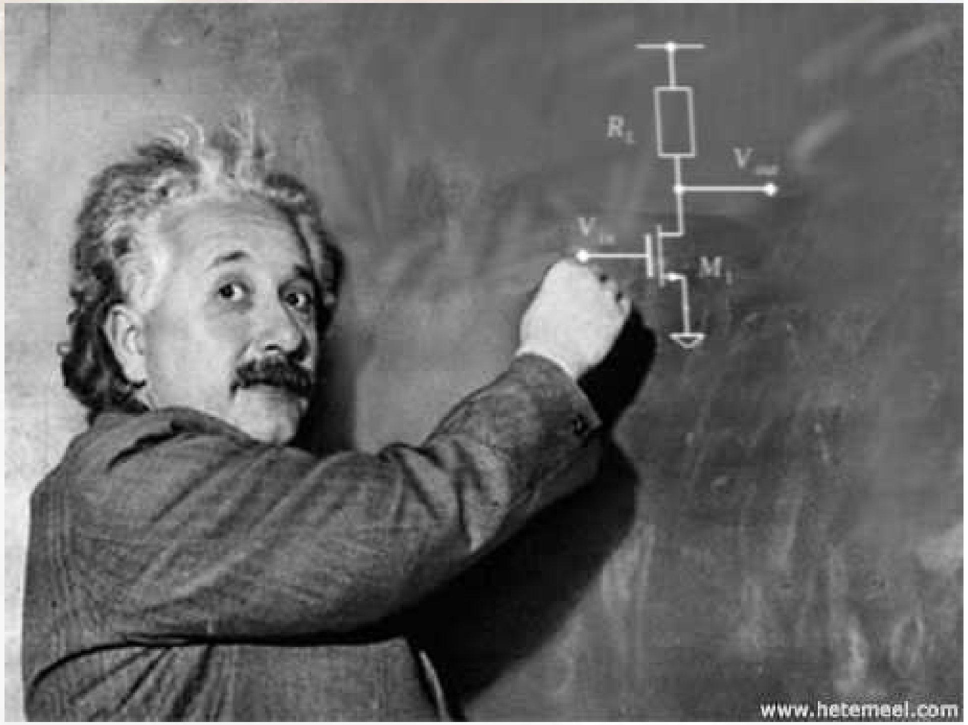
- Open-loop gain vs. closed-loop gain

Bandwidth

- Speed

Offset error

- Mismatch will cause an offset - how do we handle this?



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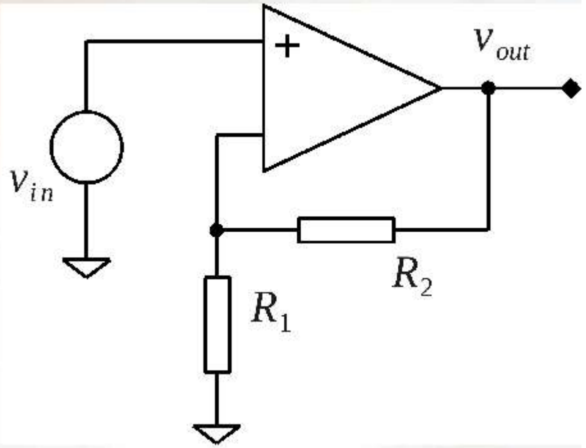
Limited gain



Ideal case:

$$\frac{R_1}{R_1+R_2}\cdot v_{out}=v_{in}\Rightarrow\frac{v_{out}}{v_{in}}=\frac{R_1+R_2}{R_1}=\Gamma$$

Non-ideal gain case:

$$v_{out}=A_0\cdot\left[v_{in}-\frac{R_1}{R_1+R_2}\cdot v_{out}\right]\Rightarrow\frac{v_{out}}{v_{in}}=\frac{1}{\frac{1}{A_0}+\frac{R_1}{R_1+R_2}}=$$

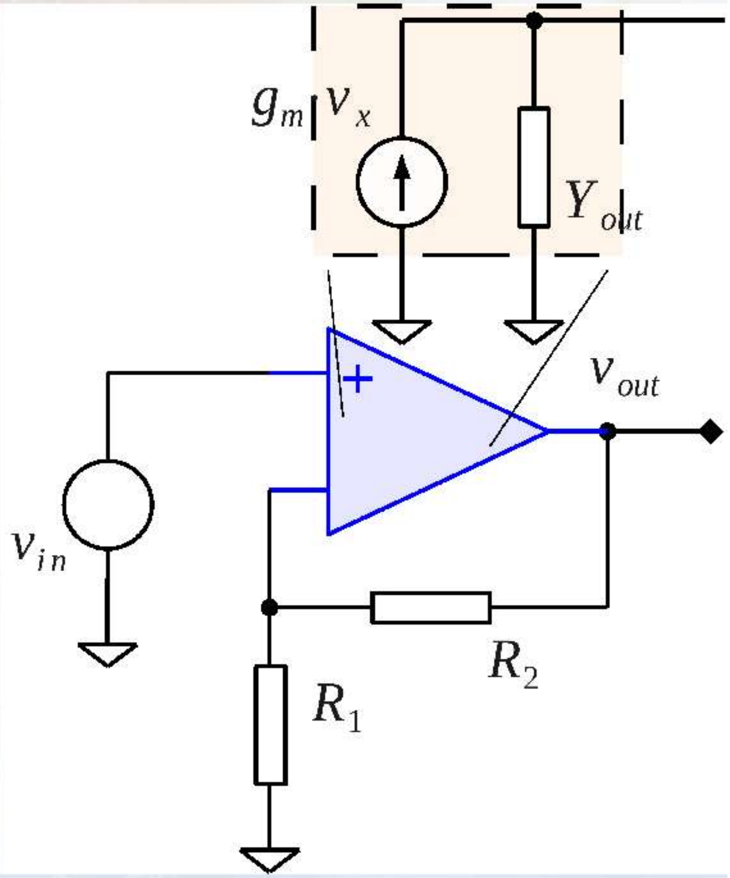
$$=\frac{R_1+R_2}{R_1}\cdot\frac{1}{1+\frac{R_1+R_2}{A_0\cdot R_1}}=\frac{\Gamma}{1+\frac{\Gamma}{A_0}}$$

Bandwidth

Single-pole (ignore effect of impedance):

$$\frac{v_{out}}{v_{in}} = \frac{\Gamma}{1 + \frac{\Gamma}{A_0} \cdot \left(1 + \frac{s}{p_1}\right)}$$

$$\frac{v_{out}}{v_{in}} = \frac{\frac{\Gamma}{1 + \Gamma / A_0}}{1 + \frac{\Gamma / A_0}{1 + \Gamma / A_0} \cdot \frac{s}{p_1}} \approx \frac{\Gamma}{1 + \frac{s}{p_1 \cdot A_0 / \Gamma}}$$



The amplifier will band-limit the system!

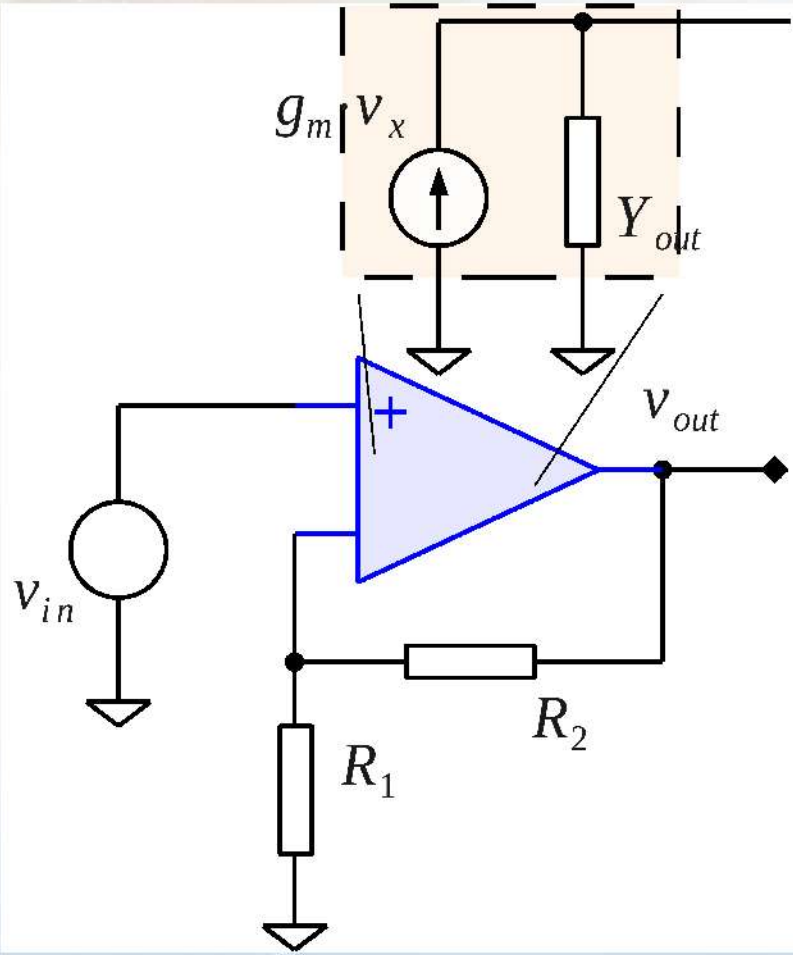
More detailed model

$$v_x = \frac{R_1}{R_1 + R_2} \cdot v_{out}$$

$$g_m(v_{in} - v_x) + (0 - v_{out})Y_{out} + \frac{0 - v_{out}}{R_1 + R_2} = 0$$

$$g_m v_{in} = v_{out} \cdot \left[Y_{out} + \frac{1 + R_1 g_m}{R_1 + R_2} \right]$$

$$\frac{v_{out}}{v_{in}} = \frac{\Gamma}{1 + \frac{1}{g_m R_1} + \frac{\Gamma}{g_m / Y_{out}}}$$, etc., etc.



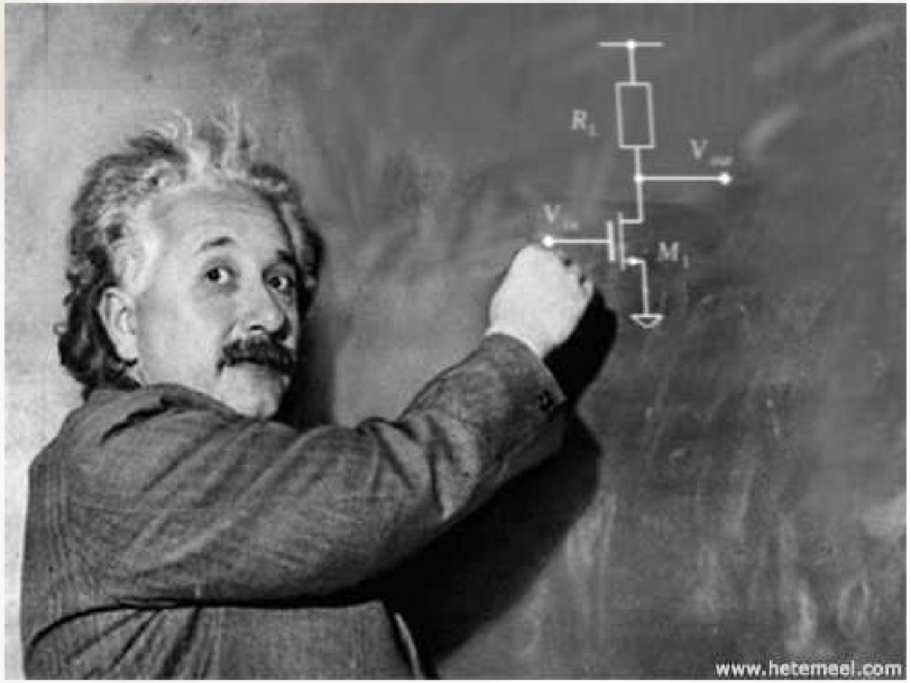
Other practical concerns wrt. current

Feedback with resistors

An OP given with a certain current drive capability will put requirements on the resistor sizes

What is the maximum swing?

What is the DC level?



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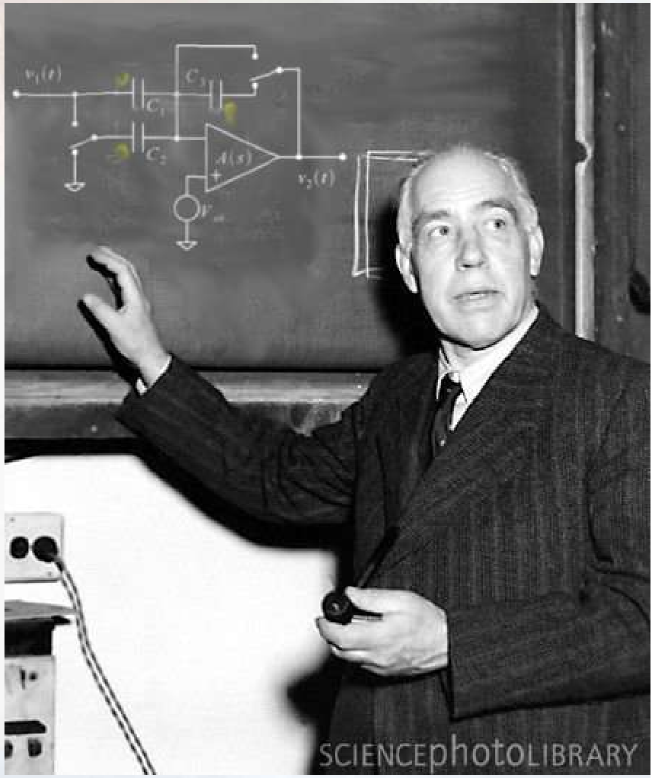
Other practical concerns wrt. gain



Integrator

Effect of limited gain on integration operation. Maximum integration is A_0.

Low-pass filter

Effect on the filter bandwidth

How fast?

A closed-loop gain of 10 and a bandwidth of 25 MHz

The "741 amplifier"

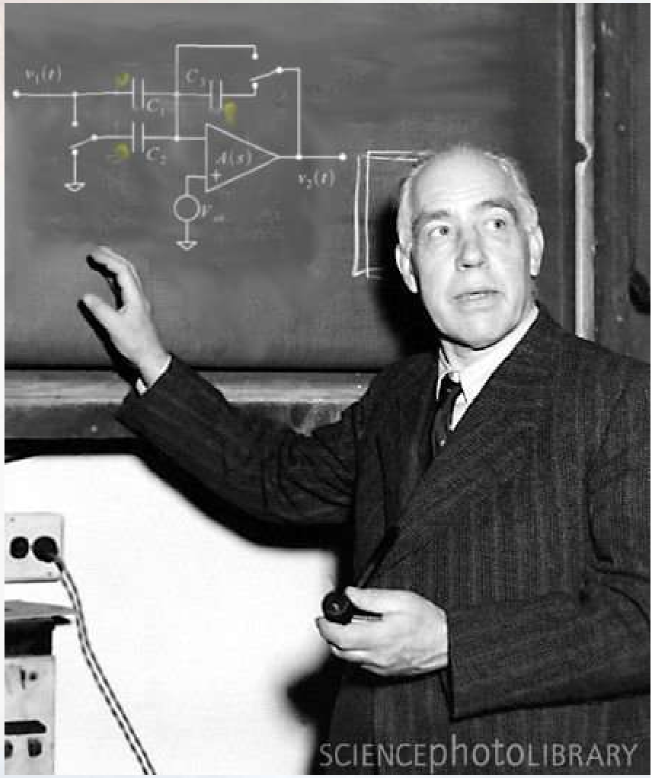
Texas instruments

opa 336 - what is the bandwidth?

opa 358 - what is the DC gain?

Analog Devices

AD854x - what is the DC gain, or what is the open-loop bandwidth?



Operational amplifier architectures

Examples

- Telescopic
- Two-stage
- Folded-cascode
- Current-mirror

Essentially just cascaded stages of different kinds

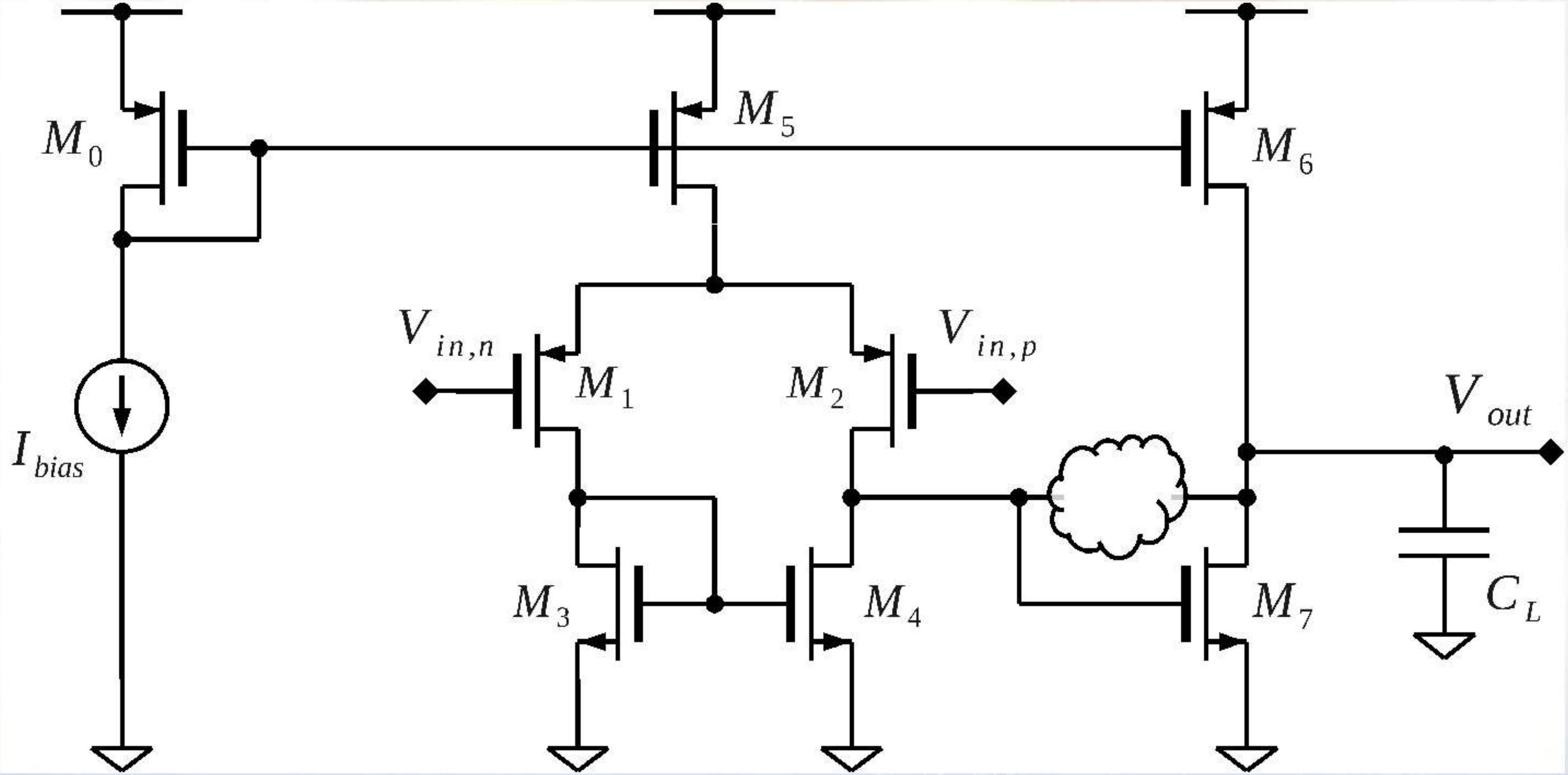
Telescopic OTA

Stack many cascodes on top of each-other and use gain-boosting, etc.

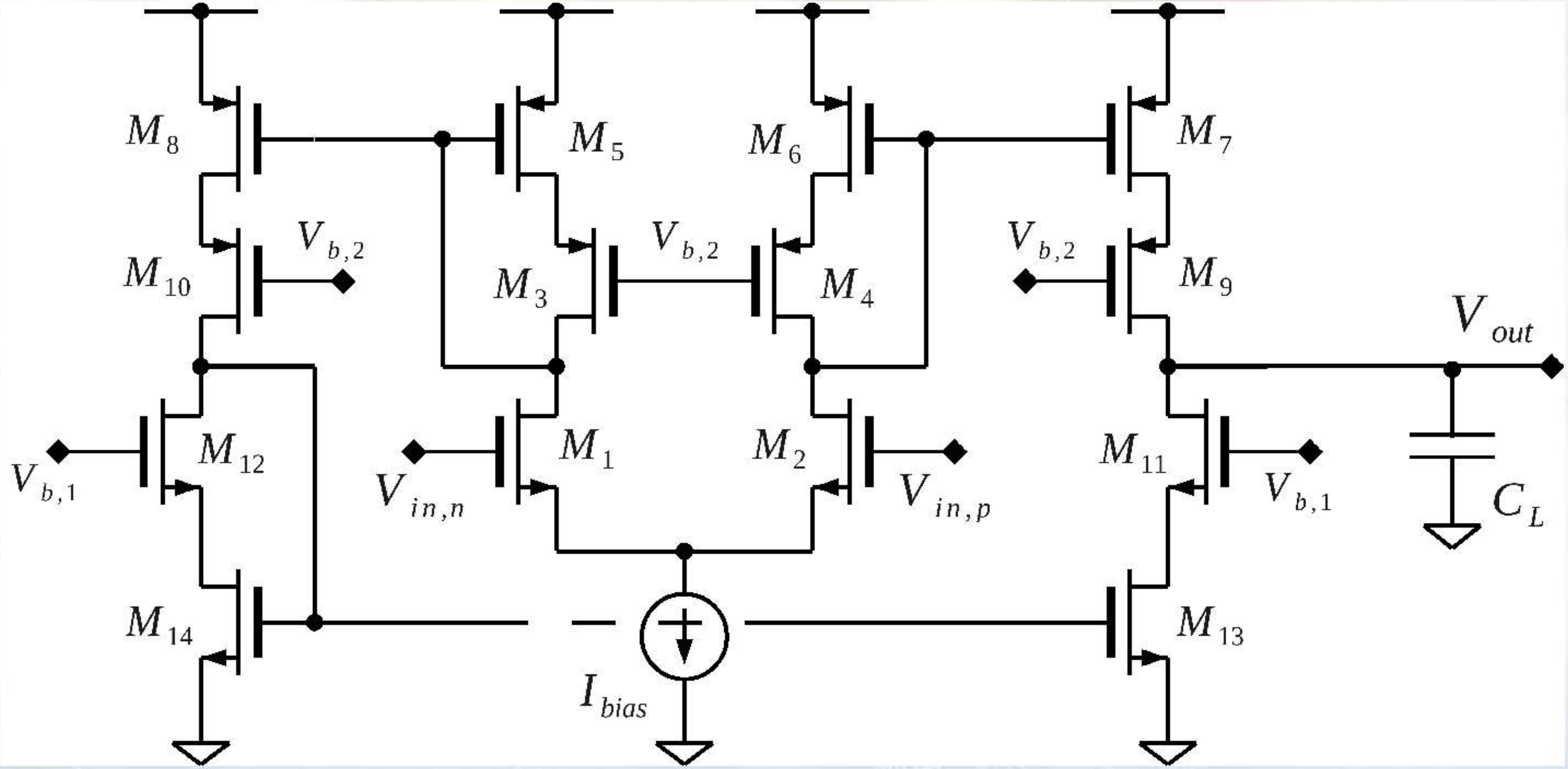
Omitted, since it is not applicable for modern processes.

The swing is eaten up.

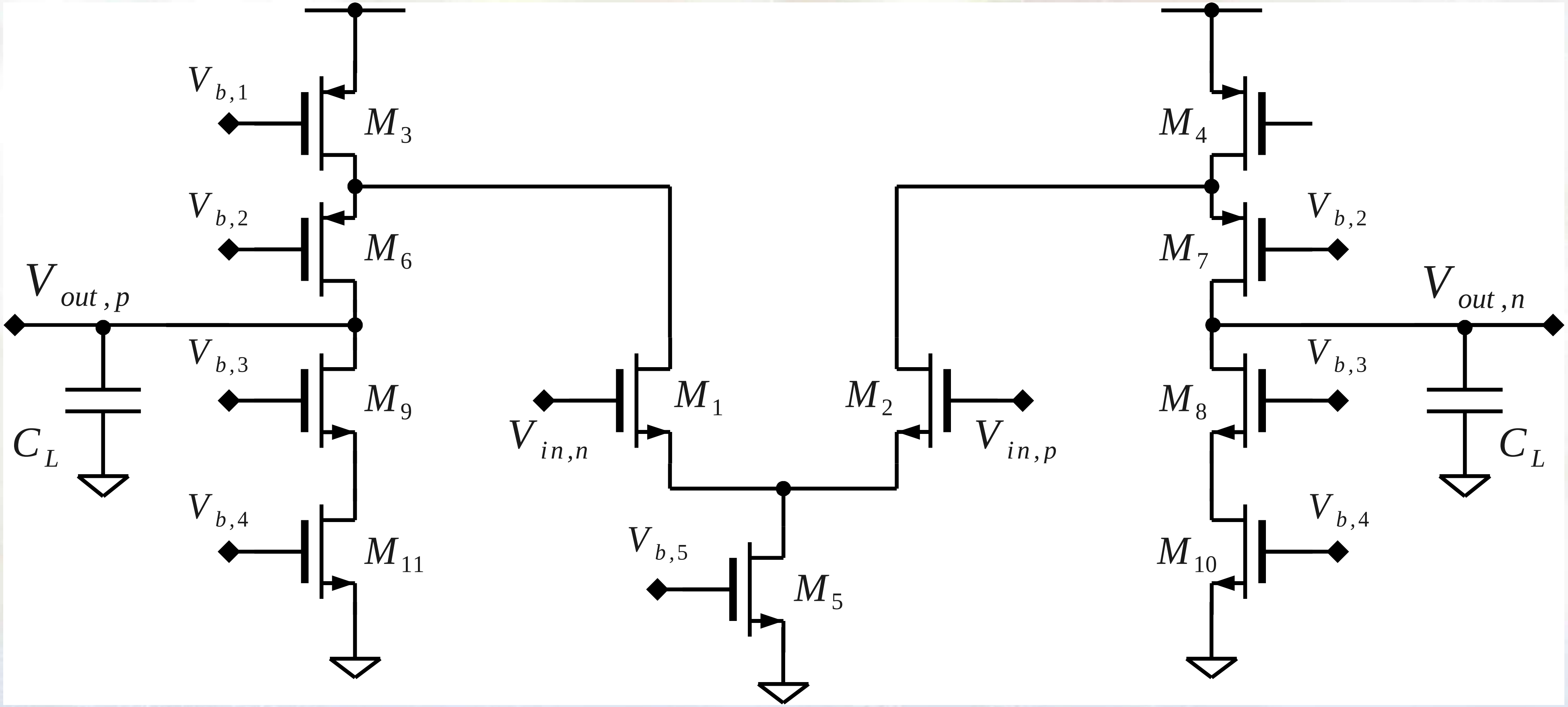
Two-stage OP/OTA



Current-mirror OP/OTA



Folded-cascode OP/OTA



OP/OTA Compilation

Cookbook recipes

Hand-outs with step-by-step explanation of the design of OP/OTAs

http://www.es.isy.liu.se/courses/ANDA/download/opampRef/ANTIK_0NNN_LN_opampHandsouts_A.pdf

Compensation techniques

http://www.es.isy.liu.se/courses/ANDA/download/opampRef/ANTIK_0NNN_LN_opampCompensationTable_A.pdf

Amplifier classes

Not really covered in this course.

Different classes, such as

Class A, B, AB, C, D, E, F, G, H, I, K, S, T, Z, etc.

Class A

Essentially the common-source stage

Class AB

Essentially a push-pull configured class A

What did we do today?

Wrapped up the CMOS part of the course

Wrapped a discussion on stability and compensation

Looked on the opamp

- macro level
- chip level

What will we do next time?

Distortion

- How is linearity of analog circuits defined?
- What other cost measures are there to define analog quality?

Noise

- What are the fundamental limits on performance and range?
- What are the mathematical tools to find them?

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