Lecture 2, Amplifiers

CMOS, Analog building blocks

LiU EXPANDING REALITY

What did we do last time?

Mainly an introduction to the course

Labs, quizzes, exam, etc.

The CMOS transistor

PMOS vs NMOS

Operating regions (cut-off, linear, saturation)

Functionality (output current as a function of the width and length)

First amplifier and parameters

First a common-source with resistive load

What will we do today?

Small-signal schematics

Linearization

Analog building blocks

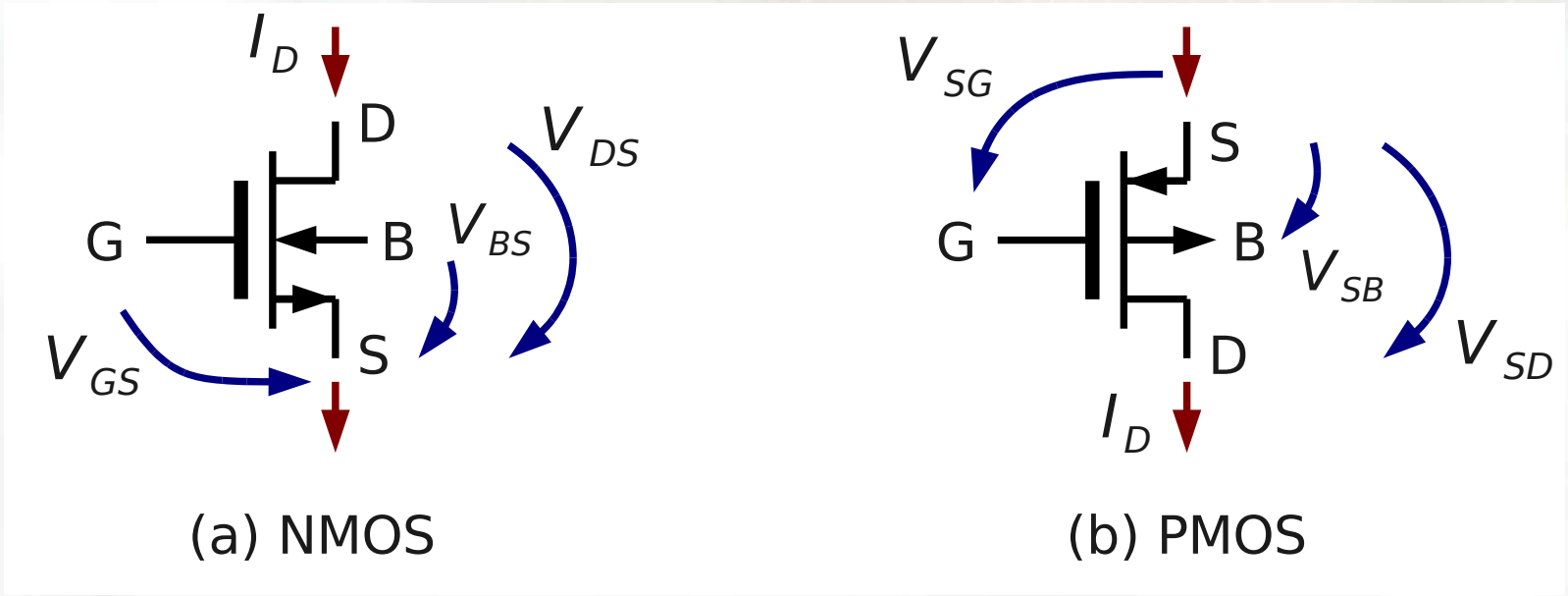
Common-source, common-drain, common-gate, etc.

Frequency domain

Dominant poles

Multiple poles, stability

The transistor revisited



The first amplifier revisited

A common-source amplifier

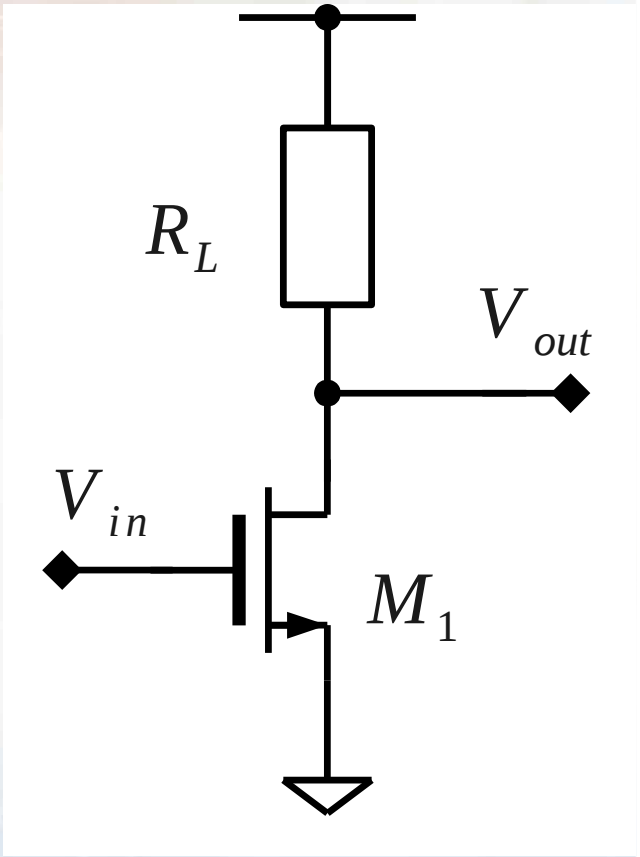
$$v_{out} = V_{DD} - R_L \cdot I_D$$

Saturation region (desired)

$$v_{out} = V_{DD} - R_L \cdot \alpha \cdot v_{eff}^2$$

Linear region

$$v_{out} = V_{DD} - R_L \cdot \alpha \cdot \left(2 v_{out} v_{eff} - v_{out}^2 \right)$$

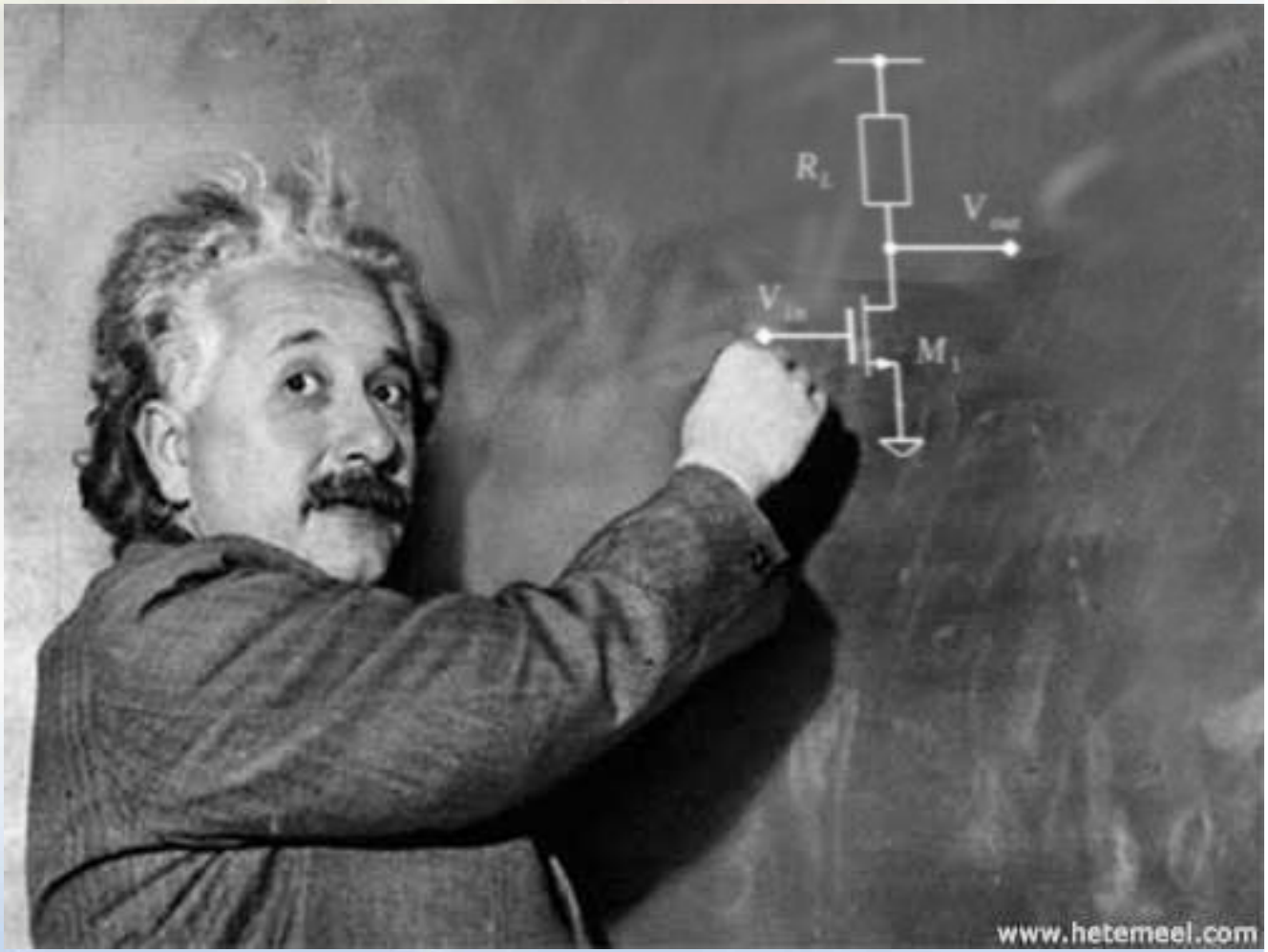


The first amplifier revisited

Large-signal transfer characteristics

Position of DC point

Other design requirements



Small-signal schematics

Linearization around a DC point

Assume small variations around the DC point

Superimpose contributions from all sources to the output

Linearization implies no distortion, no clipping, etc.

Notice that there might be a trade-off between swing and max gain

The choice of DC point is non-trivial... maximum gain? maximum swing?

Linearization example

Original

$$I_D = \frac{\mu C_{ox}}{2} \cdot \frac{W}{L} \cdot (V_{gs} - V_T)^2 \cdot \left(1 + \frac{V_{ds}}{V_\theta}\right)$$

Apply partial derivation, i.e., linearize

$$\Delta I_D = \frac{d I_D}{d \mu} \cdot \Delta \mu + \frac{d I_D}{d C_{ox}} \cdot \Delta C_{ox} + \frac{d I_D}{d W} \cdot \Delta W + \frac{d I_D}{d L} \cdot \Delta L +$$
$$+ \frac{d I_D}{d V_{GS}} \cdot \Delta V_{GS} + \frac{d I_D}{d V_T} \cdot \Delta V_T + \frac{d I_D}{d V_{DS}} \cdot \Delta V_{DS} + \frac{d I_D}{d V_\theta} \cdot \Delta V_\theta$$

Linearization example, cont'd

We assume the physical parameters to be constant

$$\Delta I_D = \frac{d I_D}{d V_{GS}} \cdot \Delta V_{GS} + \frac{d I_D}{d V_{DS}} \cdot \Delta V_{DS} + \frac{d I_D}{d V_T} \cdot \Delta V_T$$

Apply the chain rule

$$\frac{d I_D}{d V_T} \cdot \Delta V_T = \frac{d I_D}{d V_T} \cdot \frac{d V_T}{d V_{BS}} \cdot \Delta V_{BS}$$

Linearization example, cont'd

Introduce some nomenclature

$$\Delta I_D = \underbrace{\frac{d I_D}{d V_{GS}}}_{g_m} \cdot \Delta V_{GS} + \underbrace{\frac{d I_D}{d V_{DS}}}_{g_{ds}} \cdot \Delta V_{DS} + \underbrace{\frac{d I_D}{d V_T} \cdot \frac{d V_T}{d V_{BS}}}_{g_{mbs}} \cdot \Delta V_{BS}$$

and skip the deltas

$$i_d = g_m \cdot v_{gs} + g_{ds} \cdot v_{ds} + g_{mbs} \cdot v_{bs}$$

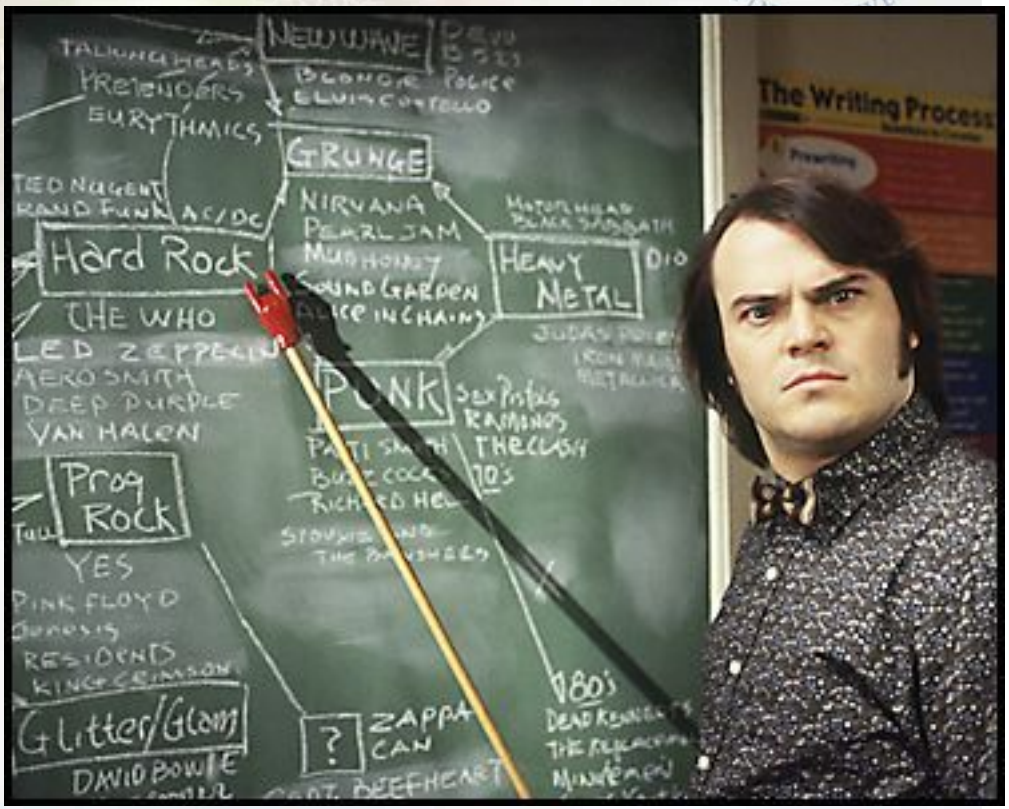
Which gives us a transistor "consisting" of three current sources

The small signal model and its impact

Illustrating the small signal model

Some calculations

(More practice in the lessons)



Transistors compiled

Parameter	Cut-off	Linear	Saturation
g_m	$\frac{\kappa I_D}{kT/q}$	$2\alpha v_{ds}$	$\frac{2I_D}{v_{eff}}$ and $2\sqrt{\alpha I_D}$
g_{mbs}	$g_m \cdot \frac{1-\kappa}{\kappa}$	$g_m \cdot \frac{\gamma}{2\sqrt{V_{SB}+2\phi_F}}$	$g_m \cdot \frac{\gamma}{2\sqrt{V_{SB}+2\phi_F}}$
g_{ds}	λI_D	$2\alpha\left(v_{eff}-v_{ds}\right)$	λI_D

How large are these values?

Transistor gain vs region

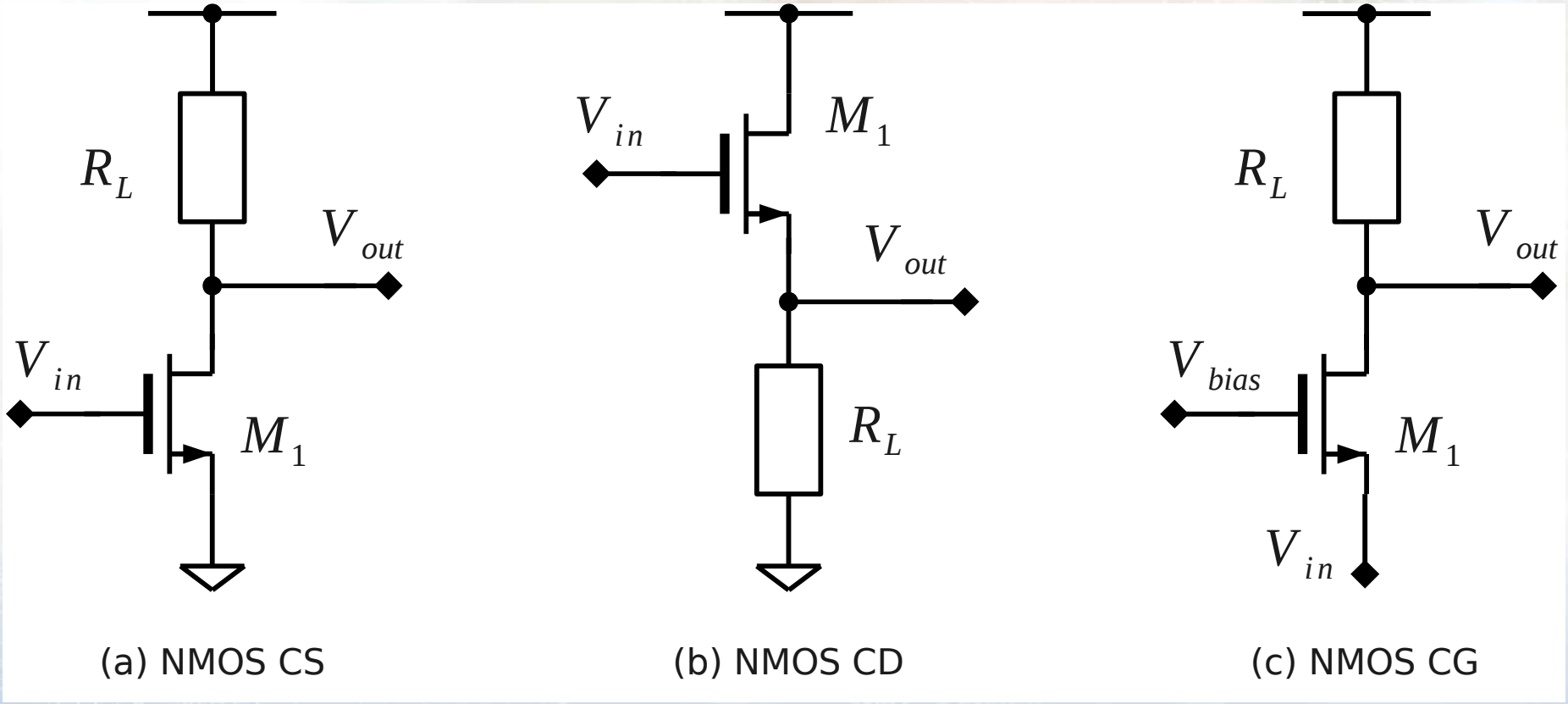
Expression	Cut-off	Linear	Saturation	
$A = \frac{g_m}{g_{ds}}$	$\frac{\kappa \cdot q}{\lambda \cdot k T}$	$\frac{v_{ds}}{v_{eff} - v_{ds}}$	$\frac{2}{\lambda \cdot v_{eff}}$	$\frac{2\sqrt{\alpha}}{\lambda \sqrt{I_D}}$

Where is highest gain?

$\kappa \approx 0.75$ and $k T / q \approx 26$ mV.

The three amplifier stages

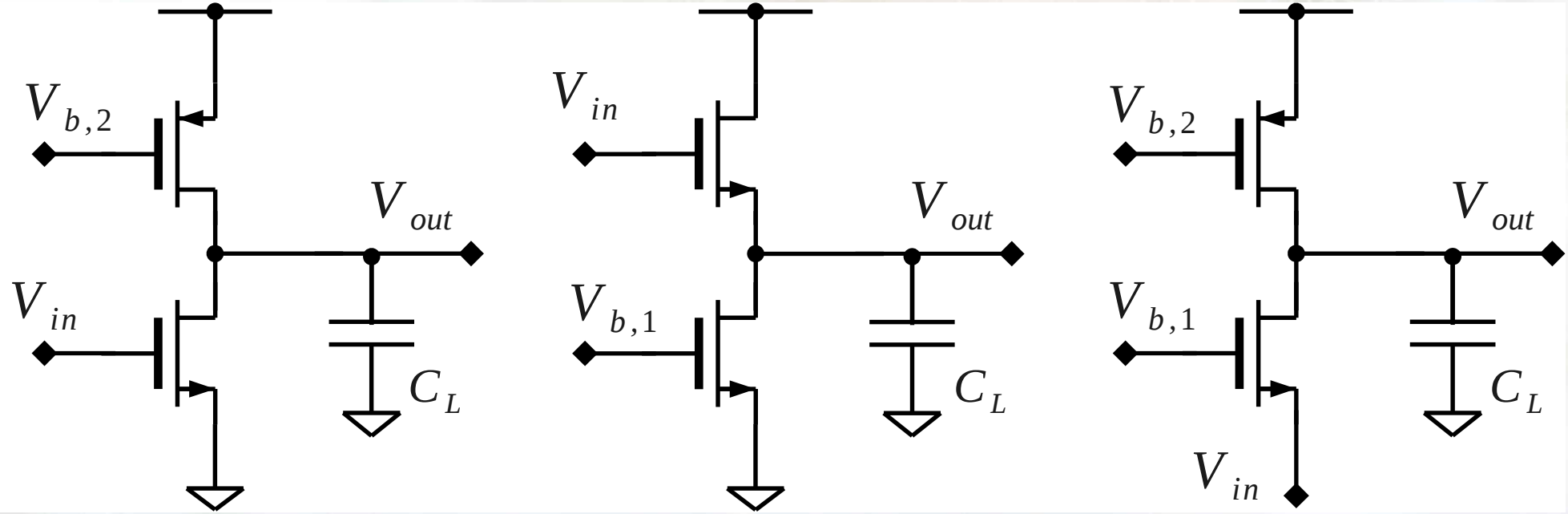
With passive load



(a) NMOS CS (b) NMOS CD (c) NMOS CG

The three amplifier stages, cont'd

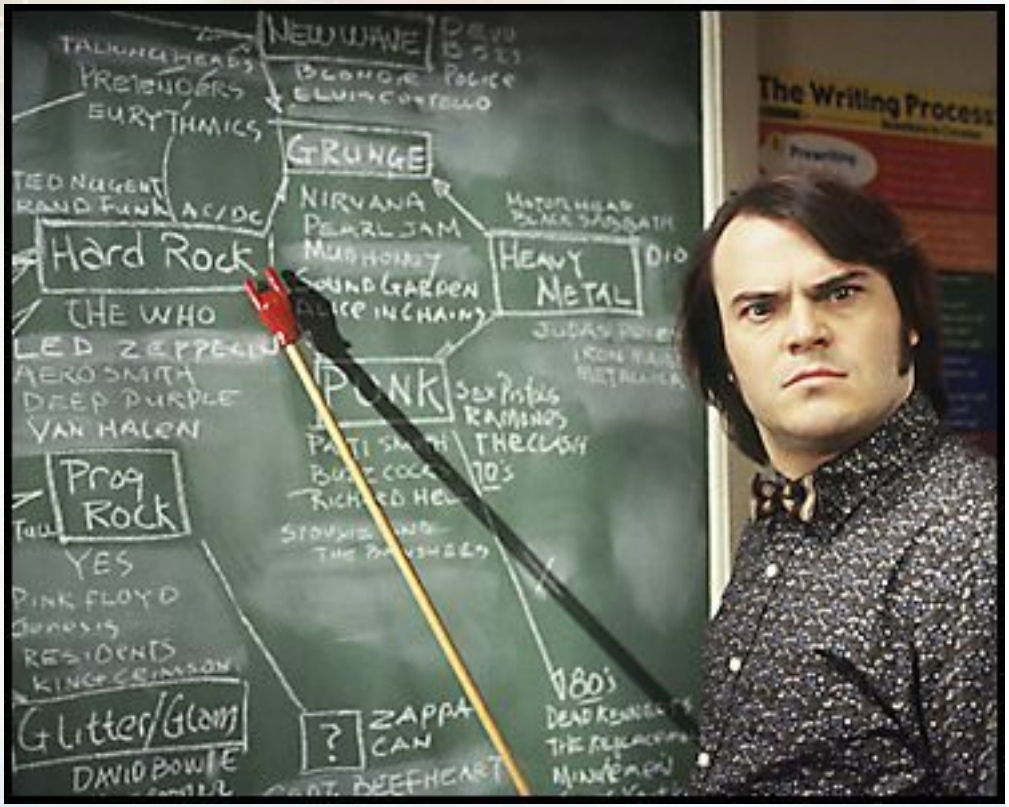
With active load



Why active load?

The small signal exercises

Using the small signal approach to derive the gain



Amplifier stages, compiled 1

Expression	CS	CD	CG
DC gain, $A_0 \approx g_m / g_{out}$	$\approx \frac{g_m}{g_P + g_N}$	$\approx \frac{g_m}{g_m + g_P + g_N} \approx 1$	$\approx \frac{g_m}{g_P + g_N}$
Output impedance, $\approx g_{out}$	$\approx g_P + g_N$	$\approx g_m$	$\approx g_P + g_N$
Input impedance, $\approx g_{in}$	∞	∞	$\approx g_m$
Bandwidth, $p_1 \approx g_{out} / C_L$	$\approx \frac{g_P + g_N}{C_L}$	$\approx g_m / C_L$	$\approx \frac{g_P + g_N}{C_L}$
Unity gain, $\approx A_0 \cdot p_1$	$\approx g_m / C_L$	N/A (why?)	$\approx g_m / C_L$

Amplifier stages, compiled 2

Expression	CS	CD	CG*)
DC gain, $A_0 \approx g_m / g_{out}$	$\approx 1/\lambda \cdot v_{eff}$	≈ 1	$\approx 1/\lambda \cdot v_{eff}$
Output impedance, $\approx g_{out}$	$\approx \lambda I_D$	$\approx 2 I_D / v_{eff}$	$\approx \lambda I_D$
Input impedance, $\approx g_{in}$	∞	∞	$\approx 2 I_D / v_{eff}$
Bandwidth, $p_1 \approx g_{out} / C_L$	$\approx \lambda I_D / C_L$	$\approx 2 I_D / C_L \cdot v_{eff}$	$\approx \lambda I_D / C_L \cdot v_{eff}$
Unity gain, $\approx A_0 \cdot p_1$	$\approx I_D / C_L \cdot v_{eff}$	N/A (why?)	$\approx I_D / C_L \cdot v_{eff}$

Amplifier stages, compiled 3

Amplifier	When and what to use?
Common-source	High-gain amplifier with high output impedance and high input impedance. Drives capacitive loads, typically in feedback configuration.
Common-gate	High-gain amplifier with high output impedance and "low" input impedance. Drives capacitive loads, typically in feedback configuration.
Common-drain	Low-gain amplifier with "low" output impedance and high input impedance. Drives resistive loads, can be in open-loop.

How to increase gain?

Assuming a simple common-source stage:

$$A = \frac{g_m}{g_{out}} = \frac{1}{\lambda \cdot v_{eff}} = \frac{2\sqrt{\alpha}}{\lambda\sqrt{I_D}}$$

The answer depends on the biasing conditions!

Decrease v_{eff}

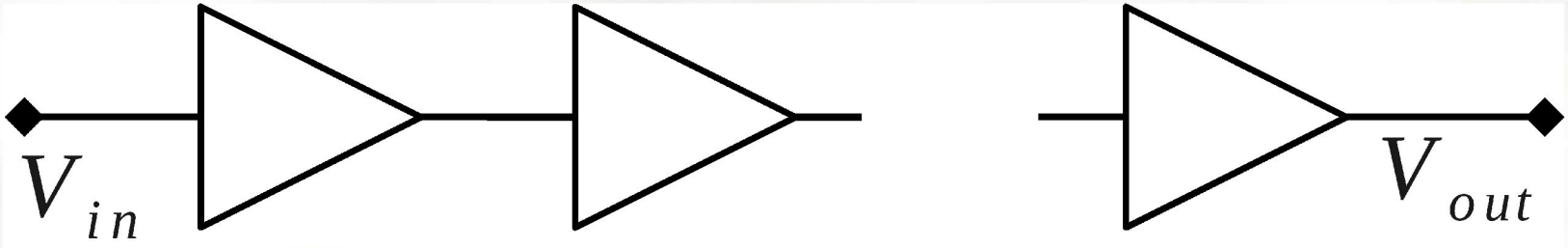
Decrease $\lambda \sim 1/L$, i.e., increase the channel length.

Decrease (!) the current I_D

Increase the transistor sizes, $\alpha \sim S \sim W$

Improving the gain, the obvious option

We can put several stages in series



Total gain is the product of all gains

Offers high swing

Might cost us more power consumption (each stage needs current)

Improving the gain, the electrical option

Revisit the expression on gain!

$$A = \frac{g_m}{g_{out}}$$

Increase the transconductance

Decrease the output conductance (i.e., increase output impedance)

We've done that kind of, c.f., lowering the v_{eff}, etc.

Cascodes, the hardware option

Introduce more hardware to increase impedance

Cascodes increase the gain

How? - a small-signal exercise

We must balance the load

both in PMOS and NMOS "direction"

(Traditional way to maximize power efficiency)

So ... it's all about impedance levels

Cascodes

(Quickly) eats up the voltage headroom

For every diode-connected transistor, we loose one V_T of swing

We can save current since only one stage

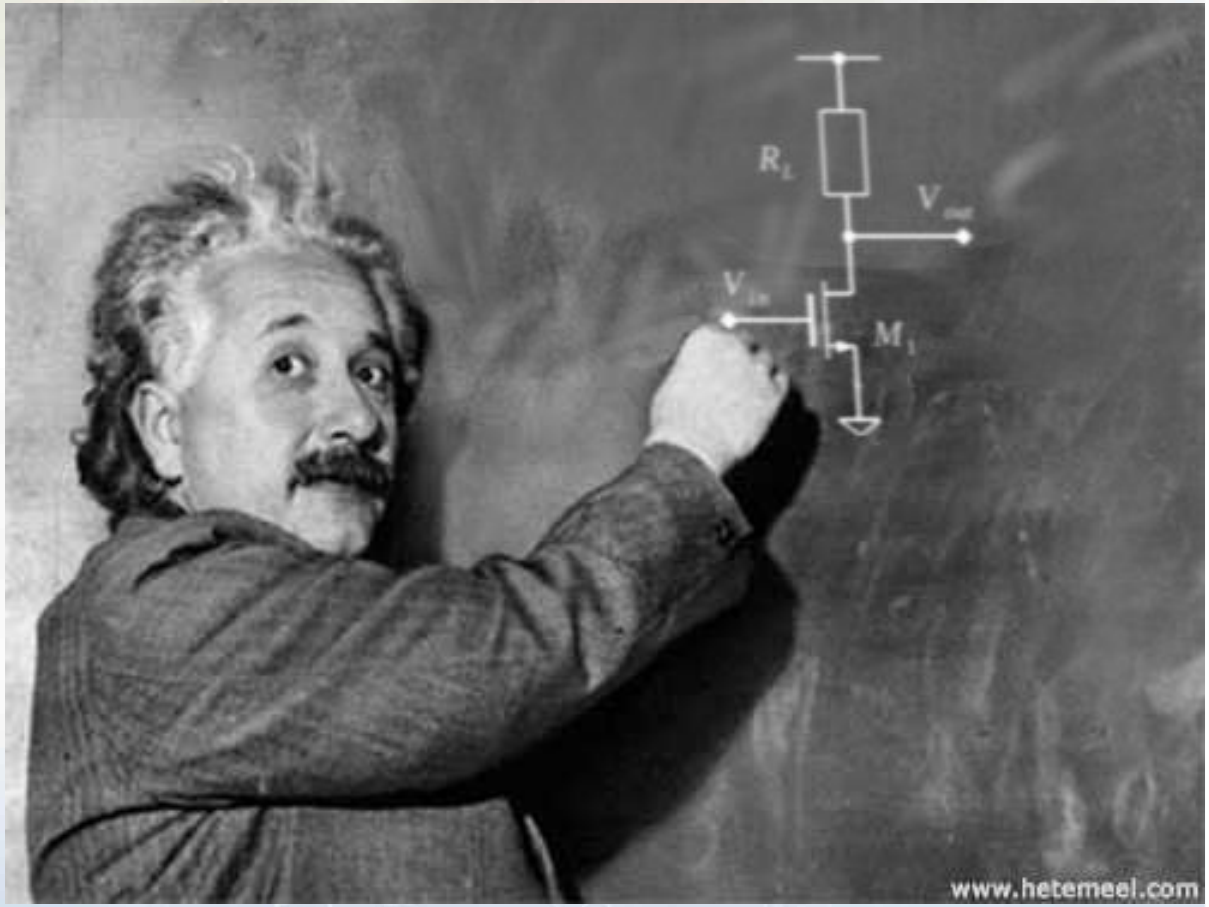
Complex biasing schemes

"The output impedance is multiplied"

Cascodes, common-source example

Voltage swing

Calculating the gain



Cascodes, common-source example

Formula still holds $A = g_m / g_{out}$ **and the output conductance is**

$$A = \frac{g_{m1}}{\frac{g_{n1} \cdot g_{n2}}{g_{m2}} + \frac{g_{p3} \cdot g_{p4}}{g_{m3}}} \approx \frac{g_{m1} \cdot g_{m2}}{2 \cdot g_{n1} \cdot g_{n2}}$$

Now, we have some more handles to increase (set) the gain.

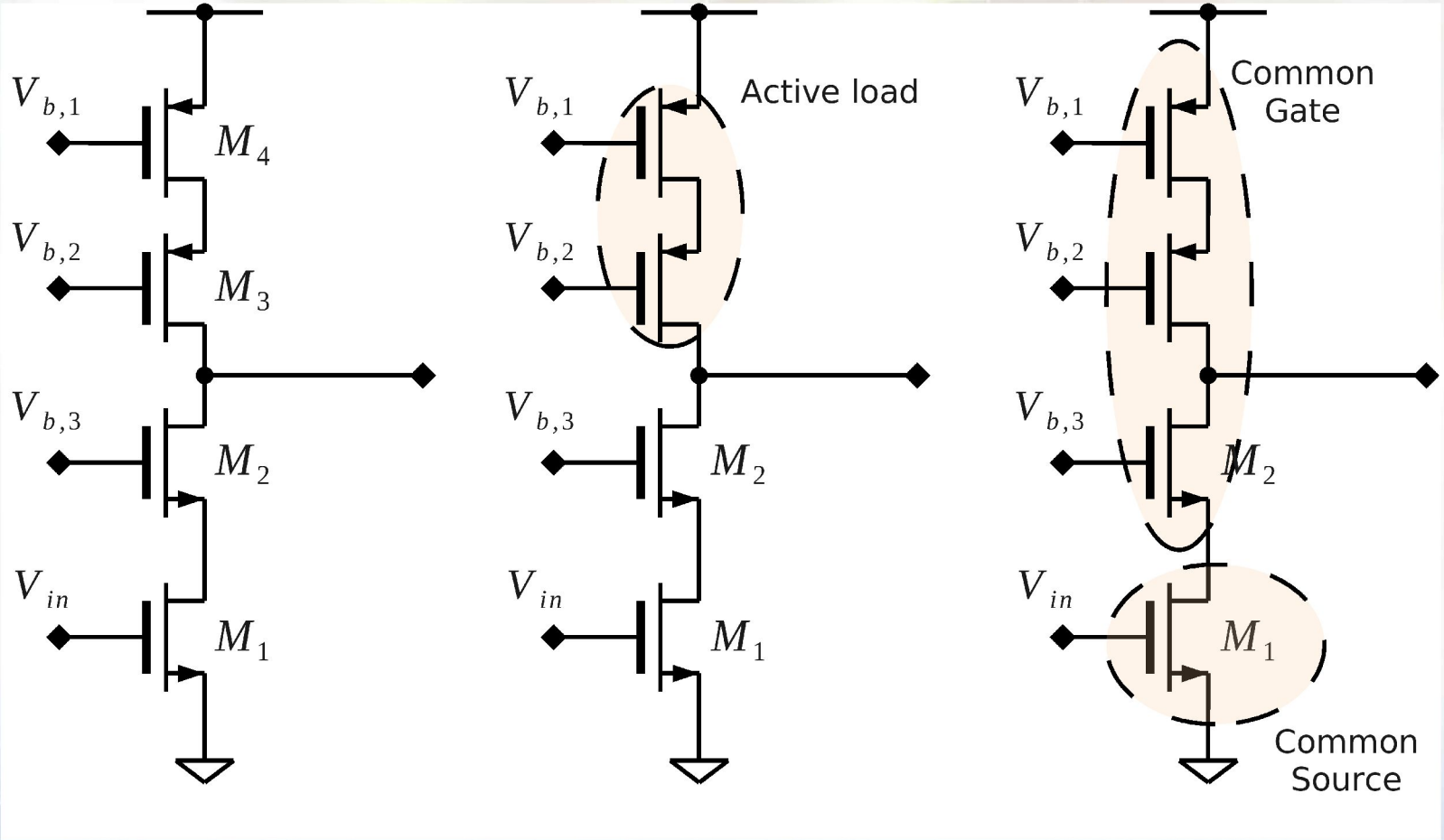
Effective voltage of input can be decoupled.

Classical analog trade-offs to distribute the gain).

But ... what happens to the gain if

the impedance levels are not balanced?

Cascodes are also multiple stages ...



Some conlusions on one slide

Cascodes eat up the swing

Cascodes save current compared to multi-stage

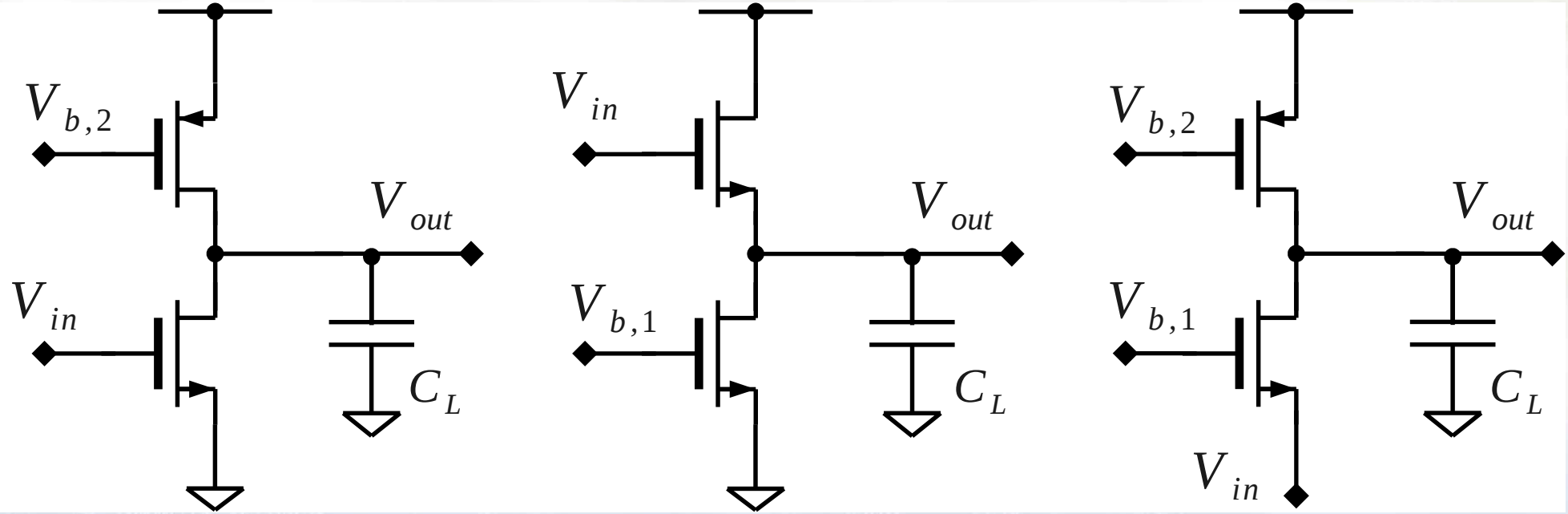
Cascodes and multi-stage have comparatively same area

Cascodes have more complex biasing schemes compared to multi-stage amplifiers

Cascodes might not be feasible in future (analog) designs

The frequency domain

Include the capacitor in your calculations



The frequency domain

Small-signal exercise

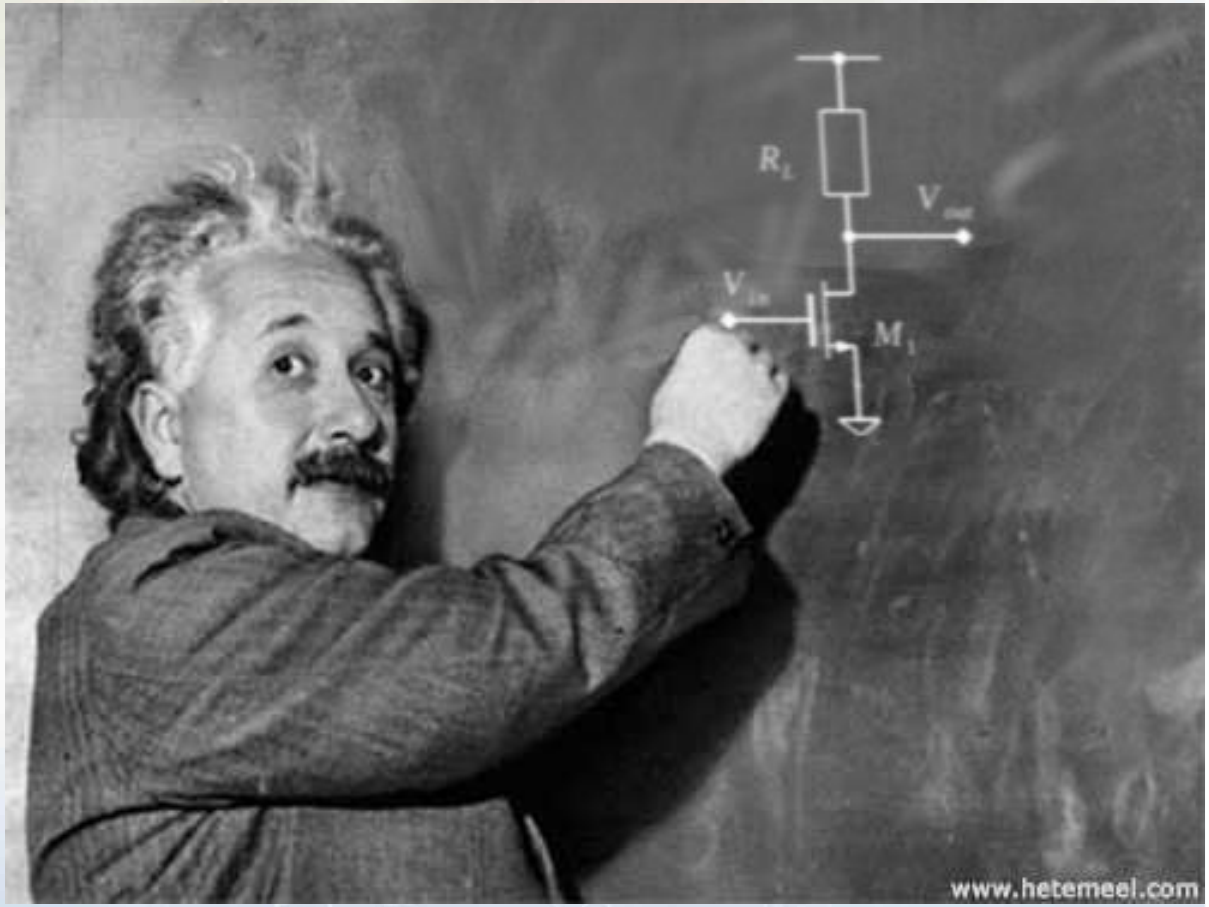
Impact of capacitor on common-source stage

Bode plot

Pole

DC gain

Unity-gain frequency



Compilation

The overall transfer function

$$A(s)=\frac{A_0}{1+\frac{s}{p_1}}=\frac{g_m/g_{out}}{1+\frac{s}{g_{out}/C_L}}$$

(Sw. “normalform”)

Notice the trade-off between bandwidth and gain!

$$A_0 \cdot p_1 \approx \omega_{ug}$$

Amplifier stages, compiled 1

Expression	CS	CD	CG*)
DC gain, $A_0 \approx \frac{g_m}{g_{out}}$	$\approx \frac{g_m}{g_P + g_N}$	$\approx \frac{g_m}{g_m + g_P + g_N} \approx 1$	$\approx \frac{g_m}{g_P + g_N}$
Output impedance, $\approx g_{out}$	$\approx g_P + g_N$	$\approx g_m$	$\approx g_P + g_N$
Bandwidth, $p_1 \approx \frac{g_{out}}{C_L}$	$\approx \frac{g_P + g_N}{C_L}$	$\approx \frac{g_m}{C_L}$	$\approx \frac{g_P + g_N}{C_L}$
Unity gain, $\approx A_0 \cdot p_1$	$\approx g_m / C_L$	N/A (why?)	$\approx g_m / C_L$

*) Source impedance not mentioned, see the exercise manual.

Amplifier stages, compiled 2

Expression	CS	CD	CG*)
DC gain, $A_0 \approx \frac{g_m}{g_{out}}$	$\approx \frac{1}{\lambda \cdot v_{eff}}$	≈ 1	$\approx \frac{1}{\lambda \cdot v_{eff}}$
Output impedance, $\approx g_{out}$	$\approx \lambda I_D$	$\approx \frac{2 I_D}{v_{eff}}$	$\approx \lambda I_D$
Bandwidth, $p_1 \approx \frac{g_{out}}{C_L}$	$\approx \frac{\lambda I_D}{C_L}$	$\approx \frac{2 I_D}{C_L \cdot v_{eff}}$	$\approx \frac{\lambda I_D}{C_L \cdot v_{eff}}$
Unity gain, $\approx A_0 \cdot p_1$	$\approx \frac{I_D}{C_L \cdot v_{eff}}$	N/A (why?)	$\approx \frac{I_D}{C_L \cdot v_{eff}}$

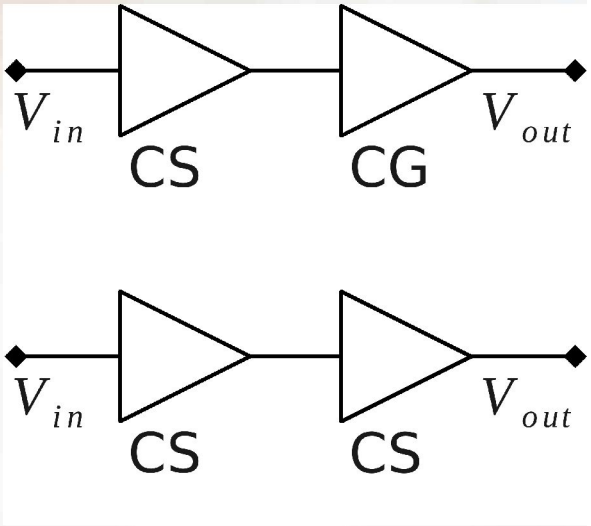
Gain increased with multi-stage amplifiers

Single-stage (cascodes) vs two-stage?

They will have the same DC gain

They will not have the same output impedance

Multiple poles ("one per stage")



The transfer function (in both cases) is

$$A(s)=\frac{A_1 \cdot A_2}{\left(1+\frac{s}{p_{11}}\right)\cdot\left(1+\frac{s}{p_{12}}\right)}$$

Multiple poles

Case 1 (CS+CG)

First amplifier sees low-impedance load: $(g_1+g_{m1})\|C_1 \approx g_{m1}\|C_1$

Second amplifier sees capacitive load: $g_{out} \approx g_2\|C_2$

Case 2 (CS+CS)

First amplifier sees high-impedance load $(g_1+0)\|C_1 \approx g_1\|C_1$

Second amplifier sees capacitive load: $g_{out} \approx g_2\|C_2$

Notice that the g_2 in Case 2 is higher than g_2 in Case 1.

Regardless what you do ... Feedback

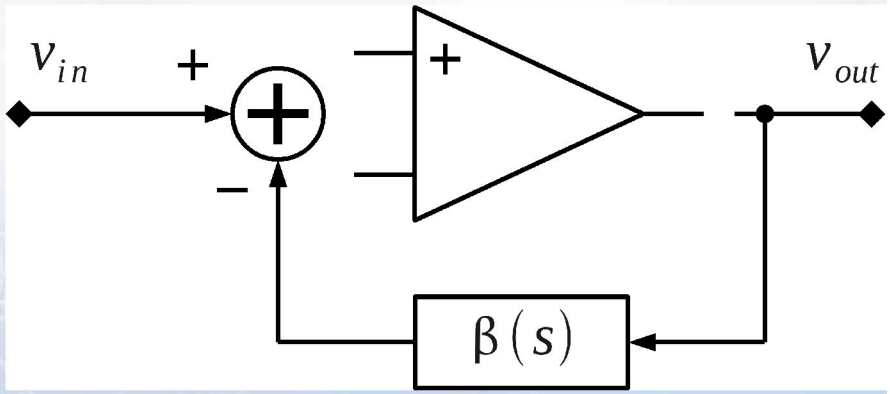
Preferably, we have a controlled system with a closed-loop gain of:

$$Y(s)=\left(X(s)-\beta(s)\cdot Y(s)\right)\cdot A(s)\Rightarrow$$

$$\frac{Y(s)}{X(s)}=\frac{A(s)}{1+\beta(s)\cdot A(s)}=\frac{1/\beta(s)}{1+\frac{1}{\beta(s)\cdot A(s)}}$$

A feedback factor of: $\beta(s)$

An open-loop gain of: $\beta(s)\cdot A(s)$



Why do you want controlled feedback?

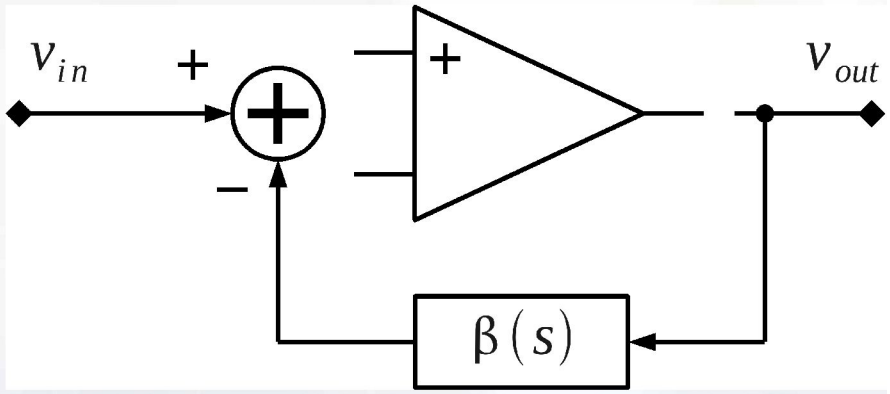
Gain is now under control!

No variation with g_m/g_{ds}, instead given by (normally) high-accuracy components

"Unlimited" drive capability

Isolation of input and output

Linearization



Remember, it is a regulation loop. It is designed to track the changes, anything added in the loop will be supressed.

The problem: Stability

In short: the transfer function must be designed such that

$$\beta(s)\cdot A(s)\neq -1$$

If this is the case, we have an infinitely high transfer function

(In reality, the whole proof is quite complex.)

Phase margin (how far are we off from this to happen)

Poor phase margin gives ringing in the output when applying step

Critically damped signal at approximately 70 degrees (poles become real rather than complex pair, i.e., they are well splitted)

The problem: Stability, cont'd

Bode plot

What happens to the transfer characteristics?

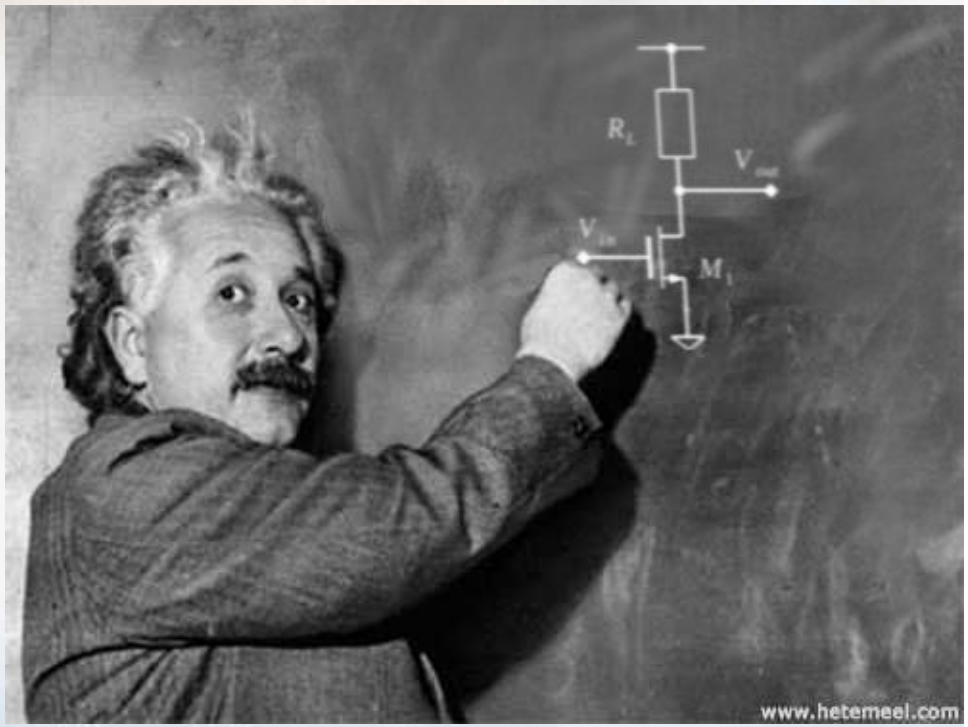
Phase margin

Step response

Settling

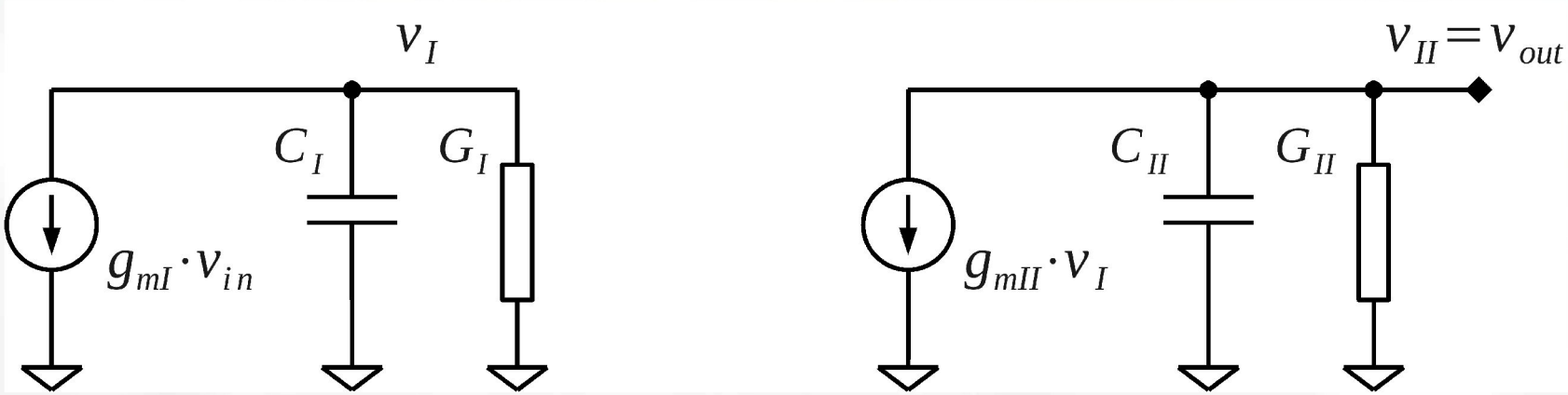
Oscillations

Critically damped at 70 degrees



We need to be a bit more systematic

The model (high-impedance load) and focus on two-pole systems



$$p_1 = \frac{G_I}{C_I},\ p_2 = \frac{G_{II}}{C_{II}},\ A_1 = \frac{g_{mI}}{G_I},\ A_2 = \frac{g_{mII}}{G_{II}}$$

Dominant pole assumption (output)

Assuming pole splitting, $p_2 \gg p_1$, gives us

$$A(s) = \frac{A_1 \cdot A_2}{\left(1 + \frac{s}{p_{11}}\right) \cdot \left(1 + \frac{s}{p_{12}}\right)} \approx \frac{A_1 \cdot A_2}{1 + \frac{s}{p_1} + \frac{s^2}{p_1 \cdot p_2}}$$

This implies: $\omega_{ug} \approx A_1 \cdot A_2 \cdot p_1$ and

$$\phi_m = 180 - arg\, A(j\omega_{ug}) = 180 - atan\frac{\omega_{ug}}{p_1} - atan\frac{\omega_{ug}}{p_2} \approx 90 - atan\frac{\omega_{ug}}{p_2}$$

$$\phi_m \approx 90 - atan\left(A_0 \cdot \frac{p_1}{p_2}\right)$$

The formulas (dominant load!)

Unity-gain frequency

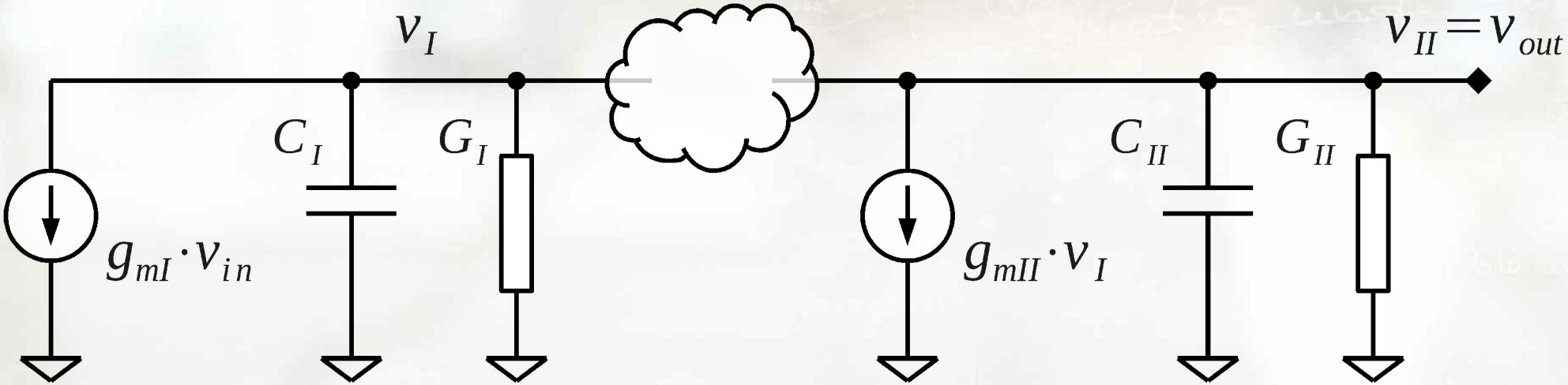
$$\omega_{ug} \approx \frac{g_{mI} \cdot g_{mII}}{G_I \cdot G_{II}} \cdot \frac{G_{II}}{C_{II}} = \frac{g_{mI} \cdot g_{mII}}{G_I \cdot C_{II}}$$

Phase margin

$$\phi_m \approx 90 - atan\frac{\omega_{ug}}{p_2} = 90 - atan\frac{\frac{g_{mI} \cdot g_{mII}}{G_I \cdot C_{II}}}{\frac{G_I}{C_I}} = 90 - atan\frac{g_{mI} \cdot g_{mII} \cdot C_I}{G_I^2 \cdot C_{II}}$$

etc., etc., etc. -- We need to be a bit more organized...

Compensation, poles are too close



The "cloud" could be a capacitor or series resistor-capacitor.

Compensation, Miller capacitance

Introduced zero	Parasitic pole	Dominant pole	Unity-gain
$z_1 = \frac{g_{mII}}{C_C}$	$p_2 = \frac{-g_{mII}}{C_{II}}$	$p_1 = \frac{-G_I \cdot G_{II}}{g_{mII} \cdot C_C}$	$\omega_{ug} = \frac{g_{mI}}{C_C}$

Introduced zero	Parasitic pole	Phase margin
$z_1 \approx 10 \cdot \omega_{ug}$	$p_2 \approx 2.2 \cdot \omega_{ug}$	≈ 60

Dominant pole moves "down", parasitic pole moves "up"

Parasitic zero added (harmful for phase margin)

Compensation, Nulling resistor 1

Introduced zero	Parasitic poles	Dominant pole	Unity-gain
$z_1 = \frac{g_{mII}}{C_C} \cdot \frac{1}{1 - R_Z \cdot g_{mII}}$	$p_2 = \frac{-g_{mII}}{C_{II}}$, $p_3 = \frac{-1}{R_Z \cdot C_{II}}$	$p_1 = \frac{-G_I \cdot G_{II}}{g_{mII} \cdot C_C}$	$\omega_{ug} = \frac{g_{mI}}{C_C}$

$$R_Z = \frac{1}{g_{mII}} \cdot \left(1 + \frac{C_{II}}{C_C}\right)$$

Introduced zero	Parasitic pole	Phase margin
$z_1 \rightarrow p_2$	$p_3 \approx 1.73 \cdot \omega_{ug}$	≈ 60

Compensation, Nulling resistor 2

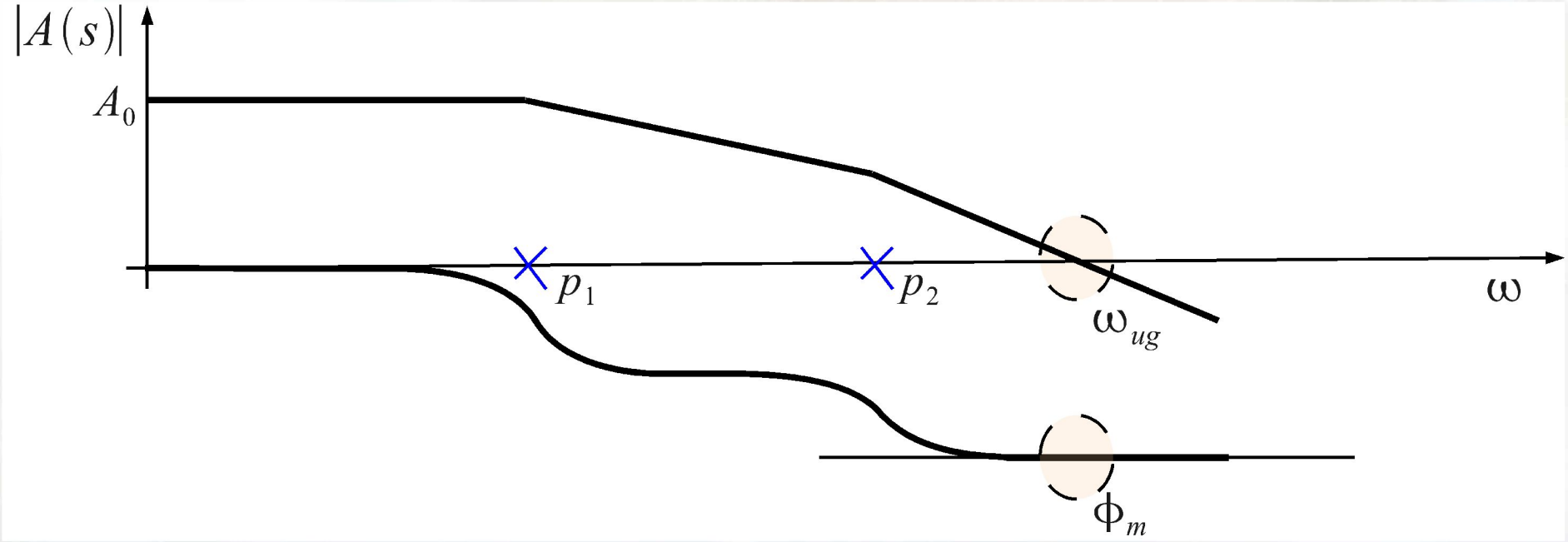
Introduced zero	Parasitic poles	Dominant pole	Unity-gain
$z_1 = \frac{g_{mII}}{C_C} \cdot \frac{1}{1 - R_Z \cdot g_{mII}}$	$p_2 = \frac{-g_{mII}}{C_{II}}$, $p_3 = \frac{-1}{R_Z \cdot C_{II}}$	$p_1 = \frac{-G_I \cdot G_{II}}{g_{mII} \cdot C_C}$	$\omega_{ug} = \frac{g_{mI}}{C_C}$

$$R_Z = \frac{1}{g_{mII}}$$

Introduced zero	Parasitic pole	Phase margin
$z_1 \to \infty$	$p_2 \approx 1.73 \cdot \omega_{ug}$, $p_3 > 10 \cdot \omega_{ug}$	≈ 60

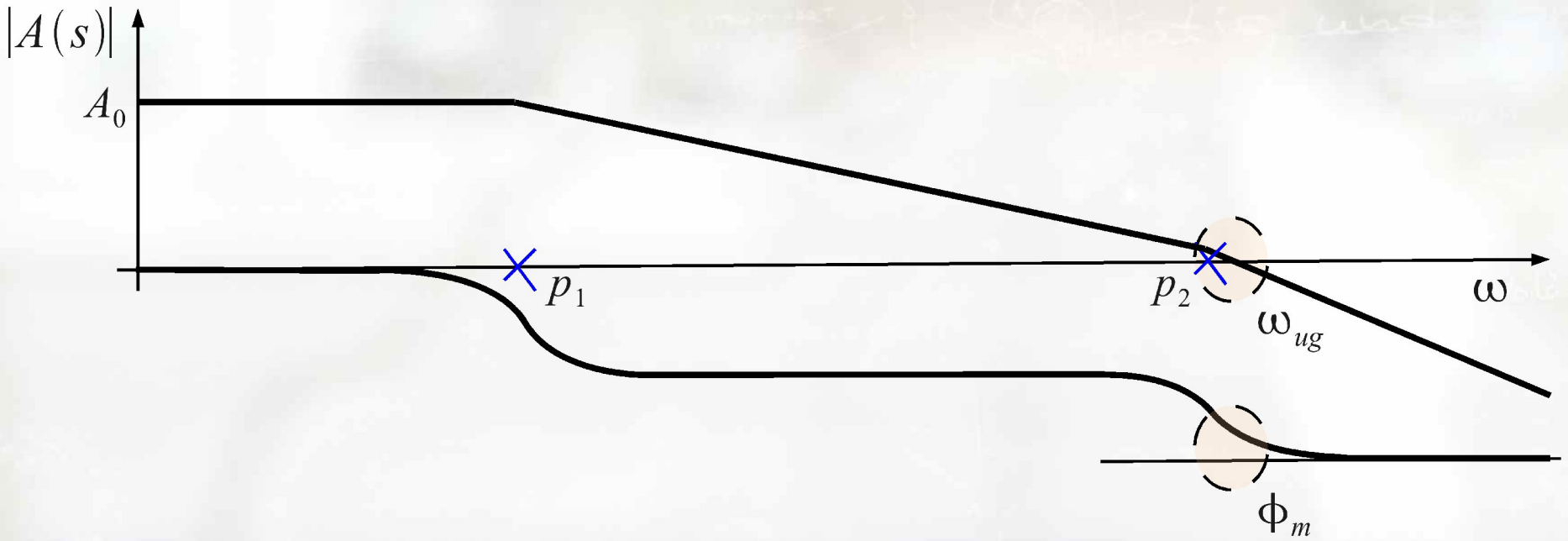
Poles and zeros revisited

Stable?



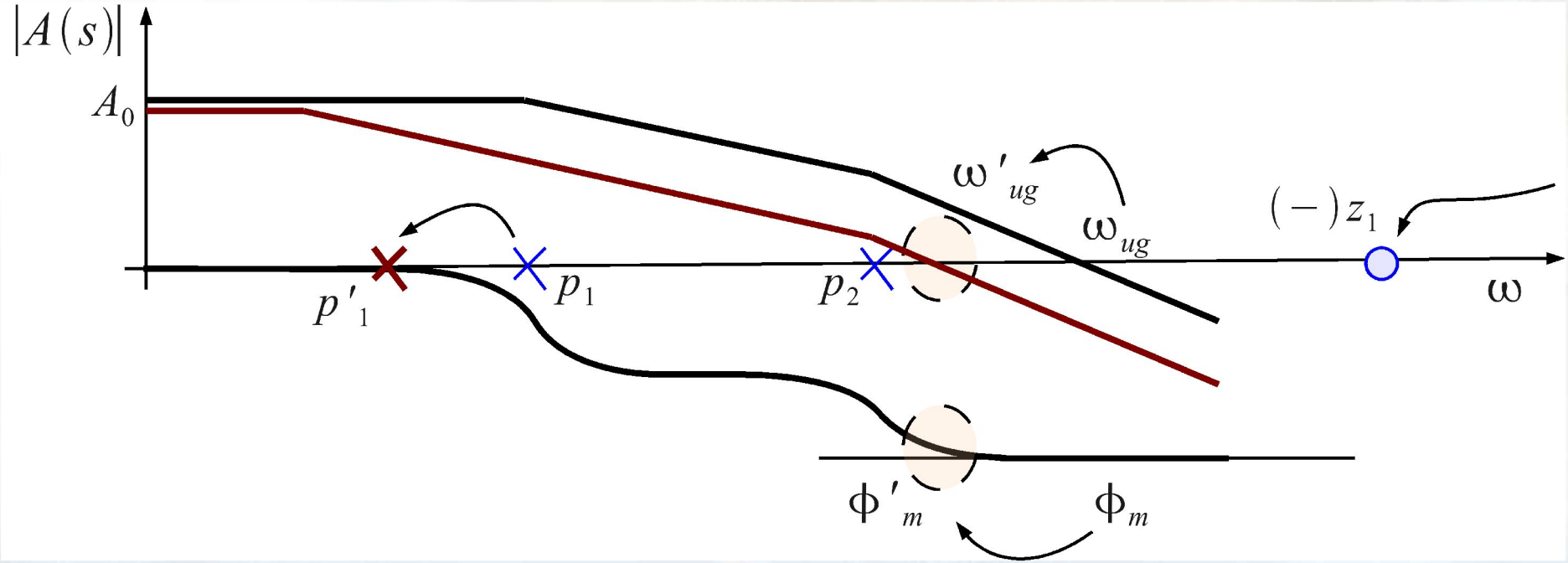
Poles and zeros revisited

Stable?



Compensation

What is the cost associated with compensation?



Compensation, two cases:

1) "Internal" node sees a low-impedance node

Typically: output load dominates, we should drive a capacitive load

Load-compensation, i.e., increase cap externally

2) "Internal" node sees a high-impedance node

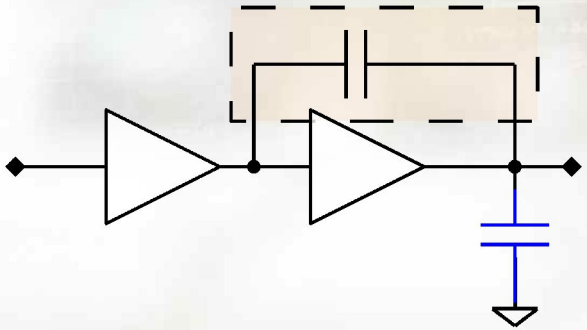
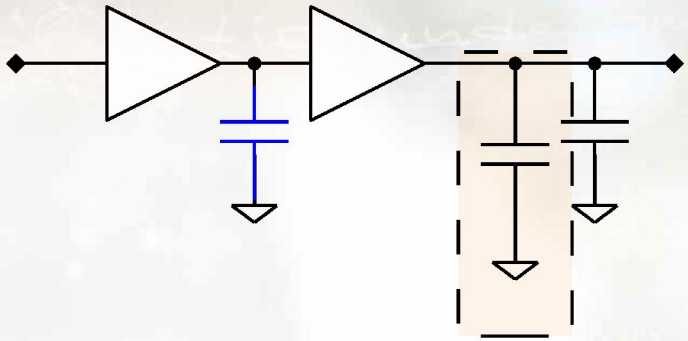
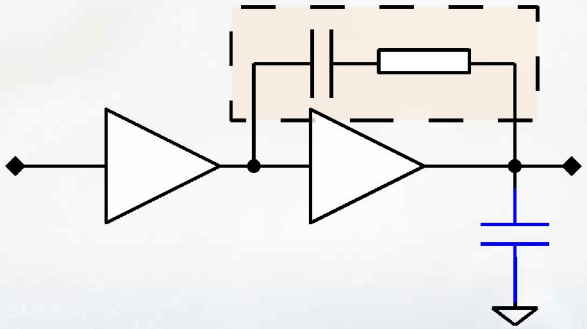
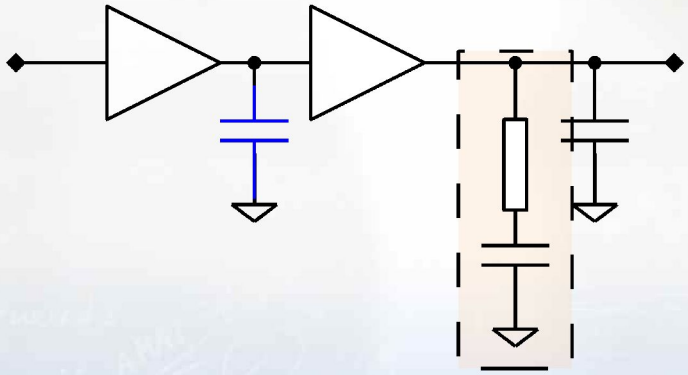
Typically: internal load dominates, and we should drive a resistive load

Miller-compensation, i.e., utilize the second-stage gain to multiply C_C

As always, some exceptions to the rule:

Nested compensation, active compensation, ... and more ...

Compensation compiled:

	Miller	Load compensation
Cap		
Cap + Res		

Rule-of-thumbs for hand-calculation

Use e.g. MATLAB to support calculations for understanding

```
/site/edu/es/ANTIK/antikLab/m/antikPoleZero.m
```

```
/site/edu/es/ANTIK/antikLab/m/antikSettling.m
```

In the end, use the simulator.

It has to be robust over temperature and other variations.

Hand calculations are incorrect per definition

Model corresponds quite well with circuit once you have identified the different stages

See for example exercises

What did we do today?

The most common amplifier stages

Frequency domain

Stability

Some top-level tips-and-tricks

What will we do next time?

More on amplifiers

Operational amplifiers

Differential amplifiers