Lecture 8, A/D D/A 1

Data converters 1

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What did we do last time?

Continuous-time filters

- Wrap-up and some more conclusions

Discrete-time filters

- Simulation of the continuous-time filters
- Discrete-time accumulators
- LDI transform
- Bilinear transform

What will we do today?

Data converters

- Fundamentals

DACs

- Overview

ADCs

- Overview

Oversampling converters

- Overview

Data converters fundamentals

DAC

Represents a digital signal with an analog signal
To control something
To transmit something (a modulated signal)

ADC

Represents an analog signal with a digital signal
To measure something
To receive something (a modulated signal)

And there are others:

Time-to-digital converters
Frequency-to-digital converters
etc.

Quantization process

If we ramp the input, the error is the deviation from a straight line

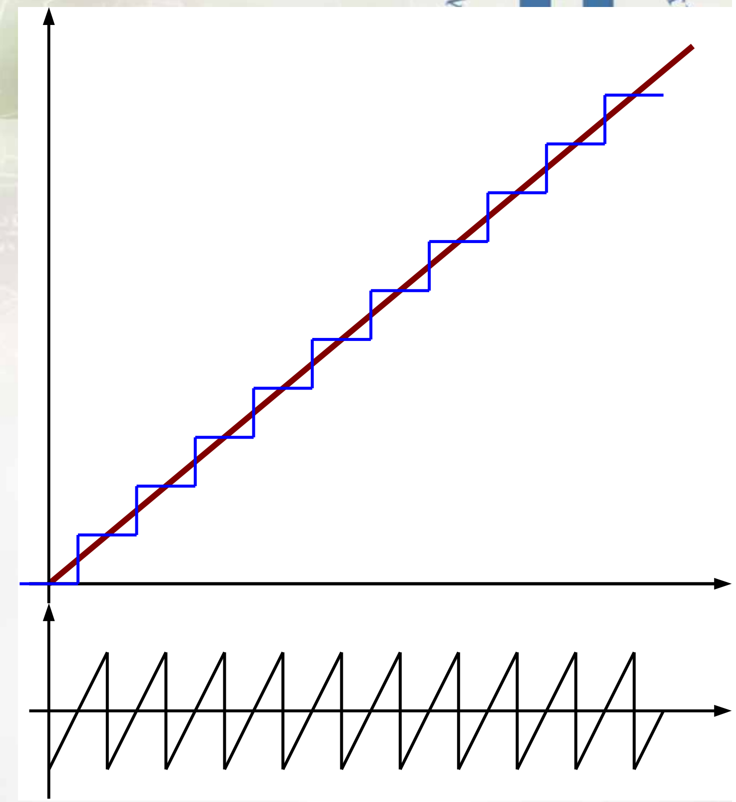
How is it defined for a DAC?

With the range 0 to V_{ref}, the stepsize is

$$\Delta = \frac{V_{ref}}{2^N}$$

The quantization error is bounded (within range)

$$Q \in \left\{ -\frac{\Delta}{2}, \frac{\Delta}{2} \right\}$$



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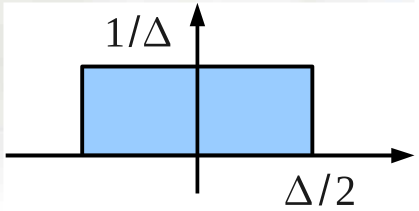
Quantization process, cont'd

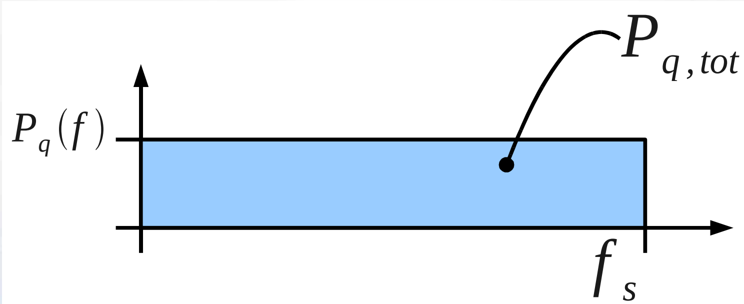
Assume signal-independent (not true for a low number of bits)



Quantization assumed to be a stochastic process and white noise, i.e., uniformly distributed in

$$\left[-\frac{\Delta}{2}, \frac{\Delta}{2}\right]$$

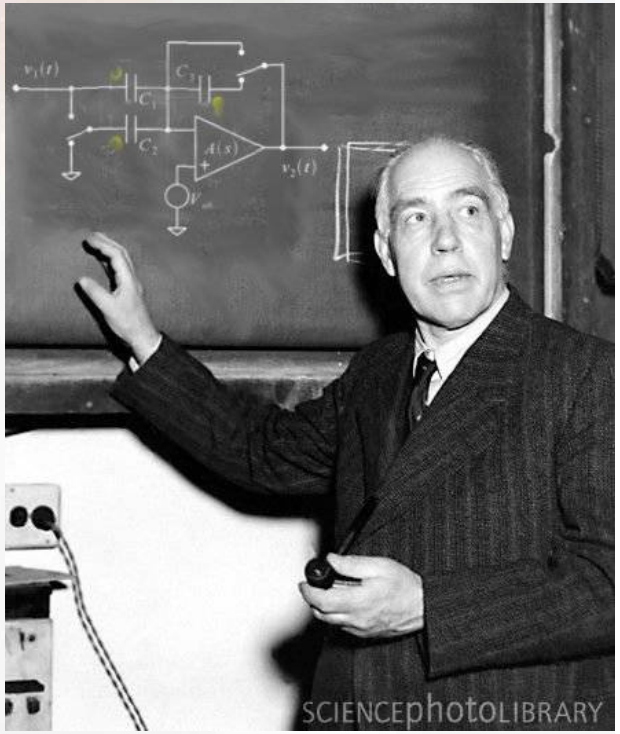
Noise power spectral density



White noise has constant spectral density

$$P_q(f) = \frac{\Delta^2}{12 \cdot f_s}$$

Quantization process, cont'd



Sigma of the probabilistic noise

Noise model

Remember the superfunction

Power spectral density

A certain bandwidth contains a certain amount of noise

Quantization process, cont'd

Peak power assuming centered around the nominal DC level

$$P_{pk} = \left(\frac{V_{ref}}{2} \right)^2$$

Maximum, average sinusoidal power

$$P_{avg} = \frac{1}{2} \cdot \left(\frac{V_{ref}}{2} \right)^2 = \frac{1}{8} \cdot V_{ref}^2 = \frac{P_{pk}}{2}$$

Peak-to-average ratio (PAR) for a sinusoid (crest factor)

$$\mathrm{PAR} = \frac{P_{pk}}{P_{avg}} = 2$$ (1.76 dB)

Quantization process, cont'd

Quantization noise power, signal-to-quantization-noise ratio

$$P_{q,tot} = \sigma^2 = \frac{\Delta^2}{12}$$ and $$\mathrm{SQNR} = \frac{P_{avg}}{P_{q,tot}} = \frac{P_{pk}}{P_{q,tot} \cdot \mathrm{PAR}}$$

$$\mathrm{SQNR} = \frac{\frac{1}{4} \cdot V_{ref}^2}{\frac{1}{12} \cdot \left(\frac{V_{ref}}{2^N} \right)^2 \cdot \mathrm{PAR}} = \frac{3 \cdot 2^{2N}}{\mathrm{PAR}}$$

Logarithmic scale

$$\mathrm{SQNR} \approx 6.02 \cdot N + 4.77 - \mathrm{PAR} = 6.02 \cdot N + 1.76$$ for our sinusoid.

D/A conversion as such

Amplitude given by scaled and summed digital bits

$$A_{out}(nT) = \sum_{k=0}^{N-1} w_k(nT) \cdot 2^k$$

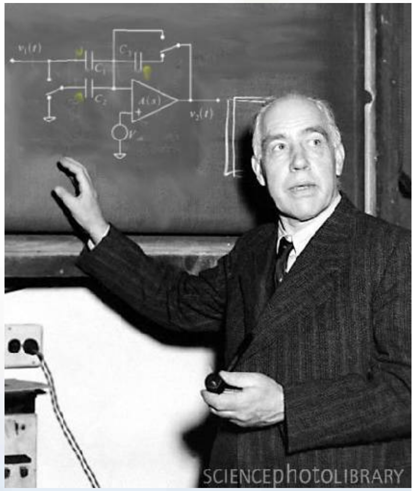
The scaling does not necessarily have to be binary:

Binary

Thermometer

Linear

Segmented



D/A conversion, cont'd

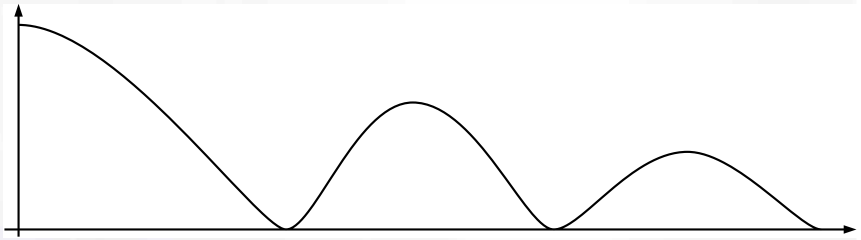
The output is a pulse-amplitude modulated signal (PAM)

$$A_{out}(t) = \sum a(nT) \cdot p(t - nT)$$

such that the spectrum is

$$A_{OUT}(j\omega) = A\left(e^{j\omega T}\right) \cdot P(j\omega)$$

Commonly, zero-order hold pulses are used as PAM (ideal reconstruction impossible)



Spectrum will be sinc weighted.

A reconstruction filter is needed to compensate!

D/A converter architectures

Current-steering

Summed weighted current sources.

Switched-capacitor (MDAC)

An SC gain circuit with weighted capacitors

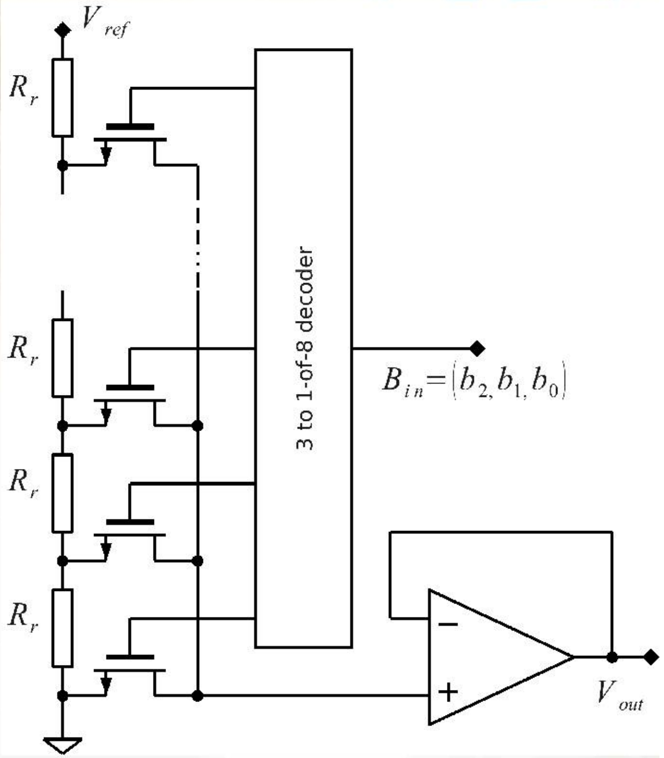
Resistor-string

Selects taps out of many and buffers

R-2R

Utilizes current dividers

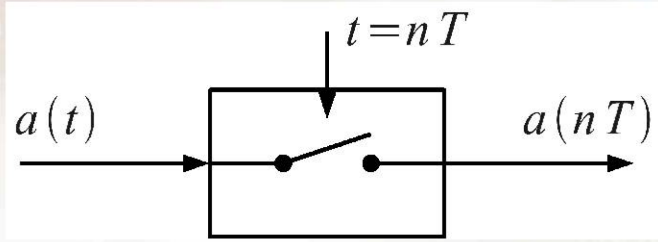
And many more



A/D conversion, sampling

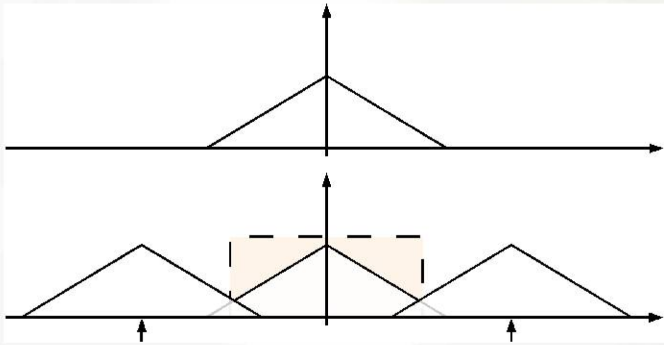
A/D conversion is a sampling process

$$a(nT) = a(t)\big|_{t=nT}$$



Poission's summation formula

$$A\left(e^{j\omega T}\right) = \sum A\left(j(\omega - 2\pi k)\cdot T\right)$$



Spectrum might repeat and overlap (folding)!

meet the sampling theorem (theoretically minimizes error)

use an anti-aliasing filter (practically minimizes error)

A/D conversion, sampling, cont'd

Tough filter requirements!

Practically, oversampling is required.

This will "separate" the repetitive spectra from each other and some filtering effort can also be moved to digital domain.

A/D conversion, mapping

Analog input is mapped to a digital code

A **range** of the signal input mapped to a unique (?) digital code

$$D(nT) = \sum_{k=0}^{N-1} w_k(nT) \cdot 2^k$$

Other formats

Thermometer, Gray, walking-one

A/D converter architectures

Flash

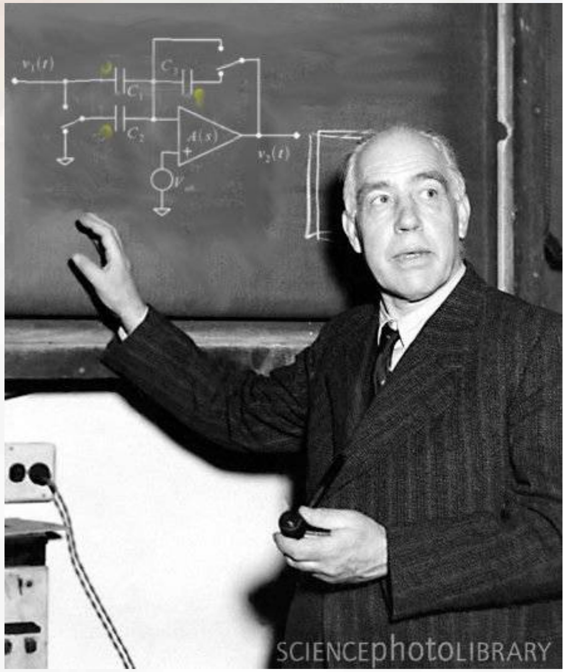
A set of comparator measures the input and compares it with a set of references.

Sub-ranging

Use a coarse stage to quantize the input. Subtract the input from the reconstructed, quantized result, amplify it and quantize again.

Pipelined

A set of sub-ranging ADCs



A/D converter architectures, cont'd

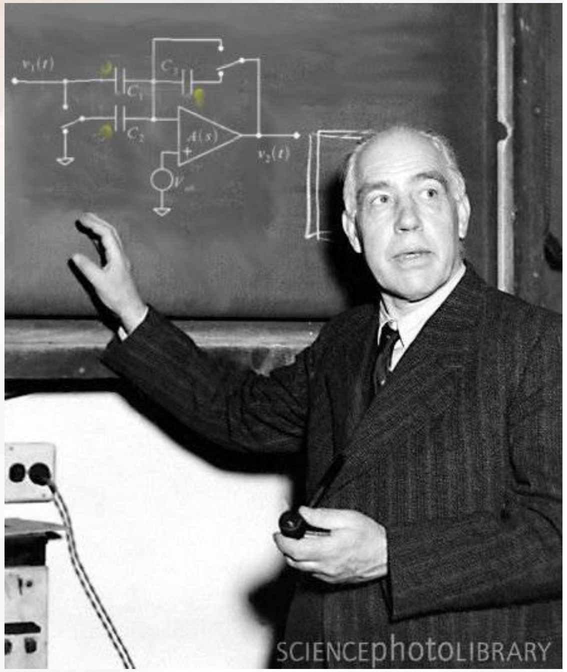
Successive approximation

One sub-ranging ADCs looping in time rather than a straight pipeline.

And plenty of others

Slope, dual-slope, folding, etc.

Oversampling ADCs later today



Data converter errors, DNL

Differential nonlinearity (DNL):
Deviations from the desired steps

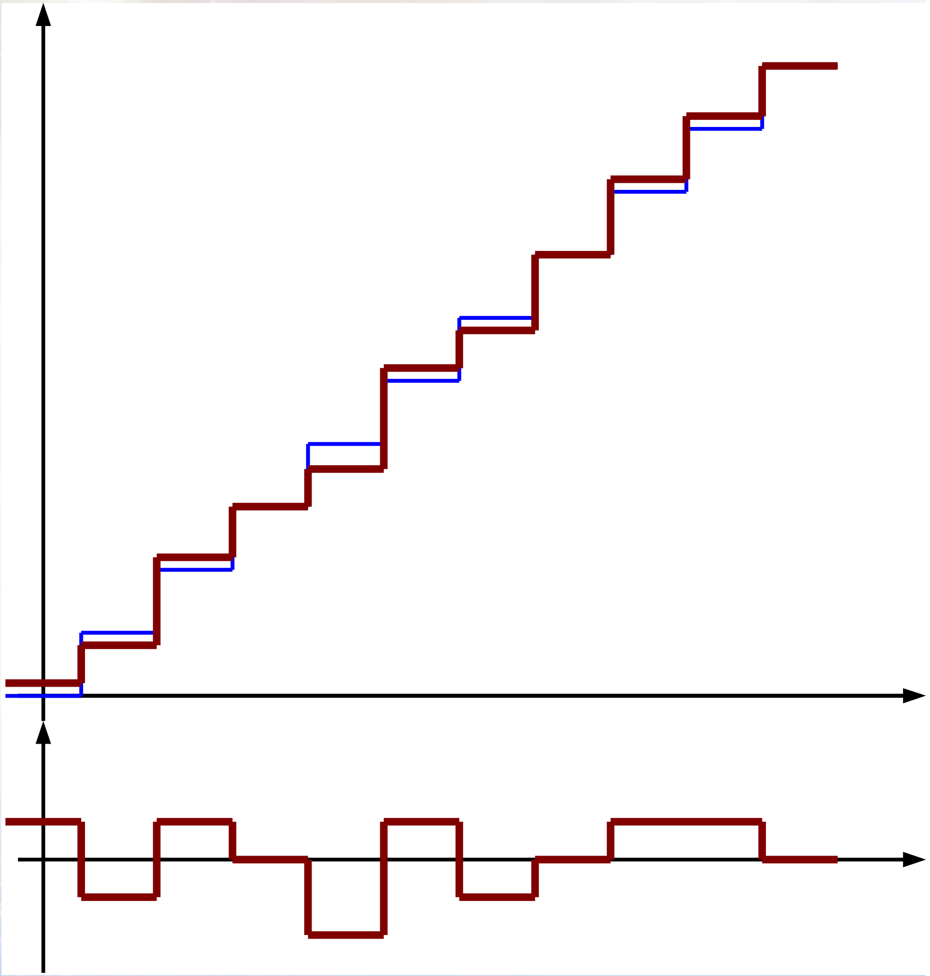
$$\mathrm{DNL}(n) = C_n - C_{n-1} - \Delta$$

$$\mathrm{DNL}(n) = \frac{C_n - C_{n-1}}{\Delta} - 1 \text{ [LSB]}$$

For full accuracy

$$|\mathrm{DNL}(n)| < 0.5 \text{ LSB} \quad \forall\, n$$

Often, the gain and offset errors are eliminated from the expression.



Data converter errors, INL

Integral nonlinearity is the deviation from the desired "line"

$$\mathrm{INL}(n) = C_n - n \cdot \Delta$$

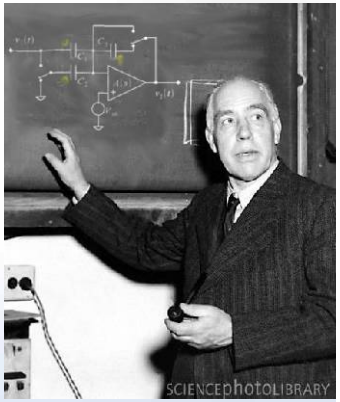
$$\mathrm{INL}(n) = \frac{C_n}{\Delta} - 1$$ [LSB]

For full accuracy

$$|\mathrm{INL}(n)| < 1 \text{ LSB} \quad \forall\, n$$

One can also show that the INL is the sum of the DNL

$$\mathrm{INL}(n) = \sum_{k=0}^{n} \mathrm{DNL}(k)$$



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Typical error measures

Static

INL, DNL, gain, offset

Dynamic (frequency and signal dependent)

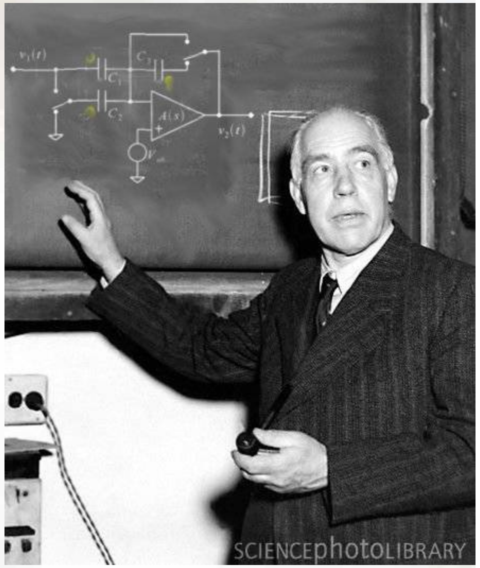
Spurious-free dynamic range, SFDR
Signal-to-noise-and-distortion ratio, SNDR
Intermodulation distortion, IMD

Resolution bandwidth, RBW

Effective number of bits, ENOB

Glitches, voltage/current spikes due to timing mismatch

Typical causes of static errors



Mismatch in reference levels

The effective resistor sizes or currents might vary due to mismatch

Offset in comparators

Any continuous-time amplifier/comparator has a signficant offset

Nonlinear effects due to unmatched biasing schemes

A power rail will introduce a gradient which will give a nonlinear transfer

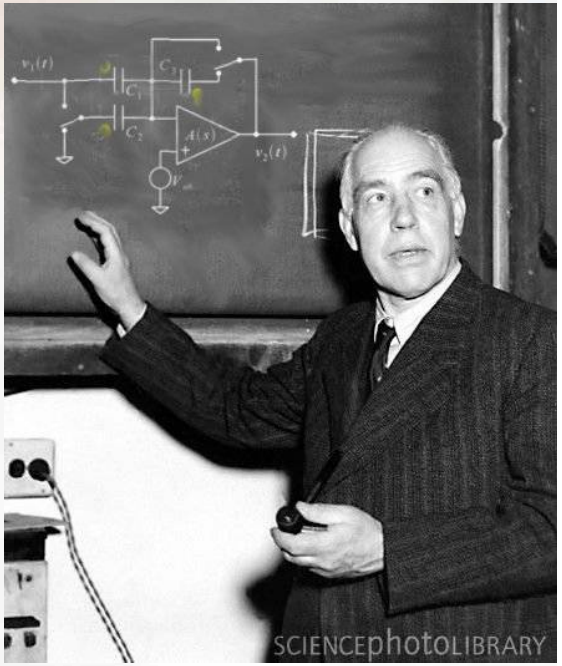
Some ways to circumvent the errors

Coding schemes in DACs

- Thermometer vs binary
- Effects with respect to mismatch
- A first glance at a scrambling technique

Digital error correction in pipelined ADCs

- Revisited another lecture

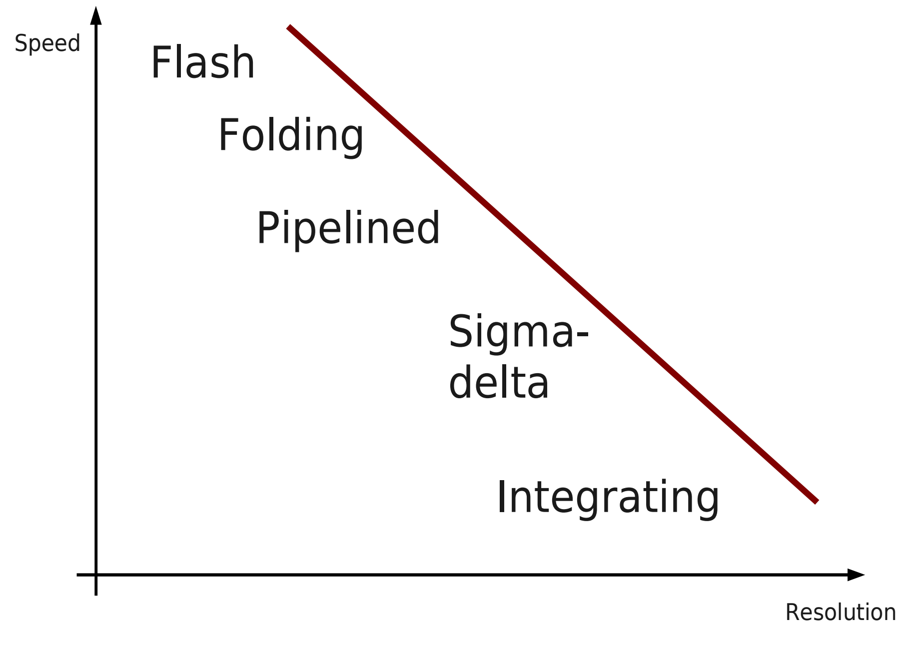


Converter trade-offs

Conversion speed vs resolution (accuracy)

Figure-of-merit, FOM

$$\mathrm{FOM} = \frac{4kT \cdot f_{bw} \cdot \mathrm{DR}}{P}$$



High-speed converters consumes a lot of power

High-resolution converters consumes large area

Attacking the filtering problem

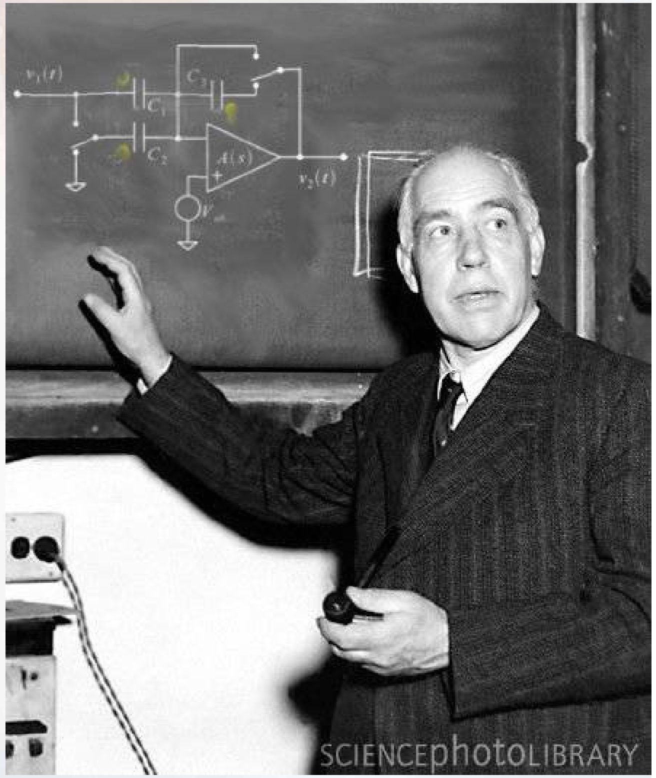
Ideal reconstruction and ideal sampling requires ideal filters

Increase your frequency range

- DAC: Interpolation and upsampling
- ADC: Decimation and downsampling

Drawbacks

- Higher power consumption
- More difficult to design (well, ...)



Notice that a DAC can never increase the number of bits!

Oversampling converters

Noise power over the entire Nyquist range:

$$\mathrm{SQNR} = 6.02 \cdot N + 1.76 \text{ [dB]}$$

With oversampling (anti-aliasing/reconstruction filter already there)

$$\mathrm{SQNR} = 6.02 \cdot N + 1.76 + 10 \cdot \log_{10} \frac{f_s}{2 \cdot f_{bw}} \text{ [dB]}$$

$$\mathrm{OSR} = \frac{f_s}{2 \cdot f_{bw}}$$

"For each doubling of the sample frequency, we gain 3 dB"

Oversampling converters

Assume we take a lower order converter to start with

$$\mathrm{ENOB} = \frac{\mathrm{SQNR} - 1.76}{6.02} = N + \frac{10 \cdot \log_{10} \mathrm{OSR}}{6.02}$$

16-bits: Use 12-bit converter, oversample 256 times

For some applications not an impossible scenario

16-bit: Use 1-bit converter, oversample 1073741824 times

1 Hz would require 1 GHz of sampling frequency ...

... there are more effective ways ...

Oversampling converters, cont'd

Since we reduce number of bits, spice it up a bit and "re-increase" complexity:

Create a converter that can also spectrally shape the new added noise

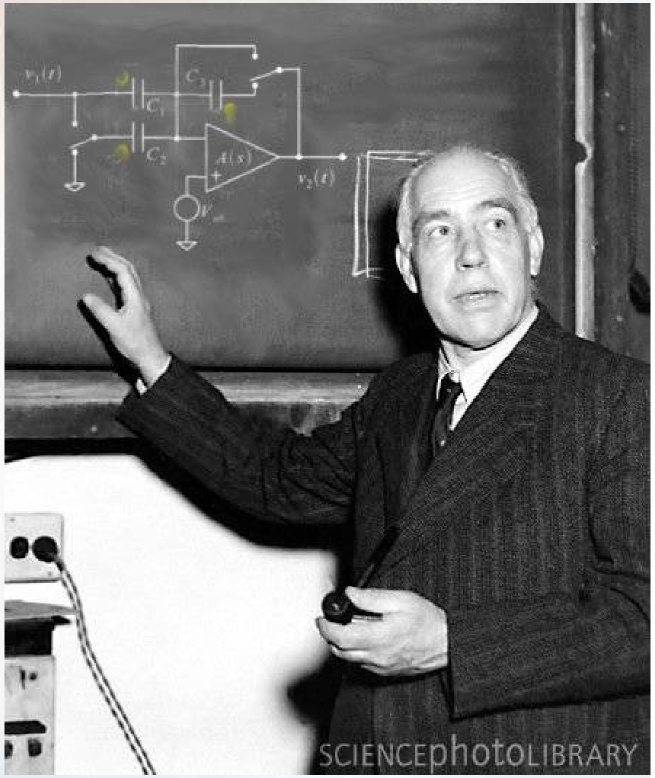
Sigma-delta modulation

HP/LP/BP-filters the added noise

Allpass filters the signal

Very much a filtering problem, but with nonlinear elements

Regulation loop!



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Sigma-delta converters, cont'd

$$Y = Q + A \cdot \underbrace{\left(X - B \cdot Y\right)}_{\epsilon} \Rightarrow Y = \frac{Q + A \cdot X}{1 + A \cdot B}$$

Noise and signal transfer functions, NTF/STF

$\mathrm{NTF}(z) = \frac{1}{1 + A \cdot B}$ and $\mathrm{STF}(z) = \frac{A}{1 + A \cdot B}$

If $A(z)$ is an integrator and $B(z) = 1$ is unity we get

$\mathrm{NTF}(z) = 1 - z^{-1}$, $\mathrm{STF}(z) = z^{-1}$

Order of the filters and oversampling determines the SQNR

$$\mathrm{SQNR} = 6.02 \cdot N + 1.76 + 10 \cdot (2 \cdot L + 1) \cdot \log_{10} \mathrm{OSR} - 10 \cdot \log_{10} \frac{\pi^{2L}}{2L + 1}$$

Sigma-delta converters, cont'd

First-order modulator and target 16 bits:

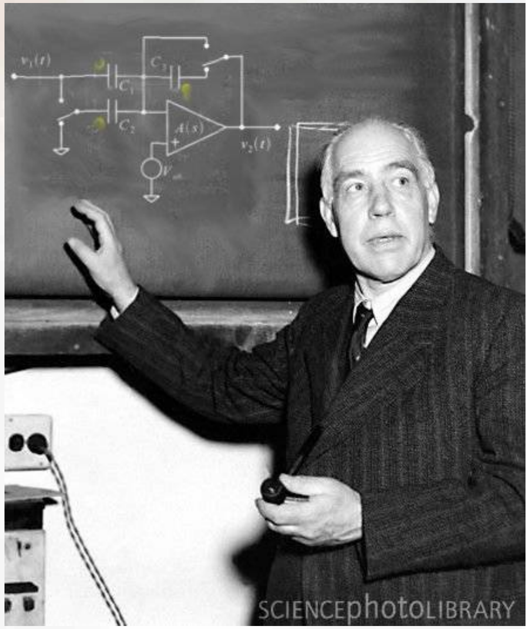
12 bits and oversample 16 times.
1 bit and oversample 1522 times (c.f. 1 G-times)

Second-order modulator and target 16 bits:

12-bits and oversample 6 times.
1-bits and oversample 116 times.

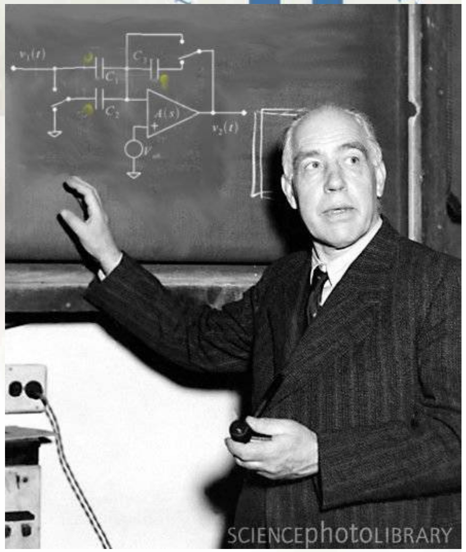
Third-order modulator and target 16 bits:

12 bits and oversample 5 times.
1 bits and oversample 40 times.



If too "aggressive", some of the momentum might be lost and filtering problem recreated.

Sigma-delta, audio example



Example:

16 bits (~100 dB)

22 kHz signal bandwidth

Target

As few bits (M) in the coarse quantizer as possible

Choose minimum possible modulator order (L)

Choose minimum possible sample frequency (fs) that maintains a simple analog anti-aliasing/reconstruction filter.

What configurations are possible?

Sigma-delta, audio example, cont'd

```
>> antikAudioSigmaDelta
SNR = 100.2442 dB, L = 2, M = 1, OSR = 128 fs = 5.632 MHz.
SNR = 115.2957 dB, L = 2, M = 1, OSR = 256 fs = 11.264 MHz.
SNR = 106.2642 dB, L = 2, M = 2, OSR = 128 fs = 5.632 MHz.
SNR = 112.2842 dB, L = 2, M = 3, OSR = 128 fs = 5.632 MHz.
SNR = 103.2527 dB, L = 2, M = 4, OSR = 64 fs = 2.816 MHz.
SNR = 112.8346 dB, L = 3, M = 1, OSR = 64 fs = 2.816 MHz.
SNR = 103.8025 dB, L = 3, M = 3, OSR = 32 fs = 1.408 MHz.
SNR = 109.8225 dB, L = 3, M = 4, OSR = 32 fs = 1.408 MHz.
```

What did we do today?

Data converters

Fundamentals

DACs and ADCs

Some outline of the architecture and properties

Oversampling converters

Basics and the trade-off between different parameters

What will we do the next time(s)?

DAC

Design example: the current-steering DAC

ADC

The comparator and its properties

Design example: the pipelined ADC

More circuit-level related stuff

Mainly switched-capacitor circuits