## Lecture 10, ANIK

## Data converters 2



## What did we do last time?

Data converter fundamentals
Quantization noise
Signal-to-noise ratio

ADC and DAC architectures
Overview, since literature is more useful explaining many, many different architectures

## What will we do today?

A quick glance at the pipelined ADC again

Sigma-delta modulators
Oversampling as such

Noise-shaping

Modulator structures

Wrap-up
Some comments on the course

## First - the subranging ADC - Basic operation

The converter "zooms" a range and converts the residue.
If flash is used as subconverter, there is only $2^{n}+2^{m}$ comparators


Another analog adder is required as well as a gain circuit, which limits the speed.

## Pipelined ADC in one picture

Multiple subranging ADC in series

A series of refinements, zoomins, of the convertible range


Assume same range in each stage


## Pipelined ADC - delays

Balance the delays and "cleverly" distribute the clock to avoid race


## Pipelined ADC - sensitive towards errors

Any misinterpreted level quickly diverges and never recovers!


Overlap can be digitally corrected (without training!)

## Pipelined ADC - error correction

Increase the number of stages and reduce overlap, i.e., decrease the scaling factor, $2^{n}$. Now, less likely to diverge and is able to recover.


More stages are required, but typically worth it

## Pipelined ADC - error correction cont'd

Trivial circuitry to retrieve the most likely code!


## Quantization noise revisited 1

Assume signal-independent (not true for a low number of bits)
Assume white noise, uniformly distributed in $\left\{-\frac{\Delta}{2}, \frac{\Delta}{2}\right\}$, with $\Delta=\frac{V_{r e f}}{2^{N}}$
Noise power spectral density (PSD)


## Quantization noise revisited 2 (quiz ...)

Noise power given by the sigma: $P_{q, t o t}=\sigma^{2}=\frac{\Delta^{2}}{12}$
Signal-to-quantization-noise ratio: $\mathrm{SQNR}=\frac{P_{a v g}}{P_{q, t o t}}=\frac{P_{p k}}{P_{q, t o t} \cdot \operatorname{PAR}}$
With values inserted

$$
\mathrm{SQNR}=\frac{\frac{1}{4} \cdot V_{r e f}^{2}}{\frac{1}{12} \cdot\left(\frac{V_{r e f}}{2^{N}}\right)^{2} \cdot \operatorname{PAR}}=\frac{3 \cdot 2^{2 N}}{\operatorname{PAR}}
$$

In logarithmic scale

$$
\mathrm{SQNR} \approx 6.02 \cdot N+4.77-\mathrm{PAR}=6.02 \cdot N+1.76 \text { for our sinusoid. }
$$

## Oversampling 1

Assume we have headroom to increase the sample frequency

Apply filtering to remove the excessive noise

We can effectively increase the performance! Or ... ?


## Oversampling converters

Noise power over the entire Nyquist range

$$
\mathrm{SQNR}=6.02 \cdot N+1.76[\mathrm{~dB}]
$$

Assume we oversample, or put it this way, we have a anti-aliasing/reconstruction filter there anyway. We get

$$
\mathrm{SQNR}=6.02 \cdot N+1.76+10 \cdot \log _{10} \frac{f_{s}}{2 \cdot f_{b w}}
$$

where the oversampling ratio is

$$
\mathrm{OSR}=\frac{f_{s}}{2 \cdot f_{b w}}
$$


"For each doubling of the sample frequency, we gain 3 dB "

## Oversampling converters

Assume we take a lower order converter to start with

$$
\mathrm{ENOB}=\frac{\mathrm{SQNR}-1.76}{6.02}=N+\frac{10 \cdot \log _{10} \mathrm{OSR}}{6.02}
$$

A 16-bit resolution can be obtained using a 12-bit converter if we oversample 256 times.

For some applications not an impossible scenario
A 16-bit resolution can be obtained using a 1-bit converter if we oversample 1073741824 times.

1 Hz would require 1 GHz of sampling frequency.

Luckily, there are more effective ways ...

## Attacking the filtering problem

Ideal reconstruction and ideal sampling requires ideal filters

Increase your frequency range
DAC: Interpolation and upsampling

ADC: Decimation and downsampling

Drawbacks
Higher power consumption


More difficult to design
FOM limit

## Digital implementation

Interpolation<br>Example<br>Decimation<br>Example



## Oversampling converters, cont'd

Since we are introducing another converter, and increasing the frequency - why not spice it a bit?

Create a converter that can also shape the new added noise

This can be done through sigma-delta modulation High-pass filters the added noise All-pass filters the signal

Designing a sigma-delta modulator is very much a filtering problem


Notice that a DAC can never increase the number of bits!

## Sigma-delta converters, cont'd

Consider the transfer function

$$
Y=Q+A \cdot \underbrace{(X-B \cdot Y)}_{\epsilon} \Rightarrow Y=\frac{Q+A \cdot X}{1+A \cdot B}
$$

Noise and signal transfer functions

$$
\mathrm{NTF}=\frac{1}{1+A \cdot B}, \mathrm{STF}=\frac{A}{1+A \cdot B}
$$

For example, $A$ is an integrator and $B$ is unity:

$$
\mathrm{NTF}=1-z^{-1}, \mathrm{STF}=z^{-1}
$$

Order of the filters and oversampling determines the SQNR. Ideally, we get:

$$
\mathrm{SQNR}=6.02 \cdot N+1.76+10 \cdot(2 \cdot L+1) \cdot \log _{10} \mathrm{OSR}-10 \cdot \log _{10} \frac{\pi^{2 \mathrm{~L}}}{2 L+1}
$$

## Sigma-delta converters, cont'd

First-order modulator. 16 -bit resolution can be obtained using a:
12-bit converter if we oversample 16 times
1-bit converter if we oversample 1522 times (c.f. 1G-times before)

Second-order modulator. 16-bit resolution ...
12-bit converter if we oversample 6 times.
1-bit converter if we oversample 116 times.

Third-order modulator. 16-bit resolution ...
12-bit converter if we oversample 5 times.
1-bit converter if we oversample 40 times.

Momentum slightly lost and filtering problem recreated!

## Sigma-delta, the audio example

## HIFI

16 bits, i.e., 100 dB
Signal bandwidth
22 kHz
Choose as few bits in coarse quantizer as possible

Choose minimum possible order

Choose minimum possible sample frequency


What configurations are possible?

## Sigma-delta, the audio example

Plugging the formula into MATLAB

$$
\mathrm{SQNR}=6.02 \cdot N+1.76+10 \cdot(2 \cdot L+1) \cdot \log _{10} \mathrm{OSR}-10 \cdot \log _{10} \frac{\pi^{2 \mathrm{~L}}}{2 L+1}
$$

gives us

```
>> antikAudioSigmaDelta
SNR = 100.2442 dB, L = 2, M = 1, OSR = 128 fs = 5.632 MHz.
SNR = 115.2957 dB, L = 2, M = 1, OSR = 256 fs = 11.264 MHz.
SNR = 106.2642 dB, L = 2, M = 2, OSR = 128 fs = 5.632 MHz.
SNR = 112.2842 dB, L = 2, M = 3, OSR = 128 fs = 5.632 MHz.
SNR = 103.2527 dB, L = 2, M = 4, OSR = 64 fs = 2.816 MHz.
SNR = 112.8346 dB, L = 3, M = 1, OSR = 64 fs = 2.816 MHz.
SNR = 103.8025 dB, L = 3, M = 3, OSR = 32 fs = 1.408 MHz.
SNR = 109.8225 dB, L = 3, M = 4, OSR = 32 fs = 1.408 MHz.
```


## What did we do today?

Sigma-delta modulators
Oversampling as such

Noise-shaping

Modulator structures

Wrap-up
Some comments on the course

## What will we do next time?

Exam ...

