Lesson 6

- Lesson Exercises: K9, K11, K12, K15, K16
- Recommended Exercises: K8, K13, K14, K17, K18, K23, B15.16

Theoretical Issues: Filter synthesis. Signal Flowchart. Integrators using Operational Amplifiers.

Theoretical

Filter Synthesis

Filter specification



Component values, R_n , L_n , C_n , and structure (Filter order, filter type, etc.) are chosen, using tables or computer tools. Naturally, several different methods can be used. Component values are denormalized with

$$R_{i,n} = R_0 \cdot R_{i,n}, L_i = \frac{R_0}{\omega_0} L_{i,n}, C_i = \frac{1}{\omega_0 R_0} C_{i,n}, \omega = \omega_0 \cdot \omega_0$$

Where R_0 is the load resistance. ω_0 is the pass band stop angluar frequency.

Continous-Time Filters

Consider the common transfer function for a linear system

$$H(s) = \frac{V_2(s)}{V_1(s)} = \frac{a_0 + a_1 s + \dots + a_{N-1} s^{N-1} + a_N s^N}{b_0 + b_1 s + \dots + b_{N-1} s^{N-1} + b_N s^N}$$

Suppose that the number of poles is equal to the number of zeros. This does not affect the following discussion. The transfer function can be described by a signal flow chart as in the figure below.



In the flow chart a number of amplifiers is identified, b_0 , a_0 ,

..., as well as summating integrators, 1/s.

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The $1/b_N$ coefficient can be eliminated in a number of different ways, i.e., be propagated forward or backward in the flow chart. The latter corresponds to the transformation of the transfer function as

$$H(s) = \frac{a_0 + a_1 s + \dots + a_N s^N}{b_0 + b_1 s + \dots + b_N s^N} = \frac{\frac{a_N}{b_N} \cdot s^N + \dots + \frac{a_0}{b_N}}{s^N + \dots + \frac{b_0}{b_N}} = \frac{a'_N \cdot s^N + \dots + a'_N}{s^N + \dots + b'_N}$$

Which is shown in the flow chart as



The negative coefficients, $-b_i$, are kept in the graph until the true coefficient values are known (simulations or tables). After that the flow chart may be transformed or relaxed further.

Scaling I

It will show that it is useful to be able to scale the signal level (or the peak value of the signal) at the output or input of each integrator. In a real implementation we want the integrators to work in their proper linear region. This helps the designer to estimate noise, distortion, bandwidth, etc. By introducing a scaling constant, k_i , to the input of each integrator or summation

node and a unscaling factor, $1/k_i$ at the output, the level at a certain node can be changed, and the transfer characteristics is still kept due to the linear behaviour of these kinds of circuits.



Leapfrog Filters

Consider a ladder fillter with impedances and admittances. Suppose the source has an inner (output) resistance of R_0 , and that the load is a terminating resistance of R_L .



Note that the structure of the ladder filter is dependent on N. If N is odd the load resistance is connected in parallel with Z_N . When N is even the load resistance is connected in series with

 Y_N . In the examples given below, N is chosen to be odd.

KCL and KVL result in a number of equations for the currents in the circuit

$$\begin{split} I_0 &= (E-V_1)/R_0, \, I_2 = Y_2(V_1-V_3), \, \dots, \\ I_{N-1} &= Y_{N-1}(V_{N-2}-V_N), \, I_{N+1} = V_N/R_L \end{split}$$

and analogously for the voltage

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$$V_1 = Z_1(I_0 - I_2), V_3 = Z_2(I_2 - I_4), \dots, V_N = Z_N(I_{N-1} - I_{N+1})$$

By introducing a normating constant (resistance), R, all equations can be rewritten as

$$RI_0 = \frac{R}{R_0}(E - V_1), RI_2 = RY_2(V_1 - V_3), \dots,$$

$$RI_{N-1} = RY_{N-1}(V_{N-2} - V_N), RI_{N+1} = \frac{R}{R_L}V_N$$

and

Ε

R/R

$$V_{1} = \frac{Z_{1}}{R}(RI_{0} - RI_{2}), V_{2} = \frac{Z_{2}}{R}(RI_{2} - RI_{4}), \dots,$$

$$V_{N} = \frac{Z_{N}}{R}(RI_{N-1} - RI_{N+1})$$

By introducing 'voltage nodes' (or variables);

$$RI_0, V_1, RI_2, V_3, \dots, V_N, RI_{N+1}$$

The equation system can be described with a signal flow chart. Compare the expressions for RI_0 and V_1 with the flow charts to the right. For the whole ladder filter this becomes



The flow chart describes a number of summating and amplifying elements. By introducing the sign of the nodes and eliminate all inverters and some small notation changes, the flow chart is transformed into



Note the change of sign of the voltage nodes and the amplifiers. If (N + 1)/2 is odd, the rightmost nodes (at the load of the ladder) are given by $-V_N$ and $-RI_{N+1}$ ($+V_{N-1}$, $+RI_{N-1}$ etc.). If (N + 1)/2 is even, the opposite is true.

Scaling II

Divide the net into a number of subnets. Every subnet will have a number of inputs and outputs. By scaling all the inputs with a factor k, all internal nodes of the subnet will be scaled with k as well. The outputs also have to be scaled by a factor 1/k to "reset".

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Ladder filters, contd.

Suppose that all $Z_i = 1/sC_i$ are kapacitances and all $Y_i = 1/sL_i$ are inductances. Example:



All amplifiers in the flow chart are now functioning as integrators (except those who are corresponding to the output resistance of the source and the load resistance).



Elliptic Leapfrog Filters

It is wanted to rewrite the signal flow grap so that only summating integrators are used. When synthesizing elliptic leapfrog filters the flow graph has to be slightly transformed. Consider the network below.



In the circuit we find the current I_2 ' through the inductor L_2 . The nodal equations are

$$V_1 = \frac{1}{sRC_1}(RI_0 - RI_2), V_3 = \frac{1}{sRC_3}(RI_2 - RI_4)$$

and

$$RI_{0} = \frac{R}{R_{i}}(V_{0} - V_{1}), RI_{2} = \frac{R}{\left(sL_{2} \parallel \frac{1}{sC_{2}}\right)}(V_{1} - V_{3}), RI_{4} = \frac{R}{R_{L}}V_{3}$$

The RI_2 expression is rewritten as

$$RI_2 = RI_2' + sRC_2(V_1 - V_3)$$
 and $RI_2' = \frac{R}{sL_2}(V_1 - V_3)$

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which gives the well-known expressions. By eliminating I_1 in the original equations, we have

$$V_{1} = \frac{1}{sRC_{1}}(RI_{0} - RI_{2}' - sRC_{2}(V_{1} - V_{3})) \text{ and}$$
$$V_{3} = \frac{1}{sRC_{2}}(RI_{2}' + sRC_{2}(V_{1} - V_{3}) - RI_{2})$$

which gives

$$V_1 = \frac{1}{sR(C_1 + C_2)}(RI_0 - RI_2') + a_{12}V_3 \text{ and}$$

$$V_3 = \frac{1}{sR(C_2 + C_3)}(RI_2' - RI_4) + a_{23}V_1$$

The constants a_{12} and a_{23} are given by

$$a_{12} = \frac{C_2}{C_1 + C_2}$$
 and $a_{23} = \frac{C_2}{C_2 + C_3}$

This is equivalent to the circuit below. An extra pair of voltage sources is used.



In the signal flow chart this is easily rewritten as



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Integrators with Operational Amplifiers

Consider a common set up consisting of an operational amplifier and a number of impedances. Suppose that the operational amplifier is ideal, hence infinite high input impedance. With KCL we have

 $\frac{V_0}{Z_0} = -\left(\frac{V_1}{Z_1} + \frac{V_2}{Z_2} + \dots + \frac{V_N}{Z_N}\right)$

which gives the voltage at the output to

$$V_0 = -\frac{Z_0}{Z_1}V_1 - \frac{Z_0}{Z_2}V_2 - \dots - \frac{Z_0}{Z_N}V_N$$

Suppose that among the impedances, Z_0 is a capacitance and the others are chosen to be resistances. This gives

$$V_0 = -\frac{1}{sR_1C_0}V_1 - \frac{1}{sR_2C_0}V_2 - \dots - \frac{1}{sR_NC_0}V_N$$

By varying R_i and C_0 we have an inverting, summating (and scaling) integrating link. A noninverting integrator is achieved by cascading the integrator with an additional invering buffer.



Transistors as resistors (MOSFET-C filter)

The resistance of a transistor in the linear region can be written as

$$R = \frac{1}{\mu_0 C_{ox} (W/L) (V_G - V_T - V_D)}$$

By changing size and control voltage, the resistance value is changed. Note that the resistance is signal dependent.

Exercises

Exercise K9

GIC - Generalized impedance converter.

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The gic can be used to realize on-chip inductances. However, the circuit is area consuming and there are some other drawbacks.

Derive the *K*-matrix

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} V_2 \\ -I_2 \end{bmatrix}$$



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where

$$A = \frac{V_1}{V_2}\Big|_{-I_2 = 0}, B = \frac{V_1}{-I_2}\Big|_{V_2 = 0}, C = \frac{I_1}{V_2}\Big|_{-I_2 = 0}, D = \frac{I_1}{-I_2}\Big|_{V_2 = 0}$$

(If N links with K-matrix K_i are cascaded, the total system can be described by the matrix product $K_{TOT} = K_1 K_2 \dots K_N$.)

Assume that the OPamps are ideal. This implies that the voltage over the input must be zero. This forces the potential in V_r to be equal to V_1 and V_2 , and further $V_1 = V_2$. With KCL, and denoting the currents through Z_2 and Z_3 with I_{Z2} and I_{Z3} , respectively, we have:

$$V_1 - I_1 Z_1 - I_{Z2} Z_2 = V_x = V_1$$
 which gives $I_{Z2} = -I_1 Z_1 / Z_2$
 $V_2 - I_2 Z_4 - I_{Z3} Z_3 = V_x = V_2$ which gives $I_{Z3} = -I_2 Z_4 / Z_3$

Due to the infinite input impedance, there can be no current flowing into the OPamps, and:

$$I_{Z2} = -I_{Z3}$$
 which gives $-I_1Z_1/Z_2 = I_2Z_4/Z_3$, or $I_1 = -I_2\frac{Z_2Z_4}{Z_1Z_3}$

From this we get

$$A = 1, B = 0, C = 0, D = \frac{Z_2 Z_4}{Z_1 Z_3}$$

If an impedance, Z, is terminating port two, the relation between output current and voltage is given by

$$V_{2} = -I_{2}Z$$

Equations $V_{1} = V_{2}$ and $I_{1} = \frac{Z_{2}Z_{4}}{Z_{1}Z_{3}} \cdot \frac{V_{2}}{Z}$ give
$$Z_{in} = \frac{V_{1}}{I_{1}} = \frac{V_{2}}{\frac{Z_{2}Z_{4}}{Z_{1}Z_{3}} \cdot \frac{V_{2}}{Z}} = Z\frac{Z_{1}Z_{3}}{Z_{2}Z_{4}}$$

Suppose

we have

$$Z_{in} = sCR^2 = sL$$

which simulates an inductor.

Exercise Extra

Find a signal flow chart which describes a 4th order leapfrog filter. Or generally, an even order leapfrog filter.

Exercise K11

Realize the filter having the transfer function

$$H(s) = \frac{1 \times 10^{\circ}}{s^2 + 3 \times 10^5 \cdot s + 6 \times 10^6}$$

We rewrite the function as

$$Y(s) \cdot [s^2 + 3 \times 10^5 \cdot s + 6 \times 10^6] = 1 \times 10^6 \cdot X(s)$$

Or

$$Y(s) = -\frac{3 \times 10^5}{s} Y(s) - \frac{6 \times 10^6}{s^2} Y(s) + \frac{1 \times 10^6}{s^2} X(s)$$

The flow graph is transformed. $A = -6 \times 10^6$,

 $B = -3 \times 10^5$ and $D = -1 \times 10^6$. Note the insertion of the inverter. This can now be used to implement the active filter.

(Note that there is no inversion included in the active RC filter implementation). Now the component values have to be determined. Assume all capacitances to be equal. We can see that the – intermediate node can be written as



B

$$V_M = \frac{A}{s} \cdot Y(s) + \frac{D}{s} \cdot X(s)$$

Identifying this from the active implementation, we have

$$V_M = -\frac{1}{sR_AC} \cdot Y(s) - \frac{1}{sR_CC} \cdot X(s)$$

This gives

$$A = -\frac{1}{R_A C} = -6 \times 10^6$$
 and $D = -\frac{1}{R_D C} = -1 \times 10^6$

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We also see that the output can be written as

$$Y(s) = \frac{1}{s} \cdot V_M + \frac{B}{s} \cdot X(s)$$

Identifying this from the active implementation, we have

$$B = -\frac{1}{R_B C} = -3 \times 10^5$$

We also see that the implementation above is impossible. The intermediate node V_M is **not** transformed correctly. In fact, we have to inverse the voltage with a buffer.



We do some notations. The structure could be changed by letting A be positive using an inverting buffer on the output signal instead. This decreases the number of opamps with one. We thereby also conclude that we do not find the simplest structure by forcing all input arguments to the summation nodes to be negative. We also see that we can use the inverting buffers to scale signal levels and relaxing the size on Z. There are numerous way to implement the filter. One can also soon realize that R_A , R_D and Z can dependently be scaled and still maintain true transfer function, see next exercise.

Exercise K12

Realize the filter having the transfer function

$$H(s) = \frac{-1 \times 10^{6} (s-1)}{s^{2} + 3 \times 10^{5} \cdot s + 6 \times 10^{6}}$$

The function is rewritten in the same manner as in the previous exercise. In this case we however have a slightly different structure. We assume that we feed back the positive output (constant A) and we construct with a negative intermediate node, $-V_M$:

$$Y(s) = -\frac{3 \times 10^5}{s} Y(s) - \frac{6 \times 10^6}{s^2} Y(s) - \frac{1 \times 10^6}{s} X(s) + \frac{1 \times 10^6}{s^2} X(s)$$

With

$$A = 6 \times 10^{6}, B = -3 \times 10^{5}, D = 1 \times 10^{6} \text{ and } E = -1 \times 10^{6}$$

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Lesson 6

The active filter structure becomes

If we now directly set up the transfer function for the active filter implementation, we have

$$-V_{M} = -\frac{1}{sCR_{D}} \cdot X + \frac{1}{sCR_{A1}} \cdot \frac{R_{A2}}{R_{A3}} \cdot Y$$

$$Y = -\frac{1}{sCR}(-V_{M}) - \frac{1}{sCR_{E}}X - \frac{1}{sCR_{B}}Y$$

$$= -\frac{1}{sCR}(-V_{M}) - \frac{1}{sCR_{E}}X - \frac{1}{sCR_{B}}Y$$

which gives

$$Y = -\frac{1}{sCR_{B}}Y - \frac{1}{s^{2}C^{2}R_{A1}R} \cdot \frac{R_{A2}}{R_{A3}} \cdot Y - \frac{1}{sCR_{E}}X + \frac{1}{s^{2}C^{2}RR_{D}}X$$

We now identify the terms

$$\frac{1}{R_BC} = 3 \times 10^5, \frac{1}{C^2 R_{A1} R} \cdot \frac{R_{A2}}{R_{A3}} = 6 \times 10^6, \frac{1}{C R_E} = 1 \times 10^6, \frac{1}{C^2 R R_D} = 1 \times 10^6$$

Suppose $C = 1 \mu$ F, and $R_{A2} = R_{A3}$. Then

$$R_B = \frac{10}{3}, R \cdot R_{A1} = \frac{1 \times 10^6}{6}, R_E = 1, R \cdot R_D = 1 \times 10^6$$

Choose $R_{A1} = 1000$ which gives $R_{A1} = \frac{1000}{6}$ and $R_D = 1000$

Exercise K15

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Pass Band: 0 < f < 3.5 kHz and $A_{max} = 1$ dB Stop Band f > 10 kHz and $A_{min} = 20$ dB Passive Butterworthfilter, order is found in table to be N = 3. We choose a voltage driven π -net with reflection r = 1 for symmetry. Resistances are chosen to be $R = R_{\pi} = R_{\pi} = 1k\Omega$

$$R_i = R_L = R_0 = 1k\Omega$$

Component values are found in table to be:

$$C_{3n} \, = \, 1 \, , \, L_{2n} \, = \, 2 \ \, {\rm and} \ \, C_{1n} \, = \, 1 \,$$

These values are denormalized according table to

$$C = \frac{C_n}{\omega_0 R_0}, L = \frac{R_0 L_n}{\omega_0}, \text{ with } \omega_0 = \omega_c \varepsilon^{-1/N} = \omega_c [\sqrt{10^{0.1A_{max}} - 1}]^{-1/N} \approx 27.55 \text{ krad/s}.$$

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 ω_{c}

 ω_{s}

ω

$$C_1 = C_3 = 36.3nF$$
 and $L_2 = 72.6mH$

A number of filter components have been found. Create a signal flow chart for the circuit. The nodal voltages for the circuit is found to be (normalized with R):

$$\begin{split} I_0 &= \frac{E - V_1}{R_i} & RI_0 &= \frac{R}{R_i} (E - V_1) \\ V_1 &= \frac{1}{sC_1} (I_0 - I_2) & V_1 &= \frac{1}{sC_1R} (RI_0 - RI_2) \\ I_2 &= \frac{V_1 - V_3}{sL_2} & RI_2 &= \frac{R}{sL_2} (V_1 - V_3) \\ V_3 &= \frac{1}{sC_3} (I_2 - I_4) & V_3 &= \frac{1}{sRC_3} (RI_2 - RI_4) \\ I_4 &= \frac{V_3}{R_L} & RI_4 &= \frac{R}{R_L} V_3 \end{split}$$

From these equations we find:



Modify the graph by propagating the inverters and denote negative voltage nodes:



We now have a number of integrators, $K\frac{1}{s}$. Realized with operational amplifiers we have a structure according to

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We now have to determine the component values for this realization, This is done by comparing the signal flow chart with the OPamp net:

Now we have several equations. Choose all capacitors to be equally large, maybe:

$$C_4 = C_5 = C_6 = 30 nF$$

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The values are chosen to be approximately equal to those found in the ladder filter realization, which would give reasonable resistance values. From the equations we also find:

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$$R_4 = R_5 = \frac{C_1 R_i}{C_4} = \frac{36.3nF \cdot 1k\Omega}{30nF} = 1.21k\Omega \text{ och } R_{10} = \frac{C_3 R_L}{C_6} = 1.21k\Omega$$

And this also gives

$$R_6 = R_9 = \frac{C_1 R}{C_4}$$
 and $R_7 = R_8 = \frac{L_2}{C_5 R}$

For symmetry, $R_6 = R_7 = R_8 = R_9$ are chosen to be equal, which gives:

$$R^{2} = \frac{L_{2}C_{4}}{C_{1}C_{5}} \Rightarrow R = \sqrt{L_{2}/C_{1}} = 1000\sqrt{72.6/36.3} \approx 1.41k\Omega$$

Finally, we have

$$R_6 = R_7 = R_8 = R_9 = 1.21 \cdot 1.41 k\Omega \approx 1.71 k\Omega$$

The final value that has to be determined is the resistor value used in the invering buffer, r. Choose r to be equal to anyone of the other resistances, i.e., :

 $r = R_6 = 1.71 k \Omega.$

Exercise K16

Synthesize an active elliptic leapfrog filter. Termination resistances are $1k\Omega$. Specification gives:

Pass band: $0 < \omega < 2\pi$ krad/s, $A_{max} = 0.1$ dB

Stop band:
$$\omega > 4\pi \text{ krad/s}, A_{min} > 20 \text{ dB}$$

Order is found with table to be N = 3.

This gives following filter structure. Component values are found to be



Denormalized values are given by

$$C = \frac{C_n}{\omega_0 R_0}$$
 and $L = \frac{R_0}{\omega_0} L_n$ give $C_1 = C_3 \approx 139.1 nF$, $C_2 \approx 38.4 nF$, $L_2 \approx 144.6 mH$

Set up the equations:

$$I_{0} = \frac{E - V_{1}}{R_{i}} \qquad RI_{0} = \frac{R}{R_{i}}(E - V_{1})$$

$$V_{1} = \frac{1}{sC_{1}}(I_{0} - I_{2}) \qquad V_{1} = \frac{1}{sRC_{1}}(RI_{0} - RI_{2})$$

$$I_{2} = \frac{1}{L_{2} || C_{2}}(V_{1} - V_{3}) \qquad RI_{2} = \frac{R}{sL_{2}/(1 + s^{2}L_{2}C_{2})}(V_{1} - V_{3})$$

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R;

 L_2

 C_2+C_2

 C_1+C_2

R

$$V_{3} = \frac{1}{sC_{3}}(I_{2} - I_{4}) \qquad V_{3} = \frac{1}{sRC_{3}}(RI_{2} - RI_{4})$$
$$I_{4} = \frac{V_{3}}{R_{L}} \qquad RI_{4} = \frac{R}{R_{L}}V_{3}$$

Introuduce a current, I_2 , through the inductor. The equations are modified:

$$RI_2 = RI_2' + sRC_2(V_1 - V_3)$$
 and $RI_2' = \frac{R}{sL_2}(V_1 - V_3)$

The RI_2 expression can be eliminated, and gives:

$$V_{1} = \frac{1}{sRC_{1}}(RI_{0} - RI_{2}' - sRC_{2}(V_{1} - V_{3})) \Rightarrow$$
$$V_{1} = \frac{1}{sR(C_{1} + C_{2})}(RI_{0} - RI_{2}') + \frac{C_{2}}{C_{1} + C_{2}}V_{3}$$

And correspondingly

$$V_3 = \frac{1}{sR(C_2 + C_3)}(RI_2' - RI_4) + \frac{C_2}{C_2 + C_3}V_1$$

This gives the structure with a pair of "helping" voltage sources. The equations are written as:

$$RI_{0} = \frac{R}{R_{i}}(E - V_{1})$$

$$V_{1} = \frac{1}{sR(C_{1} + C_{2})}(RI_{0} - RI_{2}') + \frac{C_{2}}{C_{1} + C_{2}}V_{3}$$

$$RI_{2}' = \frac{R}{sL_{2}}(V_{1} - V_{3})$$

$$V_{3} = \frac{1}{sR(C_{2} + C_{3})}(RI_{2}' - RI_{4}) + \frac{C_{2}}{C_{2} + C_{3}}V_{1}$$

$$RI_{4} = \frac{R}{R_{L}}V_{3}$$

The signal flow chart is given by



Realization

The a_{ij} terms can be realized by using capacitors instead of resistances. This realizes a negative and scaled signal flow.



Component values are found using the same manner as for the previous exercise. The resistances can be implemented by using transistors.

Lesson 8

Lesson Exercises:	K27, K28, K36, K37, K38	

Recommended Exercises: K24, K25, K26, K30, K39, B10.1-5

Theoretical Issues: SC-filter, Laddningsanalys

Theoretical

Switched-Capacitor Circuit Technique, SC

The advantages of not having to implement on-chip resistances are several. In the previous lesson we saw that the resistance implemented with a transistor is signal dependent. There are certain processes allowing special poly layers to implement resistors. There are however problems with matching and parasitic capacitances. The SC technique utilizes the fact that capacitor ratios are used. Then we only need to match capacitors.

To know all the principles of the SC technique, we have to consider the charge redistributiuon that occurs in the circuits.

Charge redistribution analysis

Consider a capacitor. The charge is equal to the voltage over the plates times the capacitance value (constant):

Q = CV

By noting the amount of charge that is transferred between different capacitor plates, a flow chart for the charge (and thereby voltages) can be constructed. By only allowing the charge to move at certain time intervals, at discrete-time points, we can control the behaviour of the circuit.

Equivalent Resistance

Consider the capacitance and the switch at time t. The charge on the top plate is equal to

 $q(t) = C \cdot v_1(t)$

A certain amount of charge will flow from the input to the top plate.

$$\Delta q(t) = q(t) - q(t - \tau) = C[v_1(t) - v_2(t - \tau)]$$

At time $t + \tau$ the charge is given by

 $q(t+\tau) = C \cdot v_2(t+\tau)$

The charge floating from the output to the top plate is given by

$$\Delta q(t+\tau) = C[v_2(t+\tau) - v_1(t)]$$

From this we conclude that during a clock period, T, a certain charge, Δq , will flow from v_1

to v_2 . This charge must equal $\Delta q = C \cdot (V_1 - V_2)$ the capacitance and change of voltage between the terminals. If there is no difference, no charge will be transferred, etc. The average current, $I = q \cdot T$, gives

$$V_1 - V_2 = \frac{T}{C} \cdot I$$
 which gives the equivalent resistance $R \equiv \frac{T}{C}$

Parasitic capacitances

We can associate a parasitic capacitance with all terminals of the transistor, source, drain, gate, and bulk:

$$C_{gd}, C_{gs}, C_{ds}, C_{db}$$
 and C_{sd}

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The switching signal is considered to be ac grounded and C_{gd} is coupled in parallel with C_{db} , as well as C_{gs} with C_{sb} .

In most cases the influence of C_{ds} is neglected, due to its low value. When the switch is conducting, C_{ds} is also considered to be replaced

when the switch is conducting, C_{ds} is also considered to be replace with a short.





By noting these parasitics their influence on the total transfer function can be analyzed.

Discrete-time Spectrum

The discrete-time signal can be written as

$$y(t) = \sum_{k=0}^{\infty} y(kT)[u(t-kT) - u(t-(k+1)T)]$$

where T is the clock period. The output spectrum can be written as

 $Y(\omega) = \operatorname{sinc}(\omega T) \cdot Y[\omega T]$

Tips for charge redistribution

Charge can not disappear fron an unconnected plate

On a voltage controlled operational amplifier it is only the output that can add or remove charge. The input is coupled to transistor gates, wherein no current can flow.

The charge disappears from the capacticance if both plates are connected to the same potential (short cut).

The charge redistribution is done in discrete events

If a capacitance is switched to a charged capacitance net, the charge will move and eventually reach equilibrium. By using the tips above and use the knowledge of how the charge is stored from one event to another, the transfer function can be derived.

Example Charge I (K25)

Derive the transfer function and discuss the sensitivity of the circuit. Values are

$$C_1 = C_2$$
 and $C_1 = 1.12C_2$

Consider the start-up conditions at time *t*. The charge at C_1 and C_2 is

$$q_1(t) = 0$$
 and $q_2(t) = C_2 v_2(t)$

 C_1 is coupled between ground and virtual ground (OPamp input). The charge must be zero.

Time $t + \tau$. Switches have changed.

 C_1 is charged by the voltage $v_1(t + \tau)$ and the output of the OPamp, v_2 , that adds extra charge. The charge at C_1 becomes

$$q_1(t+\tau) = C_1[v_1(t+\tau) - v_2(t+\tau)]$$

Note the chosen sign of the charge. For C_2 we have

$$q_2(t+\tau) = C_2 v_2(t+\tau).$$

On the negative plate, the charge is stored.

$$q_2(t+\tau) = q_2(t) \text{ dvs } v_2(t+\tau) = v_2(t)$$

(No charge can disappear from the input of the OPamp if it is unconnected).

At time $t + 2\tau$ the switches are closed. C_1 is again connected to ground and virtual ground, which empties C_1 . The positive charge leaks down to ground, the negative charge is redistributed to the negative plate of C_2 . The extra charge needed to compensate the positive plate of C_2 is taken from the OPamp output.

The charge at C_1 and C_2 must be

$$q_1(t+2\tau) = 0$$
 and $q_2(t+2\tau) = C_2v_2(t+2\tau)$

Charge conservation gives (at the negative plate of C_2)

$$-q_2(t+2\tau) = -q_2(t+\tau) + (-q_1(t+\tau)) = -q_2(t) - q_1(t+\tau)$$

This gives

$$C_2 v_2(t+2\tau) = C_2 v_2(t) + C_1 [v_1(t+\tau) - v_2(t+\tau)] =$$

$$= C_2 v_2(t+\tau) + C_1 [v_1(t+\tau) - v_2(t+\tau)]$$

We also see that





 $v_2(t+2\tau) = v_2(t+3\tau)$

which gives

$$C_2 v_2(t+3\tau) - C_2 v_2(t+\tau) + C_1 v_2(t+\tau) = C_1 v_1(t+\tau)$$

z-transform, with t = kT and $2\tau = T$

$$C_2 z^{3/2} - C_2 z^{1/2} + C_1 z^{1/2}] V_2(z) = C_1 z^{1/2} V_1(z)$$

which gives the transfer function

$$H(z) = \frac{V_2(z)}{V_1(z)} = \frac{C_1}{C_2} \cdot \frac{z^{1/2}}{z^{3/2} - (1 - C_1/C_2)} = \frac{C_1}{C_2} \cdot \frac{1}{z - (1 - C_1/C_2)}$$

If the capacitances are equally large, $C_1 = C_2$, the circuit is a simple delay element, (sampleand-hold)

$$H(z) = z^{-1}$$

In the second case, $C_1 = 1.12C_2$, the transfer function becomes

$$H(z) = \frac{1.12}{z + 0.12}$$

This is used to compensate for the sinc weighting of the signal.

Example parasitics I



The parasitic capacitances are associated with all nodes in the circuit. Consider the parasitic capacitances, C_a through C_h . They are the parasitic capacitances associated with the switches as discussed earlier.

During clock phase ϕ_2 , C_b , C_c and C_d are coupled in parallel. The same is true for C_f , C_g and C_h . C_a is connected to the output of the OPamp. C_e is connected to the input signal. The previous charge at the capacitances coupled in parallel will redistribute to C_2 .

During clock phase ϕ_1 , C_a , C_b and C_c are coupled in parallel. The same is true for C_e , C_f and C_g . C_d is coupled to virtual ground at the OPamp input. C_h is connected to ground. The parallel capacitances will be charged and during next clock phase this charge redistribute and affect the transfer function.

Note that C_h and C_d always are connected to ground or virtual ground and will therefore not affect the transfer function. While the input signal is directly connected to C_1 the capacitances

C_e, C_f, C_g, C_h will not affect the transfer function.

Example Charge II (K26)

Consider time t. Charge at C_1 and C_2 is

$$q_1(t) = C_1 v_2(t)$$
 and $q_2(t) = C_2 v_2(t)$

At
$$t + \tau C_1$$
 is charged with $v_1(t)$

$$q_1(t+\tau) = C_1 v_1(t+\tau)$$

 C_2 conserves its charge

$$q_2(t) = C_2 v_2(t) = q_2(t+\tau) = C_2 v_2(t+\tau)$$

At time $t + 2\tau C_1$ is switched

$$q_1(t+2\tau) = C_1 v_2(t+2\tau)$$

The charge at C_1 is redistributed between C_2 and C_1 in such a way that the total charge is conserved

$$q_1(t+2\tau) + q_2(t+2\tau) = q_1(t+\tau) + q_2(t+\tau)$$

 $C_1 v_2(t+2\tau) + C_2 v_2(t+2\tau) =$

$$= C_1 v_1(t+\tau) + C_2 v_2(t+\tau) = (C_1 + C_2) v_2(t+2\tau)$$

At time $t + 3\tau$. The charge at C_2 is conserved.

$$v_2(t+3\tau) = v_2(t+2\tau)$$

This is concluded into

$$(C_1 + C_2)v_2(t + 3\tau) - C_2v_2(t + \tau) = C_1v_1(t + \tau)$$

Let t = kT and $T = 2\tau$, z-transform

$$(z^{3/2}(C_1 + C_2) - z^{1/2}C_2)V_2(z) = C_1 z^{1/2}V_1(z)$$

This gives the transfer function

$$H(z) = \frac{V_2(z)}{V_1(z)} = \frac{C_1}{z(C_1 + C_2) - C_2} = \frac{C_1/(C_1 + C_2)}{z - C_2/(C_1 + C_2)}$$

 C_1 must be much larger than C_2 , $C_1 \gg C_2$, to achieve a sample-and-hold cirucit

$$H(z) = z^{-1}$$



Example parasitics II

Consider the parasitic capacitances C_a through C_h .

Analog Discrete-Time Integrated Circuits, TSTE80

During clock phase ϕ_2 , C_b , C_c and C_d are coupled in parallel. The same is true for C_f , C_g and C_h . C_a is short and C_e is connected to the input signal.

The charge on the parallel capacitances will redistribute to C_2 .

During clock phase ϕ_1 , C_a , C_b and C_c are coupled in parallel. The same is true for C_e , C_f and C_g . C_d is coupled to the input of the OPamp. C_h is connected to the output of the OPamp.

Now note that C_a , C_b , C_c and C_d always are connected to ground or virtual ground, hence always short and will not affect the transfer function. The charge on C_1 's plate connected to the input of the OPamp determines the transfer function. While the input signal is directly connected to C_1 neither will the capacitances C_e , C_f , C_e , or C_h affect the transfer function.



Exercises

Exercise K36

Derive the transfer function H(z).

At time t the charge at the transistors is written as

$$q_{1}(t) = C_{1}v_{1}(t)$$

$$q_{2}(t) = C_{2}v_{2}(t)$$

$$q_{\alpha 1}(t) = \alpha C_{1}v_{1}(t)$$

 $q_{\alpha 2}(t) = \alpha C_2 v_2(t)$

At $t + \tau$, αC_1 and αC_2 are completely shorted.

The total charge on C_1 and C_2 must however be conserved, while no charge can disappear from the input of the OPamp. Changes of the input signal will determine how the charge is distributed between C_1 and C_2 :

$$q_{1}(t+\tau) + q_{2}(t+\tau) = q_{1}(t) + q_{2}(t)$$
$$q_{\alpha 1}(t+\tau) = q_{\alpha 2}(t+\tau) = 0$$

At $t + 2\tau$ we use the same result. No charge disappears from the OPamp input. It has to redistribute to the other (previously discharged) capacitances:

$$q_{1}(t + \tau) + q_{2}(t + \tau) =$$

$$= q_{1}(t + 2\tau) + q_{2}(t + 2\tau) +$$

$$+ q_{\alpha 1}(t + 2\tau) + q_{\alpha 2}(t + 2\tau)$$

$$= q_{1}(t) - q_{2}(t)$$

This gives

 $C_1 v_1(t) + C_2 v_2(t) = (1+\alpha)C_1 v_1(t+2\tau) + (1+\alpha)C_2 v_2(t+2\tau)$

Let t = kT and $2\tau = T$. z-transform and the transfer function is

$$H(z) = \frac{V_2(z)}{V_1(z)} = -\frac{C_1}{C_2} \cdot \frac{(1+\alpha)z - 1}{(1+\alpha)z - 1} = -\frac{C_1}{C_2} \cdot \frac{z - \frac{1}{1+\alpha}}{z - \frac{1}{1+\alpha}} = -\frac{C_1}{C_2}$$

which is an inverting amplifier. The pole is cancelled by the zero.



Exercise K27

At time t the charge is discribed by

- $q_1(t) = C_1 v_1(t)$
- $q_2(t) = C_2 v_2(t)$ $q_3(t) = C_3 v_2(t)$
- 43(1) 3.2(

At time $t + \tau$:

Charge at C_1 and C_2

$$q_1(t+\tau) = q_1(t)$$

 $q_2(t+\tau) = q_2(t)$

 C_3 is charged with the input voltage

$$q_3(t+\tau) = C_3 v_1(t+\tau)$$

At time $t + 2\tau$:

Total charge on the three capacitances is

 $q_1(t+2\tau) + q_2(t+2\tau) + q_3(t+2\tau)$

where

$$q_1(t+2\tau) = C_1 v_1(t+2\tau)$$

 $q_2(t+2\tau) = C_2 v_2(t+2\tau)$

 $q_3(t+2\tau) = C_3 v_2(t+2\tau)$

The total charge must be conserved, no charge disappears from the input of the OPamp:

$$q_1(t+2\tau) + q_2(t+2\tau) + q_3(t+2\tau) =$$

$$= q_1(t+\tau) + q_2(t+\tau) + q_3(t+\tau) =$$

 $= q_1(t) + q_2(t) + q_3(t + \tau)$

Use the charge expression, and we have

$$(C_2 + C_3)v_2(t+2\tau) + C_1v_1(t+2\tau) = C_1v_1(t) + C_2v_2(t) + C_3v_1(t+\tau)$$

which gives

$$v_2(t+2\tau) - \frac{C_2}{C_2+C_3}v_2(t) = \frac{C_1}{C_2+C_3} \bigg[v_1(t) + \frac{C_3}{C_1}v_1(t+\tau) - v_1(t+2\tau) \bigg]$$

Let t = kT and $T = 2\tau$. z-transform

$$H(z) = \frac{V_2(z)}{V_1(z)} = \frac{C_1}{C_2 + C_3} \frac{1 + \frac{C_3}{C_1} z^{1/2} - z}{z - \frac{C_2}{C_2 + C_3}} = -\frac{C_1}{C_2 + C_3} \frac{z - \left(1 + \frac{C_3}{C_1} z^{1/2}\right)}{z - \frac{C_2}{C_2 + C_3}}$$

 V_1 C_1 V_2 C_3 C_3 C_2





We now see that the output signal is affected by the input signal at each half clock period. Two ways can be used to design a first-order all pass filter.

1) Eliminate $z^{1/2}$ by assuming $v_1(t) = v_1(t+\tau)$ which gives $z^{1/2}V_1(z) = V_1(z)$

2) Eliminate $z^{1/2}$ by assuming $v_1(t+\tau) = v_1(t+2\tau)$ which gives $z^{1/2}V_1(z) = zV_1(z)$

this gives

$$H_1(z) = -\frac{C_1}{C_2 + C_3} \cdot \frac{z - \frac{C_1 + C_3}{C_1}}{z - \frac{C_2}{C_2 + C_3}} \text{ or } H_2(z) = -\frac{C_1}{C_2 + C_3} \cdot \left(1 - \frac{C_3}{C_1}\right)^{z - \frac{1}{1 - C_3/C_1}}_{z - \frac{C_2}{C_2 + C_3}}$$

For an all pass filter, if the pole is given by z = p, the zero is given by z = 1/p. This gives

$$\frac{C_1 + C_3}{C_1} = \frac{C_2 + C_3}{C_2} \Rightarrow C_2 = C_1 \text{ or } 1 - \frac{C_3}{C_1} = \frac{C_2}{C_2 + C_3} \Rightarrow C_1 = C_2 + C_3$$

Exercise K28

At time t the lower C_1 is charged

 $q_{N1}(t) = C_1 v_1(t)$

The upper is shorted.

 $q_{U1}(t) = 0$

At time $t + \tau$ the upper C_1 is charged

$$q_{U1}(t+\tau) = C_1 v_1(t+\tau)$$

The lower is shorted. The charge will however redistribute to the negative plate at C_2 . The positive plate at C_2 will get extra charge from the output of the OPamp. The charge at C_2 is written as

$$\begin{array}{l} q_2(t+\tau) \,=\, C_2 v_2(t+\tau) \,=\, q_2(t) + q_{N1}(t) \,= \\ \\ =\, C_2 v_2(t) + C_1 v_1(t) \end{array}$$

At time $t + 2\tau$ the operation is practical the same due to the symmetrical capacitances.

$$q_2(t+2\tau) = C_2 v_2(t+2\tau) = q_2(t+\tau) + q_{U1}(t+\tau) = C_2 v_2(t+\tau) + C_1 v_1(t+\tau)$$

We see that the input signal is delayed and switched to the output at every half clock cycle. We have

$$v_2(t+2\tau) = v_2(t) + \frac{C_1}{C_2} [v_1(t+\tau) + v_1(t)]$$

And the transfer function is



$$H(z) = \frac{C_1}{C_2} \cdot \frac{z^{1/2} + 1}{z - 1}$$

If we now once again assume that $v_1(t) = v_1(t+\tau)$ or $v_1(t+\tau) = v_1(t+2\tau)$, then

$$H(z) = \frac{C_1}{C_2} \cdot \frac{2z^{-1}}{1 - z^{-1}} \text{ or } H(z) = \frac{C_1}{C_2} \cdot \frac{1 + z^{-1}}{1 - z^{-1}}$$

Exercise K38

General transfer function for bilinear integrator:

$$H(z) = K \cdot \frac{z-1}{z+1}$$

At time t the charge distribution is

$$q_1(t) = C_1 v_1(t)$$

 $q_2(t) = C_2 v_2(t)$

$$q_3(t) = 0$$
 (shorted)

At time $t + \tau C_3$ is coupled in parallel with C_1 and

will take charge from C_2 and C_1 :

$$q_1(t+\tau) = C_1 v_1(t+\tau)$$

$$a_{1}(t+\tau) = C_{1}v_{2}(t+\tau)$$





 C_1

 $q_3(t+\tau) = C_3 v_1(t+\tau)$ The charge distribution will be

$$q_1(t+\tau) + q_2(t+\tau) + q_3(t+\tau) = q_1(t) + q_2(t)$$

At time $t + 2\tau$ the total charge at C_1 and C_2 is conserved. It will though redistribute due to the change of input voltage.

$$q_1(t+\tau) + q_2(t+\tau) = q_1(t+2\tau) + q_2(t+2\tau)$$

Concludingly, we have

 $q_1(t) + q_2(t) = q_3(t+\tau) + q_1(t+2\tau) + q_2(t+2\tau)$, i.e.,

$$C_1 v_1(t) - C_1 v_1(t+2\tau) - C_3 v_1(t+\tau) = C_2 [v_2(t+2\tau) - v_2(t)]$$

which gives

$$v_2(t+2\tau) - v_2(t) = -\frac{C_1}{C_2} \left[v_1(t+2\tau) + \frac{C_3}{C_1} v_1(t+\tau) - v_1(t) \right]$$

Suppose $v_1(t) = v_1(t+\tau)$, hence a sample-and-hold circuit at the input, which eliminated the $z^{1/2}$ -term in the transfer function. Let t = kT and $2\tau = T$. z-transform

$$H(z) = \frac{V_2(z)}{V_1(z)} = -\frac{C_1}{C_2} \cdot \frac{z + (C_3/C_1 - 1)}{z - 1}$$

Elektronics Systems, http://www.es.isy.liu.se/

Choosee $C_3 = 2C_1$ and we have

$$H(z) = -\frac{C_1}{C_2} \cdot \frac{1+z^{-1}}{1-z^{-1}}$$

Exercise K37

At time *t*. The upper capacitor is shorted between ground and virtual ground and the lower capacitor is charged with the input voltage:



 C_2 has the charge:

$$q_2(t) = C_2 v_2(t)$$

At time $t + \tau$. The upper capacitor is charged.

$$q_{1u}(t+\tau) = C_1 v_1(t+\tau)$$

The lower capacitor is shorted, all charge is lost to the ground.

 $q_{1n}(t+\tau) = 0$

The charge in C_2 is conserved since no charge can disappear from the input of the OPamp.

 $q_2(t+\tau) = q_2(t) \text{ dvs } C_2 v_2(t+\tau) = C_2 v_2(t) \text{ dvs } v_2(t+\tau) = v_2(t)$

Time $t + 2\tau$. The upper capacitor is discharged, but its charge will be redistributed over the lower capacitor and C_2 . The redistribution is determined by the input voltage. We have

 $q_{1u}(t+2\tau) = 0, q_{1n}(t+2\tau) = C_1 v_1(t+2\tau), q_2(t+2\tau) = C_2 v_2(t+2\tau)$

and

$$-q_{1n}(t+2\tau) + (-q_2(t+2\tau)) = -q_{1u}(t+\tau) + (-q_2(t+\tau))$$

Which gives

 $C_1 v_1(t+2\tau) + C_2 v_2(t+2\tau) = C_1 v_1(t+\tau) + C_2 v_2(t+\tau) = C_1 v_1(t+\tau) + C_2 v_2(t)$

The input signal is sampled-and-held as

 $v_1(t+\tau) = v_1(t)$

which gives

$$C_1 v_1(t+2\tau) + C_2 v_2(t+2\tau) = C_1 v_1(t) + C_2 v_2(t)$$

z-transform

$$C_1 \cdot (z-1) \cdot V_1(z) = C_2 \cdot (1-z) \cdot V_2(z)$$

and

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$$H(z) = \frac{V_1(z)}{V_2(z)} = -\frac{C_2}{C_1} \cdot \frac{z-1}{z-1} = -\frac{C_2}{C_1}$$

The circuit is an inverting amplifier. Practically, however, a pole on the unit circle can not be

cancelled by a zero. The circuit has to be used in a feedback loop.

Exercise B10.2

At time t, switch ϕ_1 is conducting. The charges at C_1 and C_2 are given by

$$q_1(t) = C_1 \cdot v_1(t)$$
 and $q_2(t) = C_2 \cdot v_2(t)$

At time $t + \tau$, switch ϕ_2 is conducting. The charges at C_1 and C_2 are given by

$$q_1(t+\tau) = 0$$
 and $q_2(t+\tau) = C_2 \cdot v_2(t+\tau)$

Note that the positive and negative plates of C_1 are connected. The charge will cancel themselves, therefore

$$q_2(t+\tau) = q_2(t)$$

At time $t + 2\tau$, switch ϕ_1 is conducting. Now we will have a redistribution of the charge at the negative plate of C_2 (the one connected to virtual ground at the OPamp input).

$$\begin{aligned} q_1(t+2\tau) &= C_1 \cdot v_1(t+2\tau), \, q_2(t+2\tau) = C_2 \cdot v_2(t+2\tau) \text{ and} \\ -q_1(t+2\tau) + (-q_2(t+2\tau)) = -q_2(t+\tau) = -q_2(t) \end{aligned}$$

This gives

$$C_1 \cdot v_1(t+T) + C_2 \cdot v_2(t+T) = C_2 \cdot v_2(t)$$

where $T = 2\tau$. z-transforming the equation gives

$$\frac{V_2(z)}{V_1(z)} = H(z) = \frac{C_1}{C_2} \cdot \frac{z}{1-z} = -\frac{C_1}{C_2} \cdot \frac{1}{1-z^{-1}}$$

which is a invering and scaling integrator.

Exercises B10.3 - 4 are very suitable for calculation.



[kHz]

Samplad

specifikation

Referensfilterspecifikation

1.5 2.5 1/2T=20

0.2356 0.3927 π

 $\omega_0 \quad \omega_s$

Poisson

LDI

Example Exercise K40

Synthesize an LDI filter. Transformation give Rekonstruerad specifikation

28

1.25

28

28

1.25

 $s = s_0 \frac{z-1}{z^{1/2}}$ The specification on the reference filter

angular cut-off frequency is chosen to be

Analog Discrete-Time Integrated Circuits, TSTE80

 $\omega_c = 2\pi \cdot 1500 \, \text{rad/s}$

Since sampling frequency is $f_s = 40 \text{ kHz}$ we have the discrete-time cut-off frequency as

$$\Omega_c = \frac{1.5k}{40k} \cdot 2\pi \approx 0.2356$$

 $\Omega_s = \frac{2.5k}{40k} \cdot 2\pi \approx 0.3927$

and the discrete-time stop-band frequency as



$$s_0 = \frac{\omega_c}{2\sin(\Omega_c/2)} =$$

$$=\frac{3000\pi}{2\sin(0.2356/2)}\approx40.093\,\text{krad/s}$$

We find the ω_{c}

$$\omega_0 = 2s_0 \sin(\Omega_s/2) \approx$$

$$\approx 2 \cdot 40.093 \cdot \sin(0.3927/2) \approx$$

$$\approx 15.643 \, \text{krad/s}$$

Design an elliptic filter. Order is found to be N = 3. Suppose the resistors are equal, or

 $\kappa^2 = 1$ and choose $R_i = R_0 = 1k\Omega$

The normated values on the components are

$$C_{1n} = C_{3n} = 1.9314$$
, $C_{2n} = 0.3781$ and $L_{2n} = 0.7571$

These are denormalized with

$$L_i = \frac{R_0}{\omega_0} L_{in}$$
 and $C_i = \frac{1}{\omega_0 R_0} C_{in}$

Lesson 9

Lesson Exercises:	B10.5 - B10.10, K31, K32, K33, K34, K40
Lesson Exercises:	B10.5 - B10.10, K31, K32, K33, K34, K4

Recommended Exercises: K29, K35

Theoretical Issues: SC-filter

Theoretical

SC-filter

Leapfrogfilter

In many cases we use a continous-time analog reference filter to find the specifications on the SC filter. The filter is transformed with LDI or bilinear transformation into a suitable discrete-time representation.

Lossless Discrete Integrator, LDI transformation

Let the transformation be given by

$$s = s_0[z^{1/2} - z^{-1/2}] = s_0 \frac{1 - z^{-1}}{z^{-1/2}} = s_0 \frac{z - 1}{z^{1/2}} = s_0 \cdot \frac{1 - z^{-1}}{z^{-1/2}}$$

Or using integration notation

$$\frac{1}{s} = \frac{1}{s_0} \cdot \frac{z^{-1/2}}{1 - z^{-1}}$$

Let

$$s = i\omega$$
 and $z = e^{j\Omega}$

which gives

$$\omega = 2s_0 \sin\left(\frac{\Omega}{2}\right)$$
 or $s_0 = \frac{\omega}{2\sin(\Omega/2)}$

where ω is the continous-time angular frequency and Ω is the discrete-time. Due to the LDI mapping we see that

 $\omega < 2s_0$

From that we conclude that the filters to be transformed must be narrow banded. This is a drawback with the LDI transformation.

We also find that

$$z^{-1/2} = e^{-j\Omega/2} = \cos\frac{\Omega}{2} - j \cdot \sin\frac{\Omega}{2}$$

Ra

R

 I_0

 $\frac{R}{R_i}$

-V

 $-C_2/\alpha_1$

-RI₂

Which gives

$$C_1 = C_3 = 204.9nF$$
$$L_2 = 80.3mH$$
$$C_2 = 40.1nF$$

The filter is transformed. The constant used in the figure is given by

$$\alpha_1 = C_1 + C_2 = C_2 + C_3$$

Setting up the wellknown equations for currents and voltages in the filter, we have

$$RI_{0} = RI_{i} - \frac{R}{R_{i}}V_{1}$$

$$V_{1} = \frac{1}{sRC_{1}}(RI_{0} - RI_{2}), RI_{2} = \frac{R}{(sL_{2}) \parallel (1/sC_{2})}(V_{1} - V_{3})$$

$$V_{3} = \frac{1}{sRC_{3}}(RI_{2} - RI_{4}), RI_{4} = \frac{R}{R_{0}}V_{3} = \frac{R}{R_{0}}V_{L}$$

etc. With this the signal flow graph becomes



LDI transform by setting

$$s = s_0 \cdot \frac{z - 1}{z^{1/2}}$$

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$$R_0$$

 $rac{R_0}{I_0}$
Elminate $z^{-1/2}$ in the integrators by propagating backwards.



 $-C_2/\alpha_1$

 $z^{-1/2}$

 $s_0 L_2 \overline{1 - z^{-1}}$

We now though have $z^{-1/2}$ terms in the outer feedback amplifiers. This is practically not possible to implement. One way to implement this is simply to remove the $z^{-1/2}$ term in the expression:

$$\frac{R}{R_L} \cdot z^{-1/2}$$

We could assume that the original R_L and R_i have the expressions

$$R_L = R_L \cdot z^{-1/2}$$
 and $R_i = R_i \cdot z^{-1/2}$

As discussed earlier, $z^{-1/2}$ naturally contains valuable frequency information

$$z^{-1/2} = -j\frac{\omega}{2s_0} + \sqrt{1 - \left(\frac{\omega}{2s_0}\right)^2}$$

V₃=V_L

-1/2

 $s_0 R\alpha_2 1$

 $\frac{R}{R_0}$

C₂

11 C3

 V_2

Thereby

$$R_{L} \cdot z^{-1/2} = R_{L} \left[-j\frac{\omega}{2s_{0}} + \sqrt{1 - \left(\frac{\omega}{2s_{0}}\right)^{2}} \right] =$$

$$= R_{L} \sqrt{1 - \left(\frac{\omega}{2s_{0}}\right)^{2}} - j\omega\frac{R_{L}}{2s_{0}} = R_{L}(\omega) - j\omega L_{L}$$

$$R_{L} \longrightarrow \left\{ -L_{L} \right\}$$

Which is realized by a frequency dependent resistance in series

with an inductance, or more useful in this filter implementation, as a frequency dependet resistance in parallel with a capacitor.



Suppose that C_L is coupled in parallel with C_3 and correspondingly

for the inner source resistance C_i is in parallel with C_1 . This is corrected by letting the components have the values

$$C_{1}' = C_{1} - C_{i} = C_{1} - \frac{1}{2s_{0}R_{i}} = C_{1} - \frac{1}{\omega_{0}R_{i}}\sin\left(\frac{\Omega_{0}T}{2}\right) \text{ and}$$

$$C_{3}' = C_{3} - C_{L} = C_{3} - \frac{1}{2s_{0}R_{L}} = C_{3} - \frac{1}{\omega_{0}R_{L}}\sin\left(\frac{\Omega_{0}T}{2}\right)$$

We still have an error that is caused by the fact that we will not implement a frequency dependent resistance. This error is considered to be acceptable. The realization of the filter is given by the flow graph



The two integrators (inverting amplifiers with and without delay) are replaced with their corresponding SC circuits. The transfer function of the summing integrator is given by

$$V_{3}(z) = \frac{z^{-1}}{1 - z^{-1}} \cdot \left[\frac{C_{1}}{C_{3}} \cdot V_{1}(z) + \frac{C_{2}}{C_{3}} \cdot V_{2}(z) \right]$$

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Check: No direct signal path from input to the output. The transfer function of the summing and inverting integrator is given by

$$V_{3}(z) = -\frac{1}{1-z^{-1}} \cdot \left[\frac{C_{1}}{C_{3}} \cdot V_{1}(z) + \frac{C_{2}}{C_{3}} \cdot V_{2}(z)\right]$$

Check: Direct signal path from input to the output.

(Charge that is directed to C_3 is given by a linear combination of

the input signals $v_1(t)$ and $v_2(t)$.)

Integrators are used in the realization. The sizes of the capacitors

have to be identified. This is done by comparing signal paths in the SC realization with those of the signal flow graph:



For the feedback we have:

$\left[-V_{1}\right]_{V_{3}} = -\frac{C_{14}}{C_{7}}$	$\left[-V_{1}\right]_{V_{3}} = -\frac{C_{2}}{\alpha_{1}}$	$\frac{C_{14}}{C_7} =$	$\frac{c_2}{\alpha_1}$
$[V_3]_{-V_1} = -\frac{C_{15}}{C_{13}}$	$[V_3]_{-V_1} = -\frac{C_2}{\alpha_3}$	$\frac{C_{15}}{C_{13}} =$	$\frac{C_2}{\alpha_3}$

We assume that

$$R_i = R_L = R$$

Lesson 9



Further, the correction term gives

$$s_0 = \frac{\omega_c}{2\sin(\Omega_c/2)}$$
 and $C_i' = C_i - 1/2s_0R$

Which yields

$$\frac{C_4}{C_7} = \frac{C_5}{C_7} = \frac{C_6}{C_7} = \left[\frac{\omega_c R(C_1 + C_2)}{2\sin(\Omega_c/2)} - \frac{R}{2R}\right]^{-1}, \frac{C_{11}}{C_{13}} = \frac{C_{12}}{C_{13}} = \left[\frac{\omega_c R(C_3 + C_2)}{2\sin(\Omega_c/2)} - \frac{R}{2R}\right]^{-1}$$

$$\frac{C_8}{C_{10}} = \frac{C_9}{C_{10}} = \frac{2R\sin(\Omega_c/2)}{\omega_c L_2}$$

$$\frac{C_{14}}{C_{13}} = \frac{C_2}{C_2 + C_1 - \frac{\sin(\Omega_c/2)}{R_i\omega_c}} \text{ and } \frac{C_{15}}{C_{13}} = \frac{C_2}{C_2 + C_3 - \frac{\sin(\Omega_c/2)}{R_L\omega_c}}$$

With values we have

$$\frac{C_4}{C_7} = \frac{C_5}{C_7} = \frac{C_6}{C_7} = \frac{C_{11}}{C_{13}} = \frac{C_{12}}{C_{13}} = \left[\frac{2\pi \cdot 1500 \cdot 1000 \cdot (204.9n + 40.1n)}{2\sin(0.2356/2)} - \frac{1}{2}\right]^{-1} \approx 0.1072$$

$$\frac{C_8}{C_{10}} = \frac{C_9}{C_{10}} = \frac{2 \cdot 1000 \cdot \sin(0.2356/2)}{3000\pi \cdot 80.3m} \approx 0.3106$$

$$\frac{C_{14}}{C_{13}} = \frac{C_{15}}{C_{13}} = \frac{40.1n}{40.1n + 204.9n - \frac{\sin(0.2356/2)}{1000 \cdot 3000\pi}} \approx 0.1725$$

Choose the integrators' capacitors all equal

 $C_7 = C_{10} = C_{13} = 47 \,\mathrm{nF}$

From this we have the values of all other capacitors. Scaling:



Scale the filter so that the relation between the OPamp outputs and the input signal is unity $(L_{\infty}$ -norm). We are scaling the filter to keep the signal levels at wanted levels. The principle of scaling can be described by dividing the net into subnets. The subnets have a number of inputs and outputs. If the inputs are scaled with a constant k_i all nodes of the subnet will be scaled with a factor k_i , as well as we have to scale all outputs with $1/k_i$.

In this case the signal after the first node is scaled to k_1X_1 , the second with $k_2k_1X_2$ and finally the third (the output) with $k_3k_2k_1X_3$. By changing the values of the capacitances we now can realize the scaling. At C_4 we use k_1C_4 instead. For $C_6 \rightarrow C_6/k_2$, $C_8 \rightarrow C_8 \cdot k_2$,

$$C_{14} \rightarrow \frac{C_{14}}{k_2 k_3}, C_{15} \rightarrow C_{15} \cdot k_2 k_3, C_9 \rightarrow C_9 / k_3, C_{11} \rightarrow C_{11} \cdot k_3 \text{ etc.}$$

Elektronics Systems, http://www.es.isy.liu.se/

Exercises

Exercise K35

Third order low pass filter with an elliptic reference filter. The specification gives



Normalized values from table are:

$$R_i = R_0 = 1k\Omega$$
, $C_{1,n} = C_{3,n} = 0.5275$, $C_{2,n} = 0.1921$, $L_{2,n} = 0.7700$

 R_i

 C_3

LDI transformation gives

$$s = s_0 \cdot \frac{1 - z^{-1}}{z^{-1/2}}$$
 where $s_0 = \frac{\omega_{ac}}{2\sin(\omega_c T/2)}$

Denormalize the values.

Compensate for the LDI transformation errors. Find the flow graph Use standard SC integrators. Identify the values

Exercise K34

Due to the fact that

 $R = R_i = R_L$

we know that the dc gain is 1/2

You can also see that the filter is realizing a third order elliptic low pass filter. Suppose that the maximum output value is given by dc voltage. This implies that we directly can choose the scaling parameter k_1 in such a way that all nodes in the net become scaled with a factor two,

hence $k_1 = 2$.

Exercise K33

The order is found to be N = 3. Values are

$$C_{3n} = 1$$
, $L_{2n} = 2$, $C_{\overline{1n}} = 1$ and
 $R_i = R_L = 1k\Omega$





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