Lesson 10

Lesson Exercises: **B11.7-8, B12.6, B12.10**

Recommended Exercises: *B11.1-2, B11.10, B12.5-7, B12.17-18, B13., B14.*

Theoretical Issues: **Analog-to-Digital and Digital-to-Analog Converters, Repetition**

Theoretical

• Converter Types

DACs

- Current-Steering – Switched and weighted current sources
- Charge Redistribution – Switched and weighted capacitors
- R-2R Ladder – Unit current sources
- Resistor Strings – Voltage drop over a resistor string.

ADCs

- Integrating Converters – Sweep a ramp over time and compare with the input voltage.
- Successive-approximation – Comparing input voltage with a value and set bits.
- Algorithmic – Feedback and comparison.
- Flash – Parallel comparators.
- Pipeline – Several steps of converters (preferrably one-bit)
- Time-Interleaved – Parallel converters working at lower speed.

Oversampled Converters

- Interpolation Filter – Oversamples and low pass filters the input signal
- Decimation Filter – Vice versa
- Demodulator – Modulator – Shapes the noise

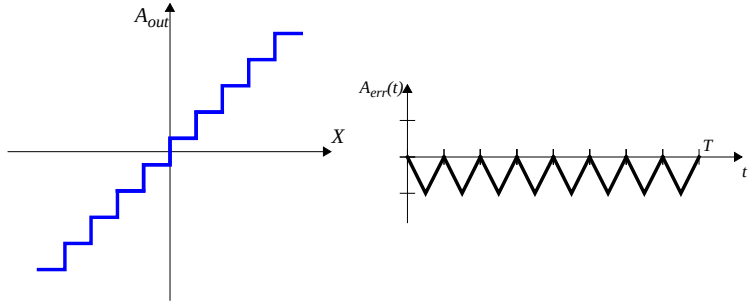
Signal feedback and error feedback

Pulse Code Modulation

• Performance Measures

- Static and Dynamic measures
- Time- and Frequency-Domain measures

Signal-to-Noise Ratio



The signal-to-noise ratio, SNR, can be found by investigating the quantization noise. It is assumed that we have fine quantization, i.e., harmonic terms are hidden below the average noise floor.

The true output value for a binary uniform converter can be written as

$$A_{true}(t) = \sum_{k=0}^{2^N-1} A_k \cdot \{u(t-k\Delta T) - u(t-(k+1)\Delta T)\}$$

It is assumed that sample-and-hold elements are used. The wanted output can be written as

$$A_{want}(t) = \frac{t}{T} \cdot A_{max} = \frac{t}{T} \cdot (A_{ref} \cdot 2^N) = \frac{t}{\Delta T} \cdot A_{ref}$$

Hence a straight line.

The quantization error as function of the time can be written as

$$A_{err}(t) = A_{want}(t) - A_{true}(t)$$

We can now find the error r.m.s. value, $A_{err,\,rms}$, by using

$$A^2_{err,\,rms} = \frac{1}{T}\int_0^T [A_{want}(t) - A_{true}(t)]^2 dt$$

We see that this can – due to the regularity of the error signal – be written as

$$A^2_{err,\,rms} = \frac{A^2_{ref}}{\Delta T/2}\int_0^{\Delta T/2} \left[\frac{t}{\Delta T}\right]^2 dt = \frac{A^2_{ref}}{12}$$

Now if the input is a full scale sinusoidal with amplitude

$$A = \frac{2^N-1}{2} \cdot A_{ref}$$

where N is the number of bits. The r.m.s. value of this sinusoidal is

$$A_{rms} = \frac{A}{\sqrt{2}} = \frac{1}{\sqrt{2}} \cdot \frac{2^N-1}{2} \cdot A_{ref}$$

We now can find the power ratio within the Nyquist bandwidth to be

$$\frac{A_{rms}^2}{A_{err,\,rms}^2} = \frac{\frac{1}{8}\cdot(2^N-1)^2\cdot A_{ref}^2}{A_{ref}^2/12} = \frac{3}{2}\cdot(2^N-1)^2$$

In a logarithmic scale and with a large number of bits this is approximately

$$\text{SNR} = 6.02\cdot N + 1.76 \text{ dB}$$

Differential Nonlinearity, DNL

Let the error at level i be described by

$$d_i = A_{true}(i) - A_{want}(i)$$

The differential nonlinearity, DNL, is given by

$$D_i = d_i - d_{i-1} = [A_{true}(i) - A_{true}(i-1)] - [A_{want}(i) - A_{want}(i-1)]$$

Since we assume that the codes are consequitive, this can be written as

$$D_i = [A_{true}(i) - A_{true}(i-1)] - 1 \text{ [LSB]}$$

where the unit LSB is used.

Integral Nonlinearіy, INL

The integral nonlinearity is the deviation from a straight line. This can also be expressed as

$$I_i = \sum_{k=0}^{i} D_i$$

Gain Error

- Linear and nonlinear gain.

Linear gain may often be neglected since it only changes the swing. Nonlinear gain however introduces distortion.

Offset Error

May often be neglected since differential signals are widely used.

Nonlinear Slewing

Affects the linearity, since we have signal dependent settling time. This introduces distortion.

Repetition

- **CMOS Models**
- **Basic Gain Stages**
- **Operational Amplifiers**
- **Feedback**
- **Comparators**
- **Noise**
- **Signal Flow Charts**
- **Second Order Filters**
- **Gm-C Filters**
- **Active RC Filters**
- **Active MOSFET-C Filters**
- **Leapfrog Filters**
- **Charge Redistribution**
- **SC Circuits**
- **LDI Transform**
- **ADCs and DACs**

Exercises

Exercise B11.1

$V_{LSB} = 1\,\text{mV}$.

10-bit indicates 2^{10} levels, hence the maximum output is $V_{LSB} \cdot (2^{10} - 1) = 1.023V$. Note that the zero code exists.

Exercise B11.2

$N = 12$ bits. The reference voltage is $V_{ref} = 3\,\text{V}$. We know that the signal-to-noise ratio is found to be $\text{SNR} = 6.02 \cdot N + 1.76$ within the Nyquist bandwidth.

If the input voltage (peak-to-peak) is $V_{pp} = 1\,\text{V}$. The signal-to-noise ratio becomes

$$\text{SNR} = 10\log\left\{\frac{\left(\frac{V_{pp}}{2}\right)^2/2}{\left(\frac{V_{ref}}{2^N}\right)^2/12}\right\} = 10\log\left(\frac{12 \cdot 2^{24}}{72}\right) = -7.78 + 72.25\ \text{[dB]}$$

If the SNR should be zero dB the input sinusoidal amplitude, $V_{pp,0}$, has to be given by

$$\left(\frac{V_{pp,0}}{2}\right)^2/2 = \left(\frac{V_{ref}}{2^N}\right)^2/12$$

which gives

$$V_{pp,0} = \sqrt{\frac{2}{3}} \cdot \frac{V_{ref}}{2^{12}} \approx 598\mu\,\text{V}$$

Exercise B11.7

$V_{ref} = 8\,\text{V}$

Values are: [–0.01, 1.03, 2.02, 2.96, 3.95, 5.02, 6.00, 7.08]

Offset error is given by the first value: $O_e = -0.01$.

The gain error is given as the difference between the true full-scale value and the wanted full-scale value (in units of LSBs), hence

$$G_e = \frac{\text{FS}_{true} - \text{FS}_{want}}{1\ \text{LSB}} = \frac{7.08 - (-0.01) - 7}{1} = 0.09$$

Note the correction for the offset error.

The DNL is given by the absolute values. First find all deviations corrected with the offset error:

$d_0 = 0$, $d_1 = 1.03 - (-0.01) - 1 = 0.04$, $d_2 = 2.02 - (-0.01) - 2 = 0.03$,

$d_3 = 2.96 - (-0.01) - 3 = 0.03$, $d_4 = 3.95 - (-0.01) - 4 = 0.04$,

$d_5 = 5.02 - (-0.01) - 5 = 0.03$, $d_6 = 6.00 - (-0.01) - 6 = 0.01$,

$d_7 = 7.08 - (-0.01) - 7 = 0.09$

The DNL is found by

$D_1 = d_1 - d_0 = 0.04 - 0 = 0.04$, $D_2 = d_2 - d_1 = 0.03 - 0.04 = -0.01$

$D_3 = d_3 - d_2 = 0.03 - 0.03 = 0$, $D_4 = 0.04 - 0.03 = 0.01$,

$D_5 = 0.03 - 0.04 = -0.01$, $D_6 = 0.01 - 0.03 = -0.02$, $D_7 = 0.09 - 0.01 = 0.08$

The INL is found by

$I_0 = 0$, $I_1 = 0.04$, $I_2 = 0.03$, $I_3 = 0.03$, $I_4 = 0.04$,

$I_5 = 0.03$, $I_6 = 0.01$, $I_7 = 0.09$

In this case the peak DNL is 0.08 and the peak INL is 0.09

We can however compensate for offset and gain error, and also assume that min and max values are fixed, i.e. 0 and 7. Therefore new, relative, values are found by setting

$$L_i = \frac{V_i}{V_{LSB}} - O_e - G_e \cdot \frac{i}{2^N - 1}$$

where $N = 7$ is the number of bits. This gives the normated values:

$L_0 = 0$, $L_1 = 1.027$, $L_2 = 2.004$, $L_3 = 2.931$,

$L_4 = 3.909$, $L_5 = 4.966$, $L_6 = 5.933$, $L_7 = 7$

From these values we now have DNL

$D_1 = 0.027$, $D_2 = -0.023$, $D_3 = -0.073$, $D_4 = -0.022$,

$D_5 = 0.057$, $D_6 = -0.033$, $D_7 = 0.067$

And INL

$I_0 = 0$, $I_1 = 0.027$, $I_2 = 0.004$, $I_3 = -0.069$,

$I_4 = -0.091$, $I_5 = -0.034$, $I_6 = -0.067$, $I_7 = 0$

Peak DNL is 0.073 and peak INL is -0.091.

Using this compensation we improve the DNL but vice versa for the INL.

Exercise B11.8

Absolute accuracy:

Peak DNL gives 0.08. $V_{LSB} > 0.08$ and $V_{LSB} = \frac{V_{ref}}{2^{N_{effabs}}} > 0.08$. Hence $N_{effabs} = 6.6\,\text{bits}$ since $V_{ref} = 8\,\text{V}$.

Relative accuracy:

Peak INL gives 0.091. Which gives $N_{effrel} = 6.5\,\text{bits}$.

Exercise B11.10

In the same way as above. Offset and gain errors are given by $O_e = 0.01$ and $G_e = 0.01$ respectively. This gives the relative values:

$$L_0 = 0,\ L_1 = 1.007,\ L_2 = 1.953,\ L_3 = 3$$

DNL is given by $D_1 = 0.007,\ D_2 = -0.054,\ D_3 = 0.047$

INL is given by $I_0 = 0,\ I_1 = 0.007,\ I_2 = -0.047,\ I_3 = 0$

Maximum relative INL error is -0.047 which gives $N_{effrel} = 6.4$ bits.

Exercise B12.5

Trivial.

The ratio between largest and smallest resistor is given by $\frac{2^{10} \cdot R}{2 \cdot R} = 512$

The currents through the resistors are found in the same way.

Exercise B12.6

In the same way as discussed in the previous exercise. The resistance ratios are of 2^i therefore the significance of the matching is 2, 4, 8, ... time the matching required for the b_1 resistor.

Exercise B12.17

Exercise B12.18

Exercise B13.1

The maximum time occurs when there is a full scale input. 18-bits give 2^{18} cycles, and the circuit also has to be reset and therefore the total conversion time is given by

$$2 \cdot 2^{18} \cdot T_{clk} = \frac{2^{19}}{f_{clk}} = \frac{2^{19}}{5 \times 10^6} \approx 105\,\text{ms}$$

Exercise B13.2