8 Amplifiers III – Special amplifiers

Part 8.A—Transconductor elements

Ideal transconductor

We want that the output current should be given by

$$I_{out} = G_m \cdot V_{in}$$

But we also (unlike the operational amplifier in open-loop configuration) want that the circuit should work in a wide input voltage range. The input and output impedances should be infinite large. At the input side, this is "easily" achieved by using CMOS gates. At the output side, we will however have problems with the limited output impedance and this is also a limiting factor on performance. In Fig. 8.1 we illustrate the transconductor and its ideal transfer function. Using the

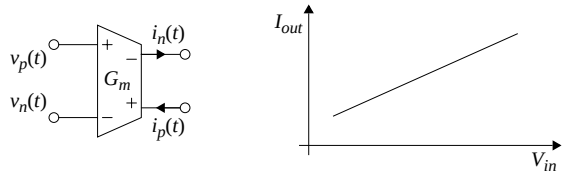

Figure 8.1: Transconductor and its ideal transfer function.

notation in the figure, we have that

$$V_{in} = v_p - v_n \text{ and } I_{out} = i_p - i_n, \text{ hence } (i_p - i_n) = G_m \cdot (v_p - v_n)$$

Improvement of linearity and CMOS transconductors

Naturally, there are several different ways to implement the transconductor. Basically, one can use an OTA but then one must be very careful with the voltage swings and the DC levels of the input signals.

One way is to linearize the circuit by using a MOS transistor in its linear region, as is illustrated by figures 15.21-23, 25 in the Johns&Martin book (Chapter 15.3).

The transconductor as integrator

In Fig. 8.2 we show four differential transconductance-C integrator configurations. The first (a) illustrates the functional view of the Gm-C integrator. The output currents are given by the transconductance times the input voltage. Then the output voltage is given by the voltage generated by the current through the capacitor. We have that

$$V_{out} = I_{out} \cdot \frac{1}{sC} \text{ and } I_{out} = V_{in} \cdot G_m, \text{ hence } V_{out} = \frac{1}{s} \cdot \frac{G_m}{C} \cdot V_{in}$$

The second figure (b) shows the real case implementation. The bottom-plate of the capacitor will be "closest" to the substrate and will therefore also create a large capacitance between the output wire and ground. This parasitic capacitance can be very large. A way to work around this is shown in (c) where we use "controlled" parasitic cancelling, hence we use two capacitors $(C/2)$ and let both transconductor outputs be connected to a bottom-plate. However, still the parasitic can be large and the best way to work around the problem is to use the configuration in (d). However,

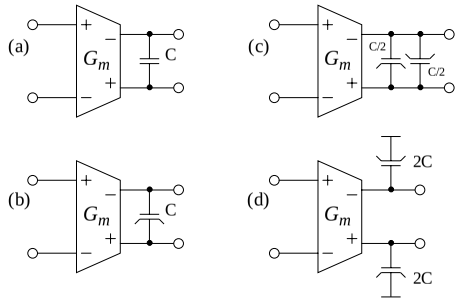

Figure 8.2: Differential transconductance-C integrator configurations. (a) Functional view, (b) real-case indicating bottom-plate, (c) "controlled" parasitics, and (d) parasitic insensitive

this configuration requires larger capacitors in order to maintain the same (G_m/C) integrator ratio. (One can also decrease the transconductance value G_m.)

Part 8.B—Switches and Track&Hold

Some important building blocks are the switches and track&hold/sample&hold. For high-accuracy A/D converters the track&hold is unavoidable.

The track&hold circuit in its simplest shape is shown in Fig. 8.3 (a). However, this circuit does

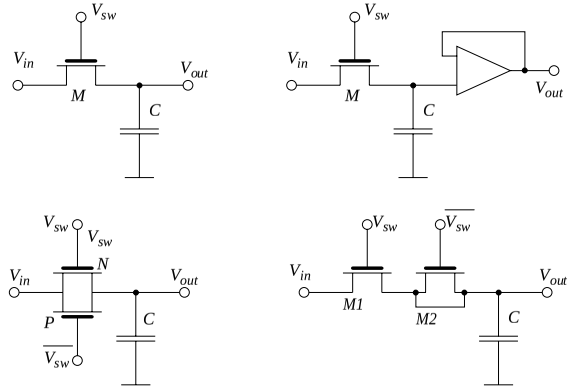

Figure 8.3: Sampling switches. (a) simple switch, (b) sampling switch with buffer, (c) dummy transistor to reduce charge injection, and (d) transmission gate implementation.

not have any driving capability and a buffer (b) is mostly needed. In (c) we use a transmission gate (PMOS and NMOS transistor) in order to reduce the resistance through the switch. Using a transmission gate also reduces the signal-dependent switching time instant of the switch.

The phenomena referred to as clock feedthrough (CFT) is reduced by using a dummy switch as illustrated in Fig. 8.3 (d).

Bandwidth of simple Track&Hold

The T&H shown in Fig. 8.3 (a) will suffer from the nonlinear resistance and the charge injection of the switch transistor. The switch voltage V_{sw} must be high compared to the input and output voltages. The transistor operates in its linear region and therefore, we have that the resistance is approximately

$$R_{on} = \frac{1}{\alpha \cdot ((V_{GS}-V_T)-V_{DS})} = \frac{1}{\alpha \cdot (V_G-V_T-V_D)} = \frac{1}{\alpha \cdot (V_{sw}-V_T-V_{in})}$$

Then the bandwidth of the switch is given by

$$\omega_{\text{-3dB}} = p_1 = \frac{1}{R_{on} \cdot C} = \frac{\alpha}{C} \cdot (V_{sw}-V_T-V_{in})$$

In order to increase the bandwidth we can choose to increase the switch voltage V_{sw} and reduce the input DC voltage as well as reducing the transistor size aspect ratio. Another approach is to use the transmission gate as illustrated in Fig. 8.3 (c) where the resistance is halfed.

Induced channel charge through clock feedthrough (CFT)

Another issue is the induced charge when the switch is turning on and off. The drain-gate (or source-gate) capacitance will through the rapid change of the switch signal add/remove charge from the sample capacitance and hence not yield the true output voltage. This effects are illustrated in Fig. 8.4

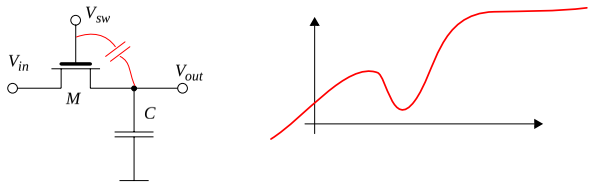

Figure 8.4: CFT in a switch with (a) capacitive coupling and (b) influence on the output signal.

The major contribution to this charge is given by

$$\Delta Q_{out} = \frac{C_{gs}}{2} \cdot V_{eff} = \frac{C_{ox} \cdot WL \cdot (V_{sw}-V_T-V_{in})}{2}$$

and it flows onto the sample capacitance and hence the induced additional voltage (sign is dependent on slope of switch signal) is given by

$$\Delta V_{out} = \frac{\Delta Q_{out}}{C} = \frac{C_{ox} \cdot WL \cdot (V_{sw}-V_T-V_{in})}{2 \cdot C}$$

Naturally, we want to keep this voltage as low as possible and therefore we can reduce V_{eff} and/or increase the sample capacitance. This will however make the switch slower. We can reduce W but once again, this increases the resistance. By reducing L we gain both in CFT and bandwidth.

The CFT can be reduced by using a dummy switch as illustrated in Fig. 8.3 (d). The dummy need to be half the size of the switch transistor and it must be switched in counter-phase. Then ΔQ_{out} from the switch will be absorbed by the dummy transistor (Fig. 8.5) and the CFT is cancelled.

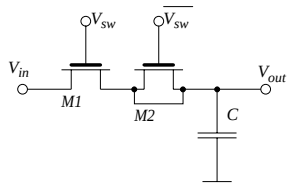

Figure 8.5: Channel charge flowing “into” the dummy switch.

Another issue is the signal-dependent sampling instant. The switch operates differently dependent on the input signal level.

However, to reach better performance, an active track&hold is most likely preferrable.

Part 8.C—Comparator

Ideal comparator

The ideal comparator as illustrated in Fig. 8.6 shall only give two output values; high or low. The

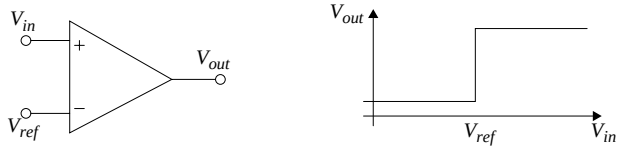

Figure 8.6: Ideal comparator and its transfer function.

input signal is compared to a reference value.

The input impedance of the comparator should be infinite and the output impedance should be zero. The comparator must also have a very high slew rate. The gain does/must/should not have to be linear.

If the comparator is not ideal, we may have problems like meta-stability as the input signal is close to the reference voltage and the output is not driven to the supplies but stuck at a value in-between which cannot be detected as neither high nor low.

OP amp as comparator

The OP amp can be used as a comparator (Fig. 8.7) but not for high performance applications. This is mainly due to the requirements on the offset voltage, settling speed and slew rate.

Assume that the comparator should be able to detect a least significant bit (LSB) and return 0 or V_{dd}. For a 14-bit application the comparator needs to be able to detect variations in the order of $V_{dd}/2^{14}$. In a 3-V application, this is equal to approximately 0.18 mV.

Notice that the settling time constant of a circuit with a dominant pole, p_1 is given by $\tau = 1/p_1$. Now, if we consider the OP/OTA, we have mostly designed it for a dominant pole at low frequencies, since the DC gain is very high. We have that

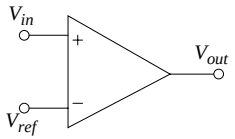

Figure 8.7: OP as comparator.

$$\tau = \frac{1}{p_1} = \frac{A_0}{\omega_u}$$

And hence the comparator using an OP will be slow. Instead we may want to increase the dominant pole with maintained unity-gain frequency to the cost of lower gain. This can practically be achieved by increasing the current through the circuit in order to also increase the slew rate. To compensate for the loss of gain, we use a multi-stage comparator (or cascaded comparators).

Cascaded comparators

The settling time constant must be reduced and the gain should be maintained. Assume that we can us a number of cascaded comparators as is illustrated in Fig. 8.8. Each comparator has a dom-

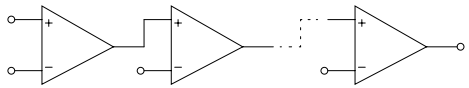

Figure 8.8: Cascaded comparators.

inant pole and a small-signal transfer function given by

$$A_i(s) = \frac{A_{i,0}}{1 + s/p_{i,1}}$$

When cascading N comparators, the total transfer function is given by

$$A_T(s) = \frac{\prod_{i=1}^{N} A_{i,0}}{\prod_{i=1}^{N}\left(1 + \frac{s}{p_{i,1}}\right)} \approx \frac{A_{T,0}}{1 + s \cdot \sum_{i=1}^{N} \frac{1}{p_{i,1}}}$$

We assume that the comparators are approximately identical and we have that

$$A_T(s) \approx \frac{A_{i,0}^N}{1 + s \cdot \frac{1}{p_1/N}}$$

where A_0 is the DC gain of one comparator and p_1 is the dominant pole. We see that the dominant pole for the multi-stage comparator is N times lower than for one of the single-stage comparators.

However, what is important is that the gain is increasing exponentially with N while the settling time constant is increasing linearly with N.

The time constants are given by

$$\tau_m = N \cdot \frac{A_{i,0}}{\omega_u} = N \cdot \frac{\sqrt[N]{A_0}}{\omega_u} \text{ and } \tau_{OP} = \frac{A_0}{\omega_u}$$

Example; if $N = 4$ and $A_0 = 2^{16}$ (64000), then we have that

$$\tau_m = 4 \cdot \frac{\sqrt[4]{2^{16}}}{\omega_u} = \frac{2^6}{\omega_u} \text{ and } \tau_{OP} = \frac{2^{16}}{\omega_u}, \text{ hence } 2^{10} \approx 1000 \text{ times larger}$$

Notice, that one should use to many stages due to the mismatch, offset, and parasitic issues.

Switched Comparators

Since in most high-performance applications a track&hold (or sample&hold) is used at the input. Therefore, the input signal is only valid at different clock phases. This should be utilized in the comparator as well, especially for offset compensation techniques.

Input offset cancellation

In Fig. 8.9 we illustrate the concept of input offset cancellation technique which requires a high-gain amplifier.

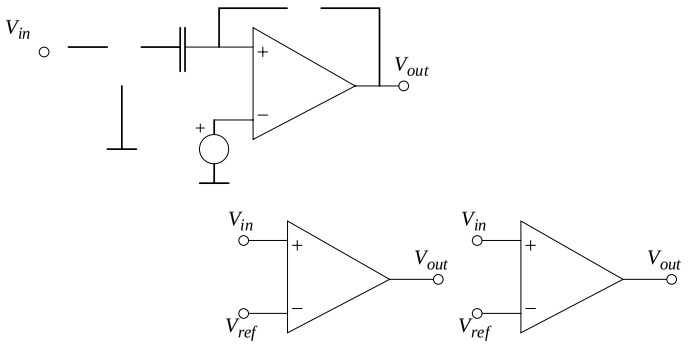

Figure 8.9: Input offset cancellation (a) with switches, (b) during phase 1, and (c) during phase 2.

On phase 1 we have a buffer configuration and the offset voltage as modelled in the figure is present at both inputs of the amplifier. The input capacitor samples V_{os}. On the second phase, the capacitor still holds the offset voltage. We have that the negative input is $V_{in} + V_{os}$ and the positive input is still given by V_{os}, hence the output is given by

$$V_{out} = A \cdot (V_{os} - (V_{in} + V_{os})) = -A \cdot V_{in}$$

and hence the offset voltage is cancelled.

This technique reduces the offset voltage, but also the $1/f$-noise. However, there is an increased capacitive load for the preceeding track&hold and there is also a resistance in the switch in the feedback loop further introducing a pole which affects the stability.

Output offset cancellation

In Fig. 8.10 we illustrate the concept of input offset cancellation technique which requires a low-gain amplifier.

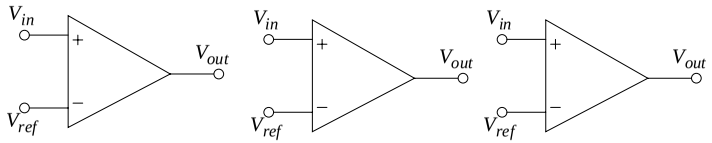

Figure 8.10: Output offset cancellation (a) with switches, (b) during phase 1, and (c) during phase 2.

On phase 1 both inputs are grounded as well as one of the capacitor plates. Therefore, we will at the output sample $A \cdot V_{os}$. On the second phase, the capacitor still holds this value and we will at the amplifier output have $A \cdot (V_{os} - V_{in})$, notice however, that at the other plate of the capacitor (i.e., the total output) we have the wanted output voltage:

$$V_{out} = A \cdot (V_{os} - V_{in}) - A \cdot V_{os} = -A \cdot V_{in}$$

This technique reduces the capacitive load at the input of the whole comparator. We also do not need any feedback. Third, since we have some gain in this amplifier, the clock feedthrough and offset in the following stages are relaxed by the gain of the first amplifier.

Latched comparators

In order to further increase the performance of the comparator, one can add a positive-feedback latch as a last stage. This requires that the output swing of the last pre-amplifier is large enough to be verified by the latch. In Fig. 8.11 this is illustrated. We have two phases, during the first

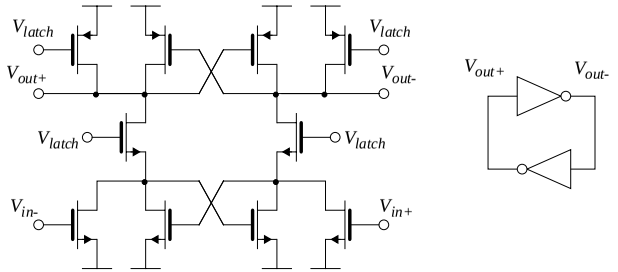

Figure 8.11: Positive-feedback track-and-latch. (a) Schematic and (b) in latch mode.

phase V_{latch} is low, and we precharge the latch. On the second phase, V_{latch} is high and the comparator operates as two inverters connected back-to-back. The output conductance of the inverters is given by the PMOS and NMOS transistor in parallel and the capacitive loads on the latch outputs are given by a number of CMOS gates. The transconductance is given by the g_m of the transistors. Typically, one can derive the settling time constant of the latch to

$$\tau_l = \frac{C_L}{g_m}$$

We know that the transconductance value is

$$g_m = \mu C_{ox} \cdot \frac{W}{L} \cdot V_{eff}$$

and the load capacitance is given by a number of gate-source capacitances:

$$C_L = nC_{ox} \cdot WL$$

We have the time constant given by

$$\tau_l = \frac{nC_{ox} \cdot WL}{\mu C_{ox} \cdot \frac{W}{L} \cdot V_{eff}} = \frac{n}{\mu} \cdot L^2 \cdot \frac{1}{V_{eff}}$$

Example on comparator

In Fig. 8.12 we illustrate a high-performance comparator that can be implemented in CMOS tech-

Figure 8.12: Example on a multi-stage discrete-time comparator with sample&hold, pre-amplifiers and positive-feedback latch.

nology.

Application of comparators

The comparators are widely used in A/D converters. In Fig. 8.13 we examplify this with a 3-bit flash A/D converter using 7 comparators.

Figure 8.13: Example on a 3-bit flash A/D converter.