TSEK37

Analog CMOS Integrated Circuits

Examination (TEN1)

Time:	14 Januari 2017 at 14.00 - 18.00
Place:	KÅRA
Responsible teacher:	Martin Nielsen-Lönn, ISY, 070-361 52 44 (martin.nielsen.lonn@liu.se)
	Will visit exam location at 15 and 17.
Number of tasks:	6
Number of pages:	6
Allowed aids:	Calculator, dictionary
Total points:	20
Notes:	Remember to indicate the steps taken when solving problems.
	Please start each new problem at the top of a page!
	Only use one side of each paper!
Exam presentation:	23 Januari 2017 at 12:00-13:00 in 3D:535, B-building

Grade	**Points**
U	<8
3	8 - <12
4	12 - <16
5	16 - 20

Questions

1) Consider the circuit shown in Fig. 1. Channel-length modulation and body effect can be neglected ($\lambda = 0$, $\gamma = 0$). Consider C_{gs} on M_2 but ignore the other parasitic capacitances, $C_L >> C_{gs}$.

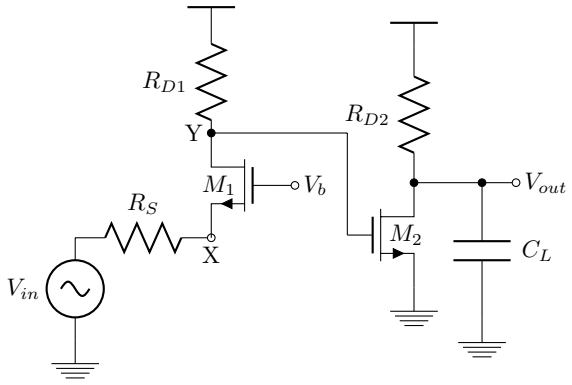

Figure 1: Schematic of a single-ended amplifier for problem 1.

(a) Draw the equivalent small-signal model and derive the expression for the transfer function in terms of the circuit component parameters. (3)

Also identify the DC voltage gain and pole(s) from the transfer function. You can assume that the poles are well separated.

(b) The amplifier has two poles. Assume that pole 1: $\omega_{p1} = 1$ krad/s, pole 2: $\omega_{p2} = 2$ Mrad/s, and unity gain frequency: $\omega_u = 2$ Mrad/s. What is the phase margin of the amplifier? (1)

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2) Consider the fully differential amplifier shown in Fig. 2. The amplifier is completely symmetric. Neglect body effect ($\gamma = 0$). However, channel-length modulation must be considered ($\lambda \neq 0$). The parasitic capacitance C_{gs} of the MOSFETs at nodes X, Y and the load capacitance C_L must be considered. Ignore other parasitic capacitances. Assume that $g_m \gg g_{ds}$.

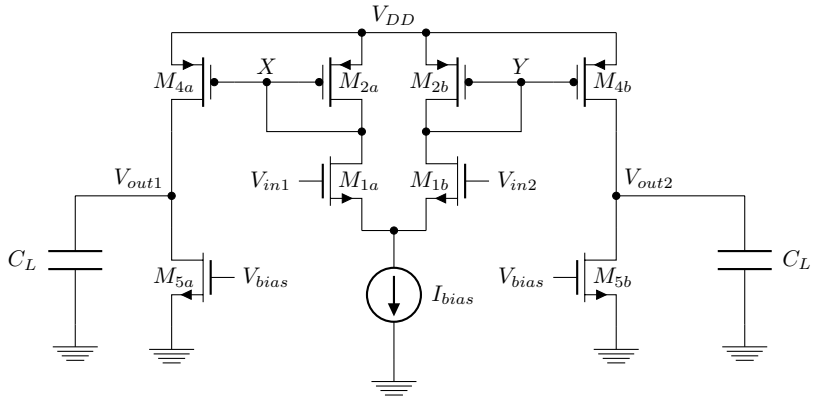

Figure 2: A fully differential amplifier.

(a) Draw the small-signal model of the amplifier shown in Fig. 2 and derive the transfer function in terms of the circuit component parameters. (2)

(b) Derive the expressions for the DC gain and the two pole frequencies. Assume that the dominant pole is formed by the load capacitor C_L and the poles are well separated, in that case what is the unity-gain frequency? (1)

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3) In Fig. 3 a current mirror circuit is shown. The aim is to copy the reference current I_{ref} to I_{out}.

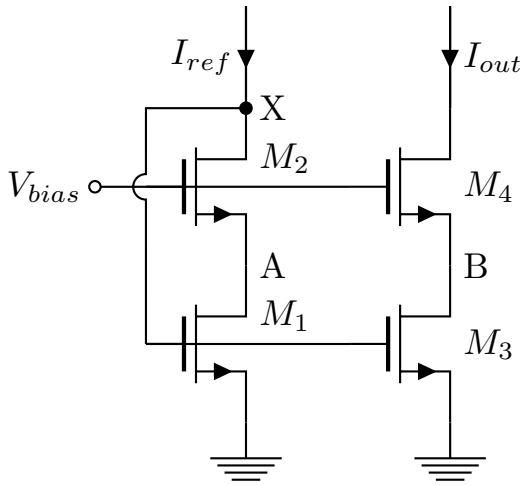

Figure 3: A low-voltage cascode current mirror.

(a) Derive the bounds for V_{bias} such that both M_1 and M_2 are in the saturation region. Give the answers in terms of V_{gs1}, V_{gs2}, V_{th1} and V_{th2}. (2)

(b) Using the lowest value for V_{bias} derived in part 1, determine the minimum allowable voltage at the output node to keep both M_3 and M_4 in the saturation region. Assume that $M_3 = M_1$ and $V_{gs4} = V_{gs2}$. Give the answer in terms of V_{gs3}, V_{gs4}, V_{th3} and V_{th4}. (1)

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4) Figure 4 shows a lossless interconnect circuit. At $t = 0$ the voltage step V_0 goes high and propagates a pulse through the circuit. Given the values below, calculate the voltage at nodes A, B and C at $t = 7$ ns. t_{d,Z_x} is the delay through transmission line Z_x. Assume that the inverters have a infinite (high) input impedance. (3)

$R_0 = 150\ \Omega$, $Z_0 = 150\ \Omega$, $Z_1 = 75\ \Omega$, $Z_2 = 50\ \Omega$, $t_{d,Z_0} = 2$ ns, $t_{d,Z_1} = 3$ ns and $t_{d,Z_2} = 4$ ns.

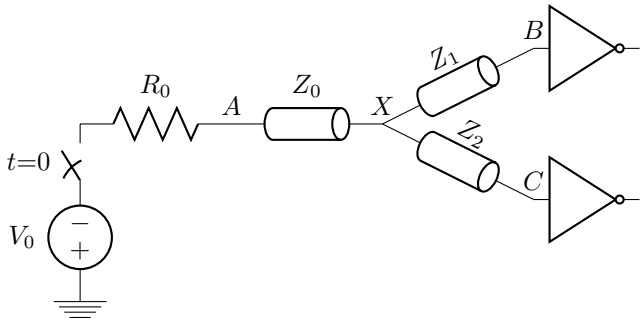


Figure 4: Transmission line circuit.

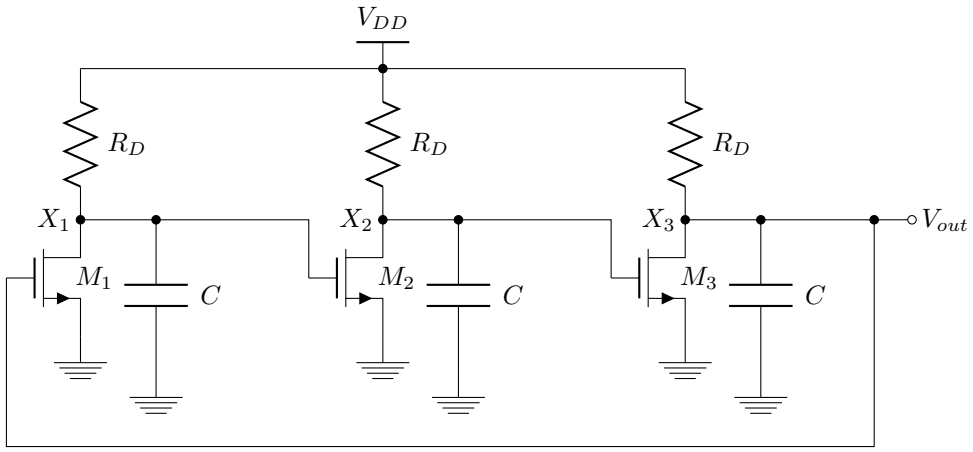


Figure 5: 3-stage ring oscillator

5) Fig. 5 shows a 3-stage ring oscillator with three identical amplifier stages. Ignore all parasitic capacitances, and assume transistor output resistance of r_o for M_1, M_2, and M_3.

   (a) Define the voltage gain and pole of each amplifier stage, and express the loop-gain transfer function of the oscillator. (1)

   (b) Assume $C = 1$ pF, $g_m = 1$ mA/V, and $r_o = 10$ kΩ.

      i. Find the value of the amplifier load resistance (R_D) for which the oscillation conditions (Barkhausen criteria) are exactly (just) fulfilled. (2½)

      ii. Find the oscillation frequency (ω_{osc}). (½)

   Hint:

   - Barkhausen criteria: $|H(j\omega)| = 1$ and $\angle\beta H(j\omega) = -180°$.
   - At oscillation each stage contributes with $-60°$ frequency-dependent phase shift (total $-180°$), thus: $\arctan(\omega_{osc}/\omega_p) = 60°$ and $\omega_{osc}/\omega_p = \sqrt{3}$.

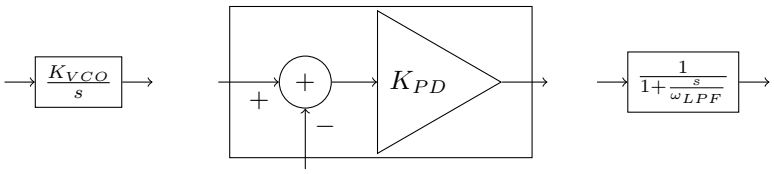
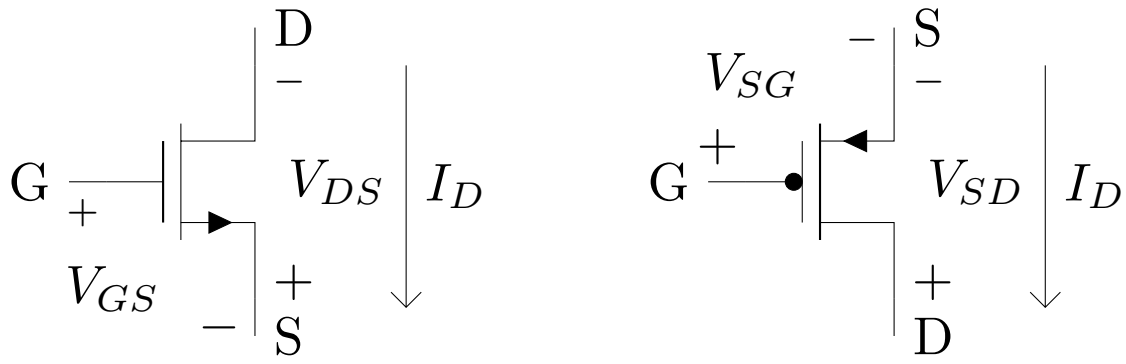


Figure 6: Linear models for Voltage Controlled Oscillator, Phase Detector, and Low-Pass Filter.

6) (a) Design a PLL by using the components in Fig. 6, and calculate the loop-gain of the PLL. (1)

   (b) Calculate the ω_{LPF} under the assumption that the PLL has ZERO phase-margin with $-180°$ phase shift at $\omega = 10\omega_{LPF}$. Here: $K_{VCO} = 100\ \frac{\text{rad}}{\text{Vs}}$ and $K_{PD} = 5$ V/rad. (2)

Transistor equations



(a) NMOS (b) PMOS

NMOS

Cutoff $I_D = 0$ $(V_{GS} < V_{TN})$

Linear mode

$I_D = \mu_n C_{ox} \frac{W}{L} \left((V_{GS} - V_{TN}) V_{DS} - \frac{V_{DS}^2}{2} \right)$ $(V_{GS} > V_{TN})$ and $(V_{DS} < V_{GS} - V_{TN})$

Saturation mode

$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TN})^2 (1 + \lambda V_{DS})$ $(V_{GS} > V_{TN})$ and $(V_{DS} > V_{GS} - V_{TN})$

PMOS

Cutoff $I_D = 0$ $(V_{SG} < |V_{TP}|)$

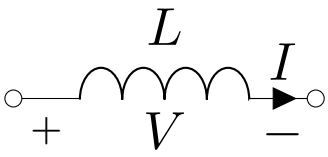
Linear mode

$I_D = \mu_p C_{ox} \frac{W}{L} \left((V_{SG} - |V_{TP}|) V_{SD} - \frac{V_{SD}^2}{2} \right)$ $(V_{SG} > |V_{TP}|)$ and $(V_{SD} < V_{SG} - |V_{TP}|)$

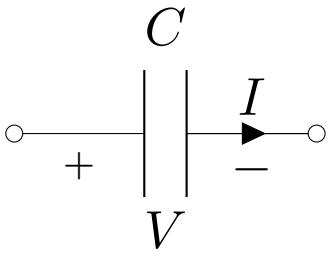
Saturation mode

$I_D = \frac{1}{2} \mu_p C_{ox} \frac{W}{L} (V_{SG} - |V_{TP}|)^2 (1 + \lambda V_{SD})$ $(V_{SG} > |V_{TP}|)$ and $(V_{SD} > V_{SG} - |V_{TP}|)$

Transmission line equations



(a) Inductor



(b) Capacitor

Complex characteristic impedance

$$Z_c = \sqrt{\frac{R+j\omega L}{G+j\omega C}}$$

Characteristic impedance for lossless TL

$$Z_0 = \sqrt{\frac{L}{C}}$$

Inductance voltage-current relation

$$V = L\frac{dI}{dt}$$

Capacitance voltage-current relation

$$I = C\frac{dV}{dt}$$

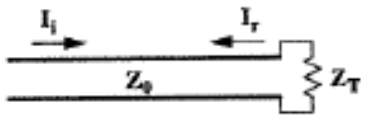
Mutual inductance

$$V_{mn} = L_{mn}\frac{dI_n}{dt} \text{ where } m \neq n$$

Telegrapher's Equation

Reflection Coefficient

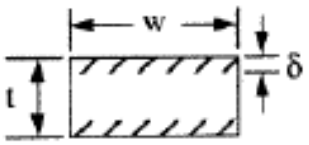
$$k_r = \frac{V_r}{V_i} = \frac{I_r}{I_i} = \frac{Z_T - Z_0}{Z_T + Z_0}$$

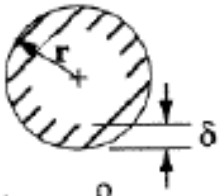


Skin Effect

Skin Depth

$$\delta = \frac{1}{\sqrt{\pi f \mu \sigma}}$$





Skin Depth Frequency

$$f_s = \frac{\rho}{\pi \mu (t/2)^2} \qquad f_s = \frac{\rho}{\pi \mu r^2}$$

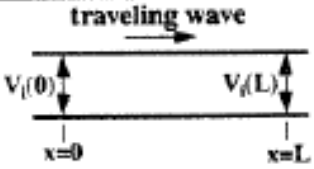
Skin Depth Resistance

$$R(f) = \frac{\sqrt{\pi f \mu \rho}}{2w} = R_{DC}\left(\frac{f}{f_s}\right)^{1/2} \qquad R(f) = \frac{\sqrt{f\mu\rho/\pi}}{2r} = \frac{R_{DC}}{2}\left(\frac{f}{f_s}\right)^{1/2}$$

Attenuation in Lossy Line

Attenuation

$$\frac{V_i(L)}{V_i(0)} = \exp[-(\alpha_R + \alpha_D)L] = \exp\left[-\left(\frac{R}{2Z_0} + \frac{GZ_0}{2}\right)L\right]$$



Conductor Loss

$$\alpha_R(f) = \frac{R_{DC}}{4Z_0}\left(\frac{f}{f_s}\right)^{1/2} \text{ (Round)} \qquad \alpha_R(f) = \frac{R_{DC}}{2Z_0}\left(\frac{f}{f_s}\right)^{1/2} \text{ (Strip)}$$

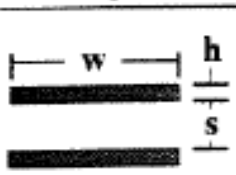
Dielectric Loss (Homogeneous)

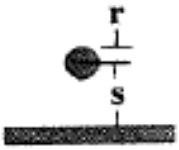
$$\alpha_D(f) = \frac{\pi\sqrt{\varepsilon_r}\tan\delta}{c} f$$

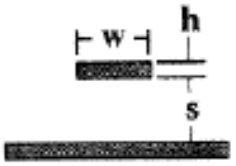
Dielectric Loss Tangent

$$\tan\delta = \frac{G}{\omega C} = \frac{\sigma_{Diel}}{\omega \varepsilon_r}$$

R,C,Z_0 for Various Geometries (Homogeneous Dielectric, $L = \varepsilon\mu/C$)







$R_{DC} = 2\frac{\rho}{wh}$	$R_{DC} = \frac{\rho}{\pi r_1^2} + \frac{\rho}{\pi(r_3^2 - r_2^2)}$	$R_{DC} = \frac{2\rho}{\pi r^2}$	$R_{DC} = \frac{\rho}{\pi r^2}$	$R_{DC} = \frac{\rho}{wh}$
$C = \frac{\varepsilon w}{s}$	$C = \frac{2\pi\varepsilon}{\log(r_2/r_1)}$	$C = \frac{\pi\varepsilon}{\log(s/r)}$	$C = \frac{\pi\varepsilon}{\log(2s/r)}$	$C = \frac{\varepsilon w}{s} + \frac{2\pi\varepsilon}{\log(s/w)}$
$Z_0 = \sqrt{\frac{\mu}{\varepsilon}}\frac{s}{W}$	$Z_0 = \sqrt{\frac{\mu}{\varepsilon}}\frac{\log(r_2/r_1)}{2\pi}$	$Z_0 = \sqrt{\frac{\mu}{\varepsilon}}\frac{\log(s/r)}{\pi}$	$Z_0 = \sqrt{\frac{\mu}{\varepsilon}}\frac{\log(2s/r)}{\pi}$	$Z_0 = \frac{\sqrt{\varepsilon\mu}}{C}$