TSEK37 Analog CMOS Integrated Circuits

EXAMINATION (TEN1)

Time:	16 January 2016 at 14.00 - 18.00
Place:	G32
Responsible teacher:	Martin Nielsen-Lönn, ISY, 070-361 52 44 (martin.nielsen.lonn@liu.se)
	Will visit exam location at 15 and 17.
Number of tasks:	6
Number of pages:	7
Allowed aids:	Calculator, dictionary
Total points:	20
Notes:	Remember to indicate the steps taken when solving problems.
	Please start each new problem at the top of a page!
	Only use one side of each paper!
Exam presentation:	22 Januari 2016 at 12:00-13:00 in 3D:535, B-building
	Grade Points
	U <8
	3 8 - <12

4

5

12 - <16

16 - 20

Questions

1) Consider the circuit shown in Fig. 1.

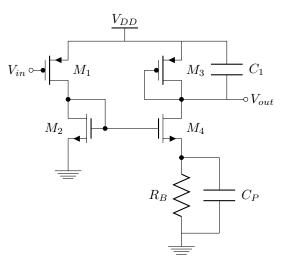


Figure 1: Schematic of a circuit.

- (a) Draw the equivalent small-signal model and derive the expression for the transfer function and from (3) that transfer function identify the DC voltage gain, pole(s) and zero(s). Neglect channel-length modulation and body effect ($\lambda = 0, \gamma = 0$). Ignore all parasitic capacitances except C_p and C_1 .
- (b) For the circuit in Fig. 1, let the unity-gain frequency $\omega_{ug} = 20$ krad/s, the dominant pole $\omega_{p1} = (1)$ 1 krad/s and the phase margin PM = 55°. Determine the value of the non-dominant pole ω_{p2} . Ignore the effect of the zero(s) on the PM.

2) Consider the fully differential amplifier shown in Fig. 2. The amplifier is completely symmetric. Neglect body effect ($\gamma = 0$). However, channel-length modulation must be considered ($\lambda \neq 0$). The parasitic capacitance C_{gs} of the MOSFETs at nodes X, Y and the load capacitance C_L must be considered. Ignore other parasitic capacitances. Assume that C_{gs} of $M_{4a,4b} = B \times C_{gs}$ of $M_{2a,2b}$, $g_{m4a,4b} = B \times g_{m2a,2b}$ and $g_m \gg g_{ds}$. B is an adjustable parameter.

(c) If the factor B is increased, how will the non-dominant pole and unity-gain frequency change? It is $(\frac{1}{2})$ assumed that the dominant pole is formed by the load capacitor C_L .

⁽a) Draw the small-signal model of the amplifier shown in Fig. 2 and derive the transfer function. $(2\frac{1}{2})$

⁽b) Derive the expressions for the DC gain, the two pole frequencies and the unity-gain frequency. It (1) is assumed that the dominant pole is formed by the load capacitor C_L .

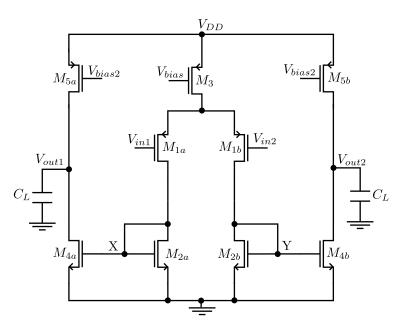


Figure 2: A fully differential amplifier.

3) In Fig. 3 a wide-swing cascode current mirror is shown. The aim here is to copy the reference current I_1 to I_2 . Assume that all transistors are in saturation and have the same threshold voltage. Neglect body effect and channel-length modulation. The transistor M_2 is designed to be at the edge of the saturation region to have the maximum voltage swing at the output node. What should be the value of n such that $I_1 = I_2$?

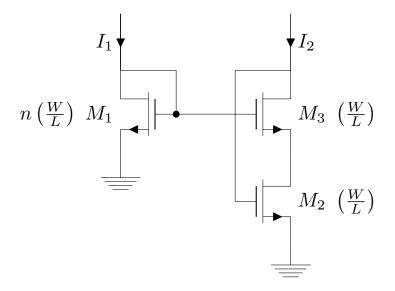


Figure 3: A wide-swing cascode current mirror.

(3)

4) Figure 4 shows a lossless interconnect circuit. At t = 0 the voltage step V_0 goes high and propagates a pulse through the circuit. Given the values below, calculate the voltage at nodes A, B and C at t = 7 ns. t_{d,Z_x} is the delay through transmission line Z_x . Assume that the inverters have a infinite (high) input impedance.

 $R_0 = 150 \ \Omega, \ Z_0 = 150 \ \Omega, \ Z_1 = 75 \ \Omega, \ Z_2 = 50 \ \Omega, \ t_{d,Z_0} = 2 \ \text{ns}, \ t_{d,Z_1} = 3 \ \text{ns} \ \text{and} \ t_{d,Z_2} = 4 \ \text{ns}.$

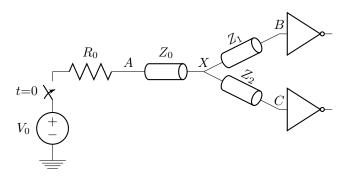


Figure 4: Transmission line circuit.

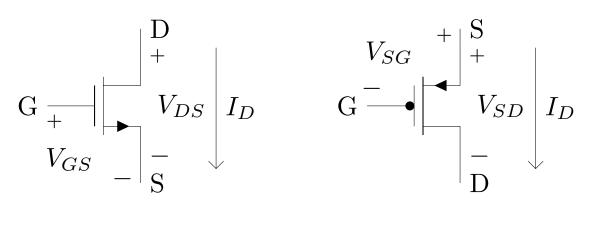
- 5) Assume that an inverter stage can be approximated as a first order circuit with a single pole at ω_0 and a stage DC-gain of -A.
 - (a) What are the possible number of stages required to construct a ring oscillator and what is the minimum number assuming each stage is made using a single-ended inverter? How would this change if differential inverters are used instead and why?
 - (b) Draw such a ring oscillator with a minimum amount of stages. Derive the open-loop transfer (1) function for this ring oscillator.
 - (c) Calculate the minimum required voltage gain per stage in order to have oscillation and how this $(1\frac{1}{2})$ gain requirement changes with the number of stage, N.
 - (d) Assume that the ring oscillator has settled into its steady state which occurs when the output signals $\binom{1}{2}$ starts to swing from roughly 0 to roughly V_{DD} . At this point the propagation delay of each stage is $t_{p,s}$. What is the output frequency if we have N number of stages?

- 6) A PLL type I contains a low-pass filter, phase detector and VCO.
 - (a) Draw the block diagram of the PLL, derive the total transfer function as $H(s) = \frac{\theta_{out}(s)}{\theta_{in}(s)}$ and show (1¹/₂) that θ_{out} is equal to θ_{in} when θ_{in} is constant.

$$H_{PD}(s) = K_{PD}[\theta_{in}(s) - \theta_{out}(s)]$$
$$H_{LP}(s) = \frac{1}{1 + \frac{s}{\omega_{p1}}}$$
$$H_{VCO}(s) = \frac{K_{VCO}}{s}$$

(b) A PLL can be used to multiply a frequency. Assume that the PLL is supposed to generate a $\binom{1}{2}$ frequency of 1 GHz from a 250 MHz clock. Modify and insert additional needed blocks in the block diagram to implement this behaviour.

Transistor equations



(a) NMOS

(b) PMOS

NMOS

Cutoff

$$(V_{GS} < V_{TN})$$

Linear mode

$$I_D = \mu_n C_{ox} \frac{W}{L} \left((V_{GS} - V_{TN}) V_{DS} - \frac{V_{DS}^2}{2} \right) \quad (V_{GS} > V_{TN}) \text{ and } (V_{DS} < V_{GS} - V_{TN})$$

Saturation mode

 $I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TN})^2 (1 + \lambda V_{DS}) \quad (V_{GS} > V_{TN}) \text{ and } (V_{DS} > V_{GS} - V_{TN})$

PMOS

Cutoff $I_D = 0$ $(V_{SG} < |V_{TP}|)$

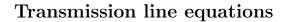
 $I_D = 0$

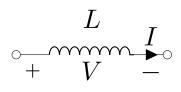
Linear mode

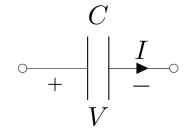
$$I_D = \mu_p C_{ox} \frac{W}{L} \left((V_{SG} - |V_{TP}|) V_{SD} - \frac{V_{SD}^2}{2} \right) \quad (V_{SG} > |V_{TP}|) \text{ and } (V_{SD} < V_{SG} - |V_{TP}|)$$

Saturation mode

$$I_D = \frac{1}{2}\mu_p C_{ox} \frac{W}{L} (V_{SG} - |V_{TP}|)^2 (1 + \lambda V_{SD}) \quad (V_{SG} > |V_{TP}|) \text{ and } (V_{SD} > V_{SG} - |V_{TP}|)$$







(a) Inductor



Complex characteristic impedance

Characteristic impedance for lossless TL

$$Z_c = \sqrt{\frac{R+j\omega L}{G+j\omega C}}$$

$$Z_0 = \sqrt{\frac{L}{C}}$$

Inductance voltage-current relation

Capacitance voltage-current relation

$$V = L \frac{dI}{dt}$$

$$I = C \frac{dV}{dt}$$

Mutual inductance

 $V_{mn} = L_{mn} \frac{dI_n}{dt}$ where $m \neq n$

