TSEK37

Analog CMOS Integrated Circuits

Examination (TEN1)

Time:	10 April 2015 at 8.00 - 12.00
Place:	U1
Resonsible teacher:	Martin Nielsen-Lönn, ISY, 070-361 52 44 (martin.nielsen.lonn@liu.se)
	Will visit exam location at 8:45 and 10:30.
Number of tasks:	6
Number of pages:	7
Allowed aids:	Calculator, dictionary
Total points:	20
Notes:	Remember to indicate the steps taken when solving problems.
	Please start each new problem at the top of a page!
	Only use one side of each paper!
Exam presentation:	17 April 2015 at 12:00-13:00 in Filtret, B-house

Grade	**Points**
U	<8
3	8 - <12
4	12 - <16
5	16 - 20

Questions

1) Consider the simple differential amplifier shown in Fig. 1. The tail current source has a finite output resistance R_{SS}. The input transistors M_1 and M_2 have a transconductance of g_m. Neglect channel-length modulation and body effect ($\lambda = 0$, $\gamma = 0$).

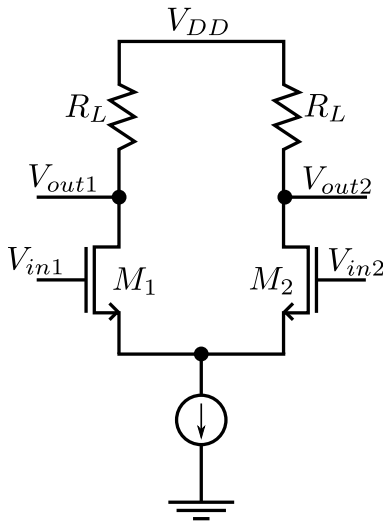

Figure 1: A simple differential amplifier.

(a) Derive the expression for the common-mode (CM) gain of the circuit. (2)

(b) Let $R_L = 10$ kΩ, $g_m = 2$ mS, and $R_{SS} = 1$ kΩ. If the input CM voltage level increases by 25 mV, what will be the change in voltage level at the outputs V_{out1} and V_{out2}? (1)

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2) Consider the fully-differential amplifier shown in Fig. 2. The amplifier is completely symmetric. Neglect body effect ($\gamma = 0$). However, channel-length modulation must be considered ($\lambda \neq 0$). At nodes X, Y consider only the C_{gs} capacitances of the MOSFETs. The devices M_3, M_4, M_5, and M_6 have equal C_{gs}. Ignore other parasitic capacitances.

(a) Draw the small-signal model of the amplifier shown in Fig. 2 and derive the transfer function. (2)

(b) Derive the expressions for the DC gain, the two pole frequencies and the unity-gain frequency. Assume $g_m \gg g_{ds}$. Also assume that the dominant pole is formed at the output node of the amplifier. (2)

(c) Let the unity-gain frequency of the amplifier = 1 Mrad/s and the dominant pole frequency = 100 krad/s. What should be the minimum frequency of the non-dominant pole in order to maintain a phase margin (PM) $\geq 60°$? (1)

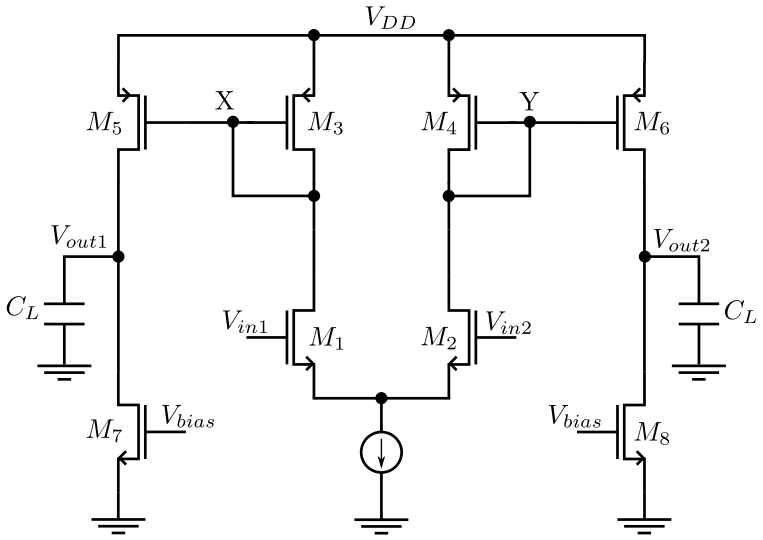

Figure 2: A fully-differential amplifier.

$\mu_n C_{ox}$	300 $\mu A/V^2$
λ_n	0.1 V^{-1}
γ_n	0
V_{t0n}	0.45 V
V_{DD}	1.2 V

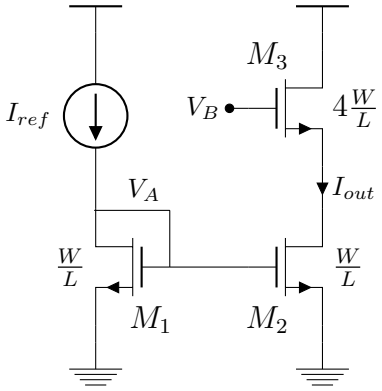

Figure 3: Cascode current mirror.

3) In Fig. 3 a cascode current mirror is shown. The aim here is to copy the reference current I_{ref} to I_{out}. Assume that $V_A = 0.6$ V, what should V_B be then to make $I_{ref} = I_{out}$? (3)

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4) Figure 4 shows a lossless interconnect circuit. At $t = 0$ the voltage step V_0 goes high and propagates a pulse through the circuit. Given the values below, calculate the voltage at nodes A and B at $t = 10$ ns. t_{d,Z_x} is the delay through transmission line Z_x. Assume that the inverters have a infinite (high) input impedance. (3)

$R_0 = 75\ \Omega$, $Z_0 = 75\ \Omega$, $Z_1 = 25\ \Omega$, $t_{d,Z_0} = 2$ ns and $t_{d,Z_1} = 2.5$ ns.

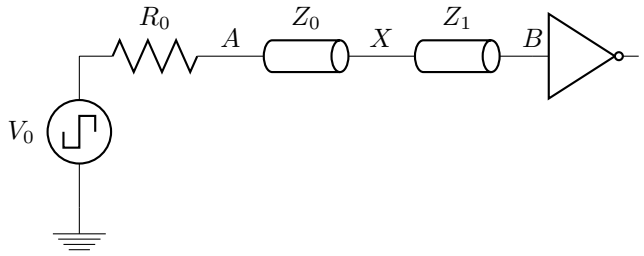

Figure 4: Transmission line circuit.

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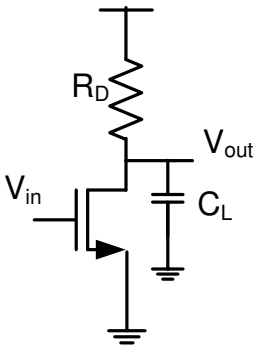
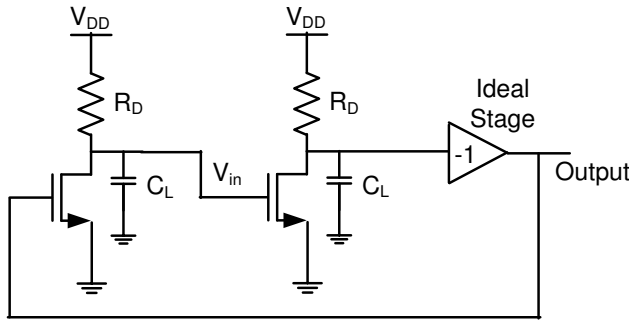
5) The common-source amplifier stage shown in Fig. 5a is used in a ring oscillator consisting of five stages.



(a) Common-source stage used in the ring oscillator.



(b) 3-stage circuit

Figure 5

(a) Calculate the oscillation frequency in terms of R_D and C_L. (1)

(b) Calculate the minimum DC gain, A_0 per stage required to sustain the oscillations. (2)

(c) The common-source amplifier is now used in a 3-stage circuit as shown in Fig. 5b. Assuming that the last stage is an ideal inverting stage with no dependence on frequency, can this circuit be used as an oscillator? Clearly explain your answer. (1)

Neglect any transistor capacitances and short-channel effects in all your calculations.

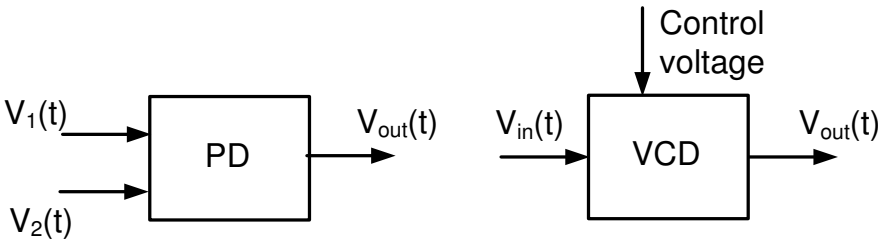


Figure 6: Available components.

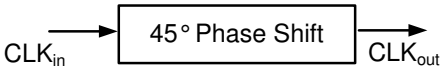


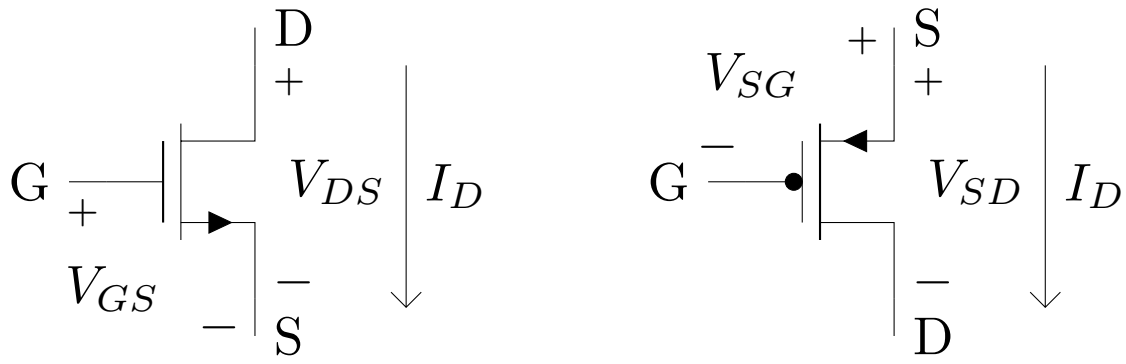
Figure 7: Clock Generator.

6) Assume that you have access to the following two components shown in Fig. 6. (2)

- An ideal Phase detector (PD).
- Many ideal Voltage Control Delay elements (VCD).

Use these two components to construct a clock phase generator that accepts an input clock, CLK_{in} and generates an output clock CLK_{out} having the same frequency as CLK_{in} but with a phase shift of 45° as shown in Fig. 7.

Transistor equations



(a) NMOS (b) PMOS

NMOS

Cutoff $I_D = 0$ $(V_{GS} < V_{TN})$

Linear mode

$I_D = \mu_n C_{ox} \frac{W}{L} \left((V_{GS} - V_{TN}) V_{DS} - \frac{V_{DS}^2}{2} \right)$ $(V_{GS} > V_{TN})$ and $(V_{DS} < V_{GS} - V_{TN})$

Saturation mode

$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TN})^2 (1 + \lambda V_{DS})$ $(V_{GS} > V_{TN})$ and $(V_{DS} > V_{GS} - V_{TN})$

PMOS

Cutoff $I_D = 0$ $(V_{SG} < |V_{TP}|)$

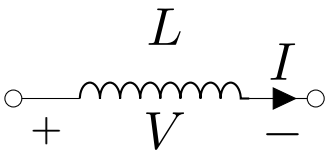
Linear mode

$I_D = \mu_p C_{ox} \frac{W}{L} \left((V_{SG} - |V_{TP}|) V_{SD} - \frac{V_{SD}^2}{2} \right)$ $(V_{SG} > |V_{TP}|)$ and $(V_{SD} < V_{SG} - |V_{TP}|)$

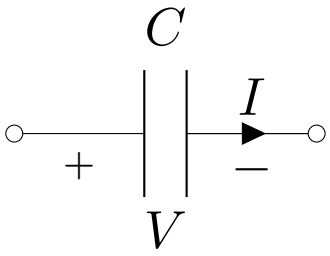
Saturation mode

$I_D = \frac{1}{2} \mu_p C_{ox} \frac{W}{L} (V_{SG} - |V_{TP}|)^2 (1 + \lambda V_{SD})$ $(V_{SG} > |V_{TP}|)$ and $(V_{SD} > V_{SG} - |V_{TP}|)$

Transmission line equations



(a) Inductor



(b) Capacitor

Complex characteristic impedance

$$Z_c = \sqrt{\frac{R+j\omega L}{G+j\omega C}}$$

Characteristic impedance for lossless TL

$$Z_0 = \sqrt{\frac{L}{C}}$$

Inductance voltage-current relation

$$V = L\frac{dI}{dt}$$

Capacitance voltage-current relation

$$I = C\frac{dV}{dt}$$

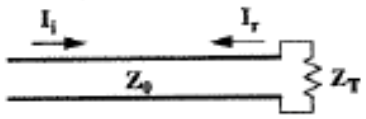
Mutual inductance

$$V_{mn} = L_{mn}\frac{dI_n}{dt} \text{ where } m \neq n$$

Telegrapher's Equation

Reflection Coefficient

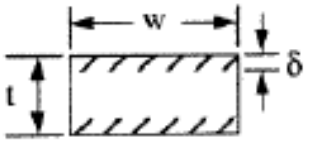
$$k_r = \frac{V_r}{V_i} = \frac{I_r}{I_i} = \frac{Z_T - Z_0}{Z_T + Z_0}$$

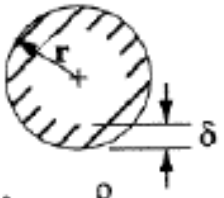


Skin Effect

Skin Depth

$$\delta = \frac{1}{\sqrt{\pi f \mu \sigma}}$$





Skin Depth Frequency

$$f_s = \frac{\rho}{\pi \mu (t/2)^2} \qquad f_s = \frac{\rho}{\pi \mu r^2}$$

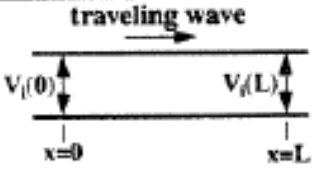
Skin Depth Resistance

$$R(f) = \frac{\sqrt{\pi f \mu \rho}}{2w} = R_{DC}\left(\frac{f}{f_s}\right)^{1/2} \qquad R(f) = \frac{\sqrt{f\mu\rho/\pi}}{2r} = \frac{R_{DC}}{2}\left(\frac{f}{f_s}\right)^{1/2}$$

Attenuation in Lossy Line

Attenuation

$$\frac{V_i(L)}{V_i(0)} = \exp[-(\alpha_R + \alpha_D)L] = \exp\left[-\left(\frac{R}{2Z_0} + \frac{GZ_0}{2}\right)L\right]$$



Conductor Loss

$$\alpha_R(f) = \frac{R_{DC}}{4Z_0}\left(\frac{f}{f_s}\right)^{1/2} \text{ (Round)} \qquad \alpha_R(f) = \frac{R_{DC}}{2Z_0}\left(\frac{f}{f_s}\right)^{1/2} \text{ (Strip)}$$

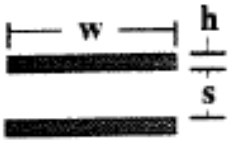
Dielectric Loss (Homogeneous)

$$\alpha_D(f) = \frac{\pi\sqrt{\varepsilon_r}\tan\delta}{c} f$$

Dielectric Loss Tangent

$$\tan\delta = \frac{G}{\omega C} = \frac{\sigma_{Diel}}{\omega \varepsilon_r}$$

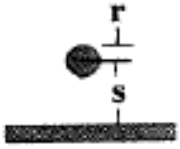
R,C,Z_0 for Various Geometries (Homogeneous Dielectric, $L = \varepsilon\mu/C$)



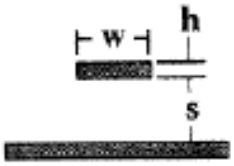
$$R_{DC} = 2\frac{\rho}{wh} \qquad C = \frac{\varepsilon w}{s} \qquad Z_0 = \sqrt{\frac{\mu}{\varepsilon}}\frac{s}{W}$$

$$R_{DC} = \frac{\rho}{\pi r_1^2} + \frac{\rho}{\pi(r_3^2 - r_2^2)} \qquad C = \frac{2\pi\varepsilon}{\log(r_2/r_1)} \qquad Z_0 = \sqrt{\frac{\mu}{\varepsilon}}\frac{\log(r_2/r_1)}{2\pi}$$

$$R_{DC} = \frac{2\rho}{\pi r^2} \qquad C = \frac{\pi\varepsilon}{\log(s/r)} \qquad Z_0 = \sqrt{\frac{\mu}{\varepsilon}}\frac{\log(s/r)}{\pi}$$



$$R_{DC} = \frac{\rho}{\pi r^2} \qquad C = \frac{\pi\varepsilon}{\log(2s/r)} \qquad Z_0 = \sqrt{\frac{\mu}{\varepsilon}}\frac{\log(2s/r)}{\pi}$$



$$R_{DC} = \frac{\rho}{wh} \qquad C = \frac{\varepsilon w}{s} + \frac{2\pi\varepsilon}{\log(s/w)} \qquad Z_0 = \frac{\sqrt{\varepsilon\mu}}{C}$$