# ExAMINATION IN 

TSEK37/TEN1

## Analog CMOS Integrated Circuits

Date: 2013-03-27<br>Time: 8-12<br>Location: U7-U10<br>Aids: Calculator, Dictionary<br>Teachers: Behzad Mesgarzadeh (5719)<br>Daniel Svärd (8946)

8 points are required to pass.

Please start each new problem at the top of a page! Only use one side of each paper!

1) Figure 1 shows a differential amplifier. The amplifier is completely symmetric, i.e. $M_{1}=M_{2}, M_{3}=M_{4}$ and $M_{5}=M_{6}$. Assume $\lambda \neq 0$ and $\gamma=0$.
(a) Draw the low-frequency small-signal model of the circuit.
(b) Derive an expression for the DC gain.
(c) What kind of circuit element do $\mathrm{M}_{5}$ and $\mathrm{M}_{6}$ realize?


Fig. 1. Differential amplifier.
2) A cascode current mirror is shown in Fig. 2. If $V_{Y}=1 V$, determine $V_{b}$ to have a perfect mirror $\left(\mathrm{I}_{\mathrm{out}}=\mathrm{I}_{\mathrm{ref}}\right)$. Assume that all transistors are long channel transistors.

$$
\begin{align*}
& \mu_{\mathrm{n}} \mathrm{C}_{\mathrm{ox}}=250 \mu \mathrm{~A} / \mathrm{V}^{2}  \tag{3p}\\
& \lambda_{\mathrm{n}}=0.1 \mathrm{~V}^{-1} \\
& \gamma_{\mathrm{n}}=0 \\
& \mathrm{~V}_{\mathrm{t} 0 \mathrm{n}}=0.5 \mathrm{~V} \\
& \mathrm{~V}_{\mathrm{dd}}=2 \mathrm{~V}
\end{align*}
$$



Fig. 2. Cascode current mirror.
3) Transimpedance amplifiers are commonly used in optical receiver circuits. This type of amplifier converts an input current, $\mathrm{i}_{\mathrm{in}}$, into a voltage, $\mathrm{v}_{\text {out }}$. Figure 3 shows an example circuit implementation of such an amplifier. For all subproblems, neglect all capacitances except $C_{X}$ and $C_{L}$; and assume $\lambda \neq 0$ and $\gamma \neq 0$.
(a) Draw the small-signal model of the amplifier.
(b) Derive an expression for the transfer function, $\mathrm{R}(\mathrm{s})=\mathrm{v}_{\mathrm{out}} / \mathrm{i}_{\mathrm{in}}$, of the amplifier. Identify the DC transimpedance and the two poles.
(c) Calculate the DC transimpedance and the location of the poles given the bias conditions in Fig. 3.
$\mu_{\mathrm{n}} \mathrm{C}_{\mathrm{ox}}=160 \mu \mathrm{~A} / \mathrm{V}^{2}$
$\mathrm{L}=0.35 \mu \mathrm{~m}$
$\mathrm{W}_{1}=\mathrm{W}_{2}=35 \mu \mathrm{~m}$
$\lambda_{\mathrm{n}}=0.1 \mathrm{~V}^{-1}$
$\gamma_{\mathrm{n}}=0.4 \mathrm{~V}^{1 / 2}$
$\mathrm{V}_{\mathrm{t} 0 \mathrm{n}}=0.5 \mathrm{~V}$
$2 \Phi_{\mathrm{F}}=0.9 \mathrm{~V}$
$\mathrm{V}_{\mathrm{dd}}=3.3 \mathrm{~V}$
$\mathrm{I}_{1}=500 \mu \mathrm{~A}$
$\mathrm{I}_{2}=2 \mathrm{~mA}$
$\mathrm{R}_{\mathrm{D} 1}=2 \mathrm{k} \Omega$
$\mathrm{R}_{\mathrm{D} 2}=500 \Omega$
$\mathrm{R}_{\mathrm{S}}=2 \mathrm{k} \Omega$
$\mathrm{C}_{\mathrm{X}}=0.25 \mathrm{pF}$
$\mathrm{C}_{\mathrm{L}}=2 \mathrm{pF}$


Fig. 3. Transimpedance amplifier.
4) Estimate the propagation delay of a $2-\mathrm{mm}$ wire with a high-frequency characteristic impedance of $50 \Omega$ and resistance per length of $r=5 \mathrm{~K} \Omega / \mathrm{m}$ and dielectric constant $\varepsilon_{r}=4$.
5) A 3-stage ring oscillator is shown in Fig. 4. Assume that all of the transistors are identical and ignore their parasitics. Calculate the phase margin of this circuit. Assume $\mathrm{R}=3.5 \mathrm{~K} \Omega, \mathrm{C}=1 \mathrm{pF}, g_{m}=1 \mathrm{~mA} / \mathrm{V}$, and $\mathrm{r}_{\mathrm{o}}=10 \mathrm{~K} \Omega$.


Fig. 4. A three-stage ring oscillator.
6) Assume you have access to the following components:

- An ideal Phase-Detector (PD), shown in Fig. 5(a).
- Many ideal Voltage-Controlled Delay elements (VCD), such as the one shown in Fig. 5(b).


Fig. 5(a)
Fig. 5(b)
Use the abovementioned components and design a clock phase generator (Fig. 5(c)) which receives a periodic clock signal $\left(\mathrm{Clk}_{\text {in }}\right)$ with an arbitrary frequency, and generates a clock signal $\left(\mathrm{Clk}_{\text {out }}\right)$ with the same frequency but with 90 degree phase shift.


Fig. 5(c)

## TRANSISTOR EQUATIONS



## NMOS

- Cutoff: $\quad \mathrm{I}_{\mathrm{D}}=0 \quad\left(\mathrm{~V}_{\mathrm{GS}}<\mathrm{V}_{\mathrm{TN}}\right)$
- Linear mode:
$I_{D}=\mu_{n} C_{o x} \frac{W}{L}\left(\left(V_{G S}-V_{T N}\right) V_{D S}-\frac{V_{D S}^{2}}{2}\right) \quad\left(\mathrm{V}_{\mathrm{GS}}>\mathrm{V}_{\mathrm{TN}}\right)$ and $\left(\mathrm{V}_{\mathrm{DS}}<\mathrm{V}_{\mathrm{GS}}-\mathrm{V}_{\mathrm{TN}}\right)$
- Saturation mode:

$$
I_{D}=\frac{1}{2} \mu_{n} C_{o x} \frac{W}{L}\left(V_{G S}-V_{T N}\right)^{2}\left(1+\lambda V_{D S}\right) \quad\left(\mathrm{V}_{\mathrm{GS}}>\mathrm{V}_{\mathrm{TN}}\right) \text { and }\left(\mathrm{V}_{\mathrm{DS}}>\mathrm{V}_{\mathrm{GS}}-\mathrm{V}_{\mathrm{TN}}\right)
$$

## PMOS

- Cutoff: $\quad \mathrm{I}_{\mathrm{D}}=0 \quad\left(\mathrm{~V}_{\mathrm{GS}}<\left|\mathrm{V}_{\mathrm{TP}}\right|\right)$
- Linear mode:

$$
I_{D}=\mu_{p} C_{o x} \frac{W}{L}\left(\left(V_{S G}-\left|V_{T P}\right|\right) V_{S D}-\frac{V_{S D}^{2}}{2}\right) \quad\left(\mathrm{V}_{\mathrm{GS}}>\left|\mathrm{V}_{\mathrm{TP}}\right|\right) \text { and }\left(\mathrm{V}_{\mathrm{SD}}<\mathrm{V}_{\mathrm{SG}}-\left|\mathrm{V}_{\mathrm{TP}}\right|\right)
$$

- Saturation mode:

$$
I_{D}=\frac{1}{2} \mu_{p} C_{o x} \frac{W}{L}\left(V_{S G}-\left|V_{T P}\right|\right)^{2}\left(1+\lambda V_{S D}\right) \quad\left(\mathrm{V}_{\mathrm{GS}}>\left|\mathrm{V}_{\mathrm{TP}}\right|\right) \text { and }\left(\mathrm{V}_{\mathrm{SD}}>\mathrm{V}_{\mathrm{SG}}-\left|\mathrm{V}_{\mathrm{TP}}\right|\right)
$$

## TRANSMISSION LINE EQUATIONS

- Complex characteristic impedance
$Z_{c}=\sqrt{\frac{R+j \omega L}{G+j \omega C}}$
- Inductance voltage-current relation:
$V=L \frac{d I}{d t}$
- Characteristic impedance for lossless TL:

$$
Z_{o}=\sqrt{\frac{L}{C}}
$$

- Capacitance voltage-current relation:
$I=C \frac{d V}{d t}$

- Mutual inductance:
$V_{m n}=L_{m n} \frac{d I_{n}}{d t}$ where $\mathrm{m} \neq \mathrm{n}$


