## **EXAMINATION IN**

# TSEK37/TEN1

## ANALOG CMOS INTEGRATED CIRCUITS

Date:	2012-12-22
Time:	8-12
Location:	U4-U7-U10
Aids:	Calculator, Dictionary
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8 points are required to pass.

### Please start each new problem at the top of a page! Only use one side of each paper!

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(1 p)

- 1) Fig. 1 shows a differential amplifier. In this circuit, the amplifier is completely symmetric and all transistors are operating in saturation.
- (a) Determine  $V_b$  to have a bias level of  $V_{DD}/2$  at the output node. (2 p)
- (b) Compute the ratio  $g_{m1}/g_{m5}$ .



Fig. 1. Differential amplifier circuit.

2) A regulated-cascode amplifier is shown in Fig. 2. Assume that all transistors are biased in the saturation region and that  $I_B$  is an ideal current source. Neglect the body effect and assume  $\lambda \neq 0$ .



Fig. 2. Regulated-cascode amplifier.

- (a) Draw the small-signal model of the amplifier. (1 p)
- (b) Derive an expression for the DC-gain.

(2 p)

**3)** A fully differential two-stage amplifier is shown in Fig. 3. For simplicity, we can ignore all parasitics of  $M_1$ - $M_8$  and we assume that the dominant pole occurs at the output node due to load capacitor *C*. Neglect the body effect (i.e.,  $\gamma=0$ ) and assume  $\lambda\neq 0$ .



Fig. 3. A two-stage differential amplifier.

- (a) Draw the small-signal model of the two-stage amplifier and derive the AC transfer function  $(V_{out}/V_{in})(s)$ . (2 p)
- (b) Identify the DC gain and the pole? (1 p)
- (c) Calculate the unity-gain frequency  $f_u$ ? (1 p)
- 4) An RC-wire with length of *d* is devided into *m* equal-length sections and *m* repeaters are inserted between sections as shown in Fig. 4. Assume that the propagation delay of each repeater is  $t_p$  and D(m) represents the total delay of wire including repeaters. We have measured the total delay for two cases when the wire is devided into 6 and 8 sections and we have obtained  $D(8)-D(6)=4t_p/3$ . Determine the required number of sections to get optimum delay through this wire. (4 p)

*Hint:* The delay through an RC wire is  $0.38rcd^2$ , where d is wire length and r and c are resistance and capacitance per unit length.





5) A 4-stage ring oscillator (with identical stages) utilizes a differential inverter as it is shown in Fig. 5. We assume that this inverter is completely symmetric and all parasitics are neglected except the output capacitance of each stage (i.e., C). Determine the minimum of R required to start the oscillation according to Barkhausen criteria. Assume also that  $g_{m_1} = g_{m_2} = 1 \ mV/A$ , and  $\lambda = \gamma = 0$ . (4 p)



Fig. 5. A differential inverter.

6) An XOR gate is utilized as phase detector in a DLL. When the phase deference between the input and the output of the DLL is 225°, draw the waveforms related to the phase detector and calculate its average output voltage. Assume that the waveforms are ideal square waves with full swing between 0 and 3 V. (2 p)

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 $< V_{GS}$  -  $V_{TN}$ )

#### **TRANSISTOR EQUATIONS**





#### **NMOS**

- **Cutoff:**
- Linea

Linear mode:  

$$I_D = \mu_n C_{ox} \frac{W}{L} \left( (V_{GS} - V_{TN}) V_{DS} - \frac{V_{DS}^2}{2} \right) \qquad (V_{GS} > V_{TN}) \text{ and } (V_{DS} - V_{TN})$$

Saturation mode: ٠

$$I_{D} = \frac{1}{2} \mu_{n} C_{ox} \frac{W}{L} (V_{GS} - V_{TN})^{2} (1 + \lambda V_{DS}) \qquad (V_{GS} > V_{TN}) \text{ and } (V_{DS} > V_{GS} - V_{TN})$$

 $I_D = 0 \qquad (V_{GS} < V_{TN})$ 

#### **PMOS**

- $I_{\rm D} = 0$ 137 **Cutoff:** ٠
- Linear mode: .

$$(V_{\rm GS} < |V_{\rm TP}|)$$

$$I_{D} = \mu_{p} C_{ox} \frac{W}{L} \left( \left( V_{SG} - |V_{TP}| \right) V_{SD} - \frac{V_{SD}^{2}}{2} \right) \qquad (V_{GS} > |V_{TP}|) \text{ and } (V_{SD} < V_{SG} - |V_{TP}|)$$

**Saturation mode:** ٠

$$I_{D} = \frac{1}{2} \mu_{p} C_{ox} \frac{W}{L} (V_{SG} - |V_{TP}|)^{2} (I + \lambda V_{SD}) \qquad (V_{GS} > |V_{TP}|) \text{ and } (V_{SD} > V_{SG} - |V_{TP}|)$$

#### **TRANSMISSION LINE EQUATIONS**

• Complex characteristic impedance

$$Z_c = \sqrt{\frac{R + j\omega L}{G + j\omega C}}$$

• Inductance voltage-current relation:

$$V = L \frac{dI}{dt}$$

• Characteristic impedance for lossless TL:

$$Z_0 = \sqrt{\frac{L}{C}}$$

• Capacitance voltage-current relation:

$$I = C \frac{dV}{dt}$$

С

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• Mutual inductance:

$$V_{mn} = L_{mn} \frac{dI_n}{dt}$$
 where m  $\neq$  n

