# ExAMINATION IN 

TSEK37/TEN1

## Analog CMOS Integrated Circuits

Date: 2012-04-13<br>Time: 14-18<br>Location: TER2<br>Aids: Calculator, Dictionary<br>Teachers: Behzad Mesgarzadeh (5719)<br>Ali Fazli (2794)<br>Daniel Svärd (8946)

8 points are required to pass.

Please start each new problem at the top of a page! Only use one side of each paper!

1) A current mirror circuit is shown in Fig. 1. If properly sized, this circuit can realize accurate mirroring with a high output impedance while consuming low voltage headroom.


Fig. 1. Current mirror.
(a) Derive the bounds on $\mathrm{V}_{\mathrm{b}}$ such that $\mathrm{M}_{1}$ and $\mathrm{M}_{2}$ are in the saturation region. Determine the restriction on the sizing of $\mathrm{M}_{2}$ for this to be possible. Give the answers in terms of $\mathrm{V}_{\mathrm{GS} 1}, \mathrm{~V}_{\mathrm{GS} 2}, \mathrm{~V}_{\mathrm{TH} 1}$ and $\mathrm{V}_{\mathrm{TH} 2}$.
(b) Using the lowest value of $\mathrm{V}_{\mathrm{b}}$ from (a), determine the minimum allowable voltage at node P to keep $M_{3}$ and $M_{4}$ in saturation. Assume that $M_{3}=M_{1}$ and that the transistors are sized such that $\mathrm{V}_{\mathrm{GS} 4}=\mathrm{V}_{\mathrm{GS} 2}$. Give the answer in terms of $\mathrm{V}_{\mathrm{GS} 3}, \mathrm{~V}_{\mathrm{GS} 4}, \mathrm{~V}_{\mathrm{TH} 3}$ and $V_{\text {TH4 }}$.
2) An amplifier with a DC gain of $\mathrm{A}_{0}$ and poles at 1 MHz and 450 MHz is connected in a feedback loop with a gain of 4 (i.e. the feedback factor ( $\beta$ ) is $1 / 4$ ). Compute the value of $\mathrm{A}_{0}$ such that the phase margin is $60^{\circ}$.

Hint: $\arctan u+\arctan v=\arctan \left(\frac{u+v}{1-u v}\right)(\bmod \pi), \quad u v \neq 1$
3) A fully differential current-mirror amplifier is shown in Fig. 2. The bias current of the device $\mathrm{M}_{4}$ is mirrored $B$ times to the output stage, i.e. $\mathrm{I}_{\mathrm{D} 4}=\mathrm{B} \times \mathrm{I}_{\mathrm{D} 2}$. A local positive feedback composed of transistors $\mathrm{M}_{3}$ and $\mathrm{M}_{3 \mathrm{~b}}$ is used to enhance the DC gain.


Fig. 2. Current mirror amplifier.
(a) Disregard the positive feedback containing $\mathrm{M}_{3}-\mathrm{M}_{3 \mathrm{~b}}$ devices and draw the smallsignal model. Determine the DC gain in terms of the transconductance $g_{m}$, the conductance $g_{d s}$, and the mirroring ratio $B$. Assume that $\gamma=0$.
(b) Consider the positive feedback and derive the DC gain expression. How can the DC gain be enhanced by sizing of the transistors $\mathrm{M}_{3}$ and $\mathrm{M}_{3 \mathrm{~b}}$ ?
(c) Consider the current-mirror amplifier as a two-pole system and that it is frequency compensated by the load capacitor $\mathrm{C}_{\mathrm{L}}$, rather than miller capacitor. Also, assume that the second pole (non-dominate) occurs in the gate of the transistors $\mathrm{M}_{2}, \mathrm{M}_{3 \mathrm{~b}}$, and $\mathrm{M}_{4}$. Derive the approximate expressions for the two poles.
(1 p)
4) A lossless interconnect is shown in Fig. 3. At time 0 , the voltage step of $V_{0}$ drives a transmission line that is splitted into different sections, each driving an inverter with a high impedance input. With the impedance given below, calculate the voltage at A, B and C at the time instant 7.5 ns .
$\mathrm{R}_{0}=75 \Omega, \mathrm{Z}_{0}=75 \Omega, \mathrm{Z}_{1}=150 \Omega$, and $\mathrm{Z}_{2}=50$.


Fig. 3. A transmition-line circuit.
5) Assume that the output of a voltage-controlled oscillator (VCO) is a sinusoidal as it is shown in Fig. 4. In this figure, $\omega_{0}$ is the output frequency when $\mathrm{V}_{\text {cont }}=0, \mathrm{~K}_{\mathrm{VCO}}$ is the gain of the VCO, and $\mathrm{V}_{\text {cont }}$ is the control voltage of the VCO. Now Assume that we apply a small sinusoidal control voltage to this VCO (i.e., $V_{\text {cont }}=V_{m} \cos \left(\omega_{m} t\right)$ ). If $\mathrm{V}_{\mathrm{m}}$ is small enough to satisfy $K_{V C O} V_{m} \ll \omega_{m}$ and $\omega_{m}<\omega_{0}$, draw the output spectrum of the VCO. Motivate your answer by presenting the details of your calculations. We can assume that the VCO characteristic is linear.


Fig. 4. A voltage-controlled oscillator.
6) A PLL type I with $\zeta=0.1$ is utilized to generate a $200-\mathrm{MHz}$ carrier frequency. If $\omega_{L P F}=2 \pi \times 28.6 \mathrm{KHz}$ and the output is to be changed from 201 MHz to 201.5 MHz , how long does it take in the worst-case for the PLL to settle within 100 Hz of its final value?

Hint: The step response of a PLL type I with underdamped response is as:
$\omega_{\text {out }}(t)=\left\{1-\frac{1}{\sqrt{1-\zeta^{2}}} \cdot e^{-\zeta \omega_{n} t} \sin \left(\omega_{n} \sqrt{1-\zeta^{2}} t+\theta\right)\right\} \Delta \omega u(t)$
where
$2 \zeta \omega_{n}=\omega_{L P F}$

## TRANSISTOR EQUATIONS

NMOS


PMOS


## NMOS

- Cutoff: $\quad \mathrm{I}_{\mathrm{D}}=0 \quad\left(\mathrm{~V}_{\mathrm{GS}}<\mathrm{V}_{\mathrm{TN}}\right)$
- Linear mode:

$$
I_{D}=\mu_{n} C_{o x} \frac{W}{L}\left(\left(V_{G S}-V_{T N}\right) V_{D S}-\frac{V_{D S}^{2}}{2}\right) \quad\left(\mathrm{V}_{\mathrm{GS}}>\mathrm{V}_{\mathrm{TN}}\right) \text { and }\left(\mathrm{V}_{\mathrm{DS}}<\mathrm{V}_{\mathrm{GS}}-\mathrm{V}_{\mathrm{TN}}\right)
$$

- Saturation mode:

$$
I_{D}=\frac{1}{2} \mu_{n} C_{o x} \frac{W}{L}\left(V_{G S}-V_{T N}\right)^{2}\left(1+\lambda V_{D S}\right) \quad\left(\mathrm{V}_{\mathrm{GS}}>\mathrm{V}_{\mathrm{TN}}\right) \text { and }\left(\mathrm{V}_{\mathrm{DS}}>\mathrm{V}_{\mathrm{GS}}-\mathrm{V}_{\mathrm{TN}}\right)
$$

## PMOS

- Cutoff:

$$
\mathrm{I}_{\mathrm{D}}=0 \quad\left(\mathrm{~V}_{\mathrm{GS}}<\left|\mathrm{V}_{\mathrm{TP}}\right|\right)
$$

- Linear mode:

$$
I_{D}=\mu_{p} C_{o x} \frac{W}{L}\left(\left(V_{S G}-\left|V_{T P}\right|\right) V_{S D}-\frac{V_{S D}^{2}}{2}\right) \quad\left(\mathrm{V}_{\mathrm{GS}}>\left|\mathrm{V}_{\mathrm{TP}}\right|\right) \text { and }\left(\mathrm{V}_{\mathrm{SD}}<\mathrm{V}_{\mathrm{SG}}-\left|\mathrm{V}_{\mathrm{TP}}\right|\right)
$$

- Saturation mode:

$$
I_{D}=\frac{1}{2} \mu_{p} C_{o x} \frac{W}{L}\left(V_{S G}-\left|V_{T P}\right|\right)^{2}\left(1+\lambda V_{S D}\right) \quad\left(\mathrm{V}_{\mathrm{GS}}>\left|\mathrm{V}_{\mathrm{TP}}\right|\right) \text { and }\left(\mathrm{V}_{\mathrm{SD}}>\mathrm{V}_{\mathrm{SG}}-\left|\mathrm{V}_{\mathrm{TP}}\right|\right)
$$

## TRANSMISSION LINE EQUATIONS

- Complex characteristic impedance
$Z_{c}=\sqrt{\frac{R+j \omega L}{G+j \omega C}}$
- Inductance voltage-current relation:
$V=L \frac{d I}{d t}$
- Characteristic impedance for lossless TL:

$$
Z_{o}=\sqrt{\frac{L}{C}}
$$

- Capacitance voltage-current relation:
$I=C \frac{d V}{d t}$

- Mutual inductance:
$V_{m n}=L_{m n} \frac{d I_{n}}{d t}$ where $\mathrm{m} \neq \mathrm{n}$


