Exercies for Tutorial 6: Timing issues

1. Assume that an inverter stage can be approximated as a first-order circuit with a single pole at ω_0 and a stage gain of $-A$. Determine the open-loop transfer function of a 5-stage ring oscillator. Calculate the minimum required voltage gain per stage in order to have oscillation.

$$H(s) = -\frac{A^5}{\left(1+\frac{s}{\omega_o}\right)^5},\ A_{min} = 1.23$$

2. A voltage-controlled oscillator with linear tuning characteristic has a gain of $2\pi \times 10^8 \frac{rad}{s}/V$. The control voltage varies between 0 and $3\ V$. When the control voltage is $0.5\ V$, the oscillation frequency is $1\ GHz$. Calculate the required control voltage to get $1.25\ GHz$ oscillation frequency.

$$V_{cont} = 2.5\ V$$

3. Consider the PLL loop filter circuit shown in Figure 13. Determine the transfer function $G(s)$ of this filter. The op-amp is ideal.

$$G(s) = -\frac{1+sR_1C}{sR_2C}$$

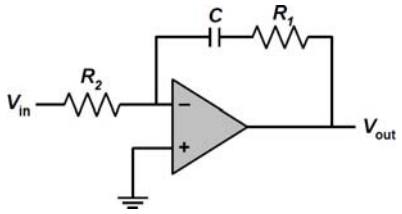

Figure 13 Loop filter circuit.

4. A block diagram of a PLL is shown in Figure 14. φ_{in} is the reference phase and φ_{out} is the output of the oscillator. The following relations can be identified:

$$V_1 = K_{PD}(\varphi_{in} - \varphi_{out})$$
$$\frac{d\varphi_{out}}{dt} = K_{VCO}V_2$$

a) Determine the closed-loop transfer function of the PLL from φ_{in} to φ_{out}. Use the loop filter transfer function $G(s)$ in problem 3.

$$H(s) = -\frac{K_{PD}K_{VCO}(1+sR_1C)}{s^2R_2C - K_{PD}K_{VCO}(1+sR_1C)}$$

b) What are the necessary conditions on K_{PD} and K_{VCO} for stability?

$$K_{PD}K_{VCO} < 0$$

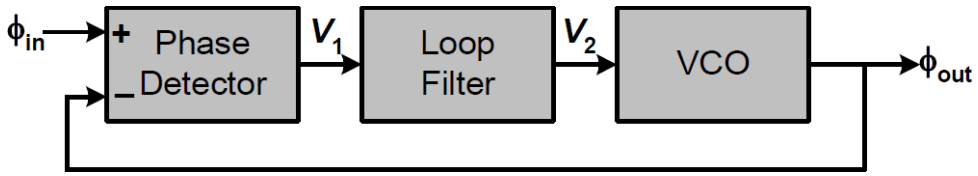

Figure 14 PLL block diagram.