VLSI Chip Design Project TSEK06

Project Description and Requirement Specification

Version 1.1

Project: High Speed Serial Link Transceiver

Project number: 4

Project Group:

Name	Project members	Telephone	E-mail
	Project leader and designer 1(5)		
	Designer 2(5)		
	Designer 3(5)		
	Designer 4(5)		
	Designer 5(5)		

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1 Background

This document describes the design requirement specification of a high speed serial link transceiver. Serial link interfaces are used to transmit high speed data on a single link to avoid skew issues when transmitting parallel words. The receiver must be able to extract the clock from the transmitted data and use this to successfully sample the incoming data. Coding is often used to guarantee a certain amount of transitions on the data line for the clock extraction to work, and for the decoding to work correct, detection of the word boundaries will be necessary.

1.1 Project Goal

The project goal is to design an integrated circuit (IC) in complementary metal-oxide semiconductor (CMOS) technology. Students, participating in this project as project members and project leaders, should learn the different steps of the IC design flow. That includes the analysis of the given system architecture, simulation, layout implementation and verification. The project students have an optional choice to manufacture the designed circuit on a chip. To test the manufactured chips, another course (TSEK11) is available after the project.

1.2 Milestones and Deadline

1: Project selection	Week 4
2: Pre-study, project planning, and discussion with supervisor	Week 5
3: High-level modeling design and simulation result (report)	February 15
4: Gate/transistor level design and simulations result (report)	March 11
5: Layout, DRC, parasitic extraction, LVS, post-layout simulations, modification and chip evaluations.	May 11
6: **DEADLINE**, Delivery of the completed chip.	**May 13**
7: **DEADLINE**, Final report, and oral presentation	**May 23**

1.3 Parties

The following parties are involved in this project:

1) Customer: Vishnu Unnikrishnan

2) Project supervisor: Vishnu Unnikrishnan
   Tasks:
   - Formulates the project requirements
   - Provides technical support
   - Reviews the project documents.

3) Project leader: One of the members in the design team.
   Tasks:
   - Responsible for organization of the team and the project planning
   - Divides the design and documentation work in an efficient way
   - Organizes the team meetings as well as the meetings between the team and supervisor

- Keeps the supervisor informed about the progress of the project (**at least one email or meeting per week**)

4) Project design members (including the project leader)

- Are equally responsible for project planning and design
- Participate actively in all the meetings
- Support the team and the project leader
- Keep the team and project leader informed about the progress of their tasks.

2 Project Description

2.1 System Description

The complete system to be built, as seen in Figure 1, should be a working serial link transceiver. The transmitter sends random data words over the link and after processed by the receiver the recovered words should be compared against the transmitted words in order to estimate the word error rate at high throughputs.

The transmitter should be able to send out a continuous stream of random data words or the so called comma symbols (sync words) at any given time. The comma words are used by the receiver to both estimate the optimal sampling point as well as to detect the beginning/end of the transmitted words. The data/comma transmission can be either implemented as two externally controlled modes of operation or, alternatively (recommended approach), comma words could be periodically inserted in the data stream to make the data transfer more robust and self-healing in case the synchronization is lost. The 8-bit data words are to be coded to 10-bit words with an 8b10b encoder in order to control the DC signal level on the channel and guarantee enough signal transitions that helps the clock recovery.

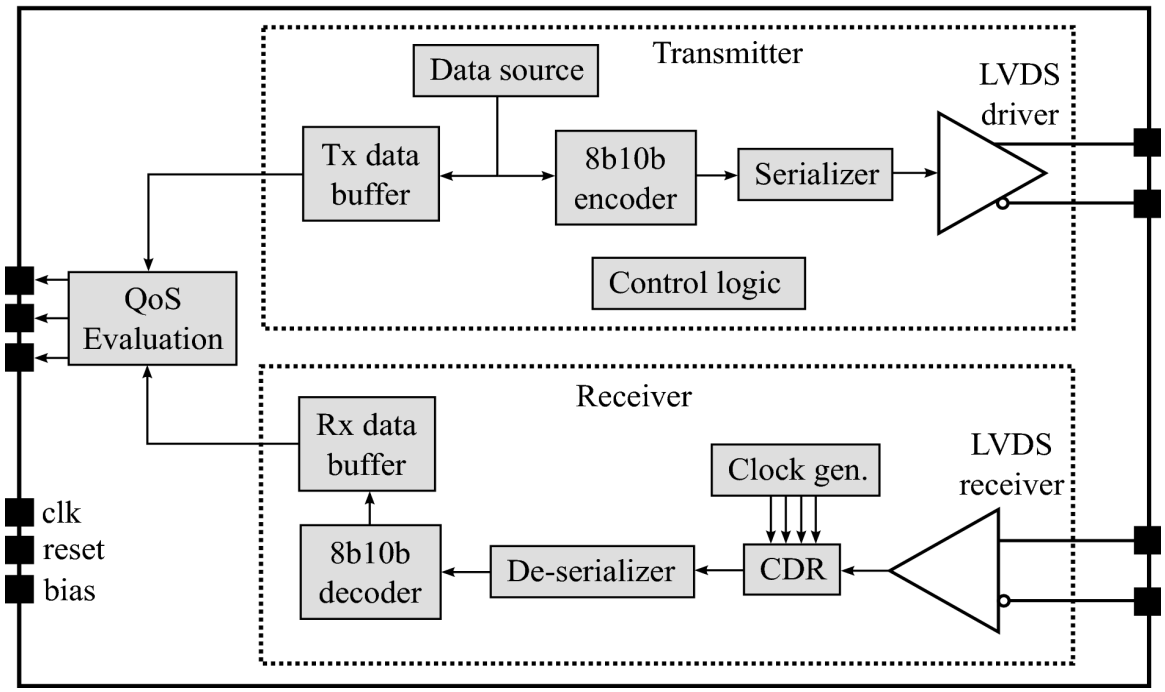

Figure 1: High speed serial link transceiver system overview.

The receiver works by oversampling the incoming data by a factor of 4. From these samples, the rising and the falling edges are detected and an optimal sampling instance is decided upon. The optimal sampling point is continuously calculated and up-dated for every bit such that the system dynamically adapts to the drift and momentary bit length variations resulting from inter-symbol interference. With the help of the comma sequences/symbols the correct word boundaries are detected. The 10 bit words are then either passed to the 8b10b decoder to generate an estimate of the 8b data originally transmitted if the received word is a data symbol or an internal control signal is generated if the received word is a comma symbol.

Once data is sent from the transmitter and received, they are checked for parity errors (compliance to 8b10b encoding) and then the received word is compared to the transmitted words. A successful reception indicated by a match, is communicated to the outside world through a pulse transmitted at an IO pin. In case the received word do not match the transmitted word, error codes can be sent as pulses, that helps resolve between different possible error scenarios. The pulses could also indicate a comma reception in case a periodic comma insertion is implemented. The hit pulses and the error pulses can be used to estimate the word error rate as a function of the data rate.

2.2 Important Design Metrics

The design target for this project is to reach a data rate, limited by the on-chip clock frequency at around 500 Mbit/s over a 10 cm PCB track. Lower data rates should also be supported over longer network cables.

During comma transmission mode the detection of comma sequences should cause pulses on one of the output pins. During data mode, pulses should be sent out if the received word matches the transmitted, otherwise the diagnostic pin states should indicate the type fault. These pulses are used to calculate the word error rate.

The purposes for the twelve pins in the project can be found in the table below.

Pins	Pin description
1,2	Differential output
3,4	Differential input
5	Clock input
6	VDD
7	VSS
8,9,10	Diagnostic output
11	Bias to control output drive strength
12	Reset

2.3 Design details

The details of the receiver architecture is shown in Figure 2. The incoming data is oversampled by a factor of 4 using a multi-phase clock and the 'Select phase' block determines the correct clock phase for data sampling, based on the location of the rising and falling data edges. The concept of the phase selection is shown in Figure 3 showing how to calculate the optimal sampling instance depending on the transition points. This will compensate for skew and duty ratio variations of the incoming serial data sequence.

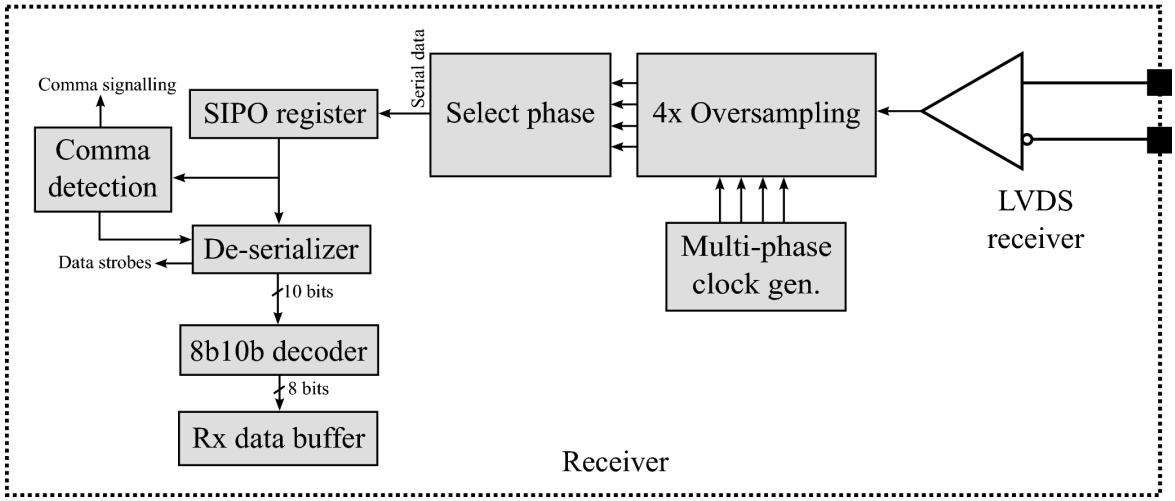

Figure 2: Detailed receiver architecture.

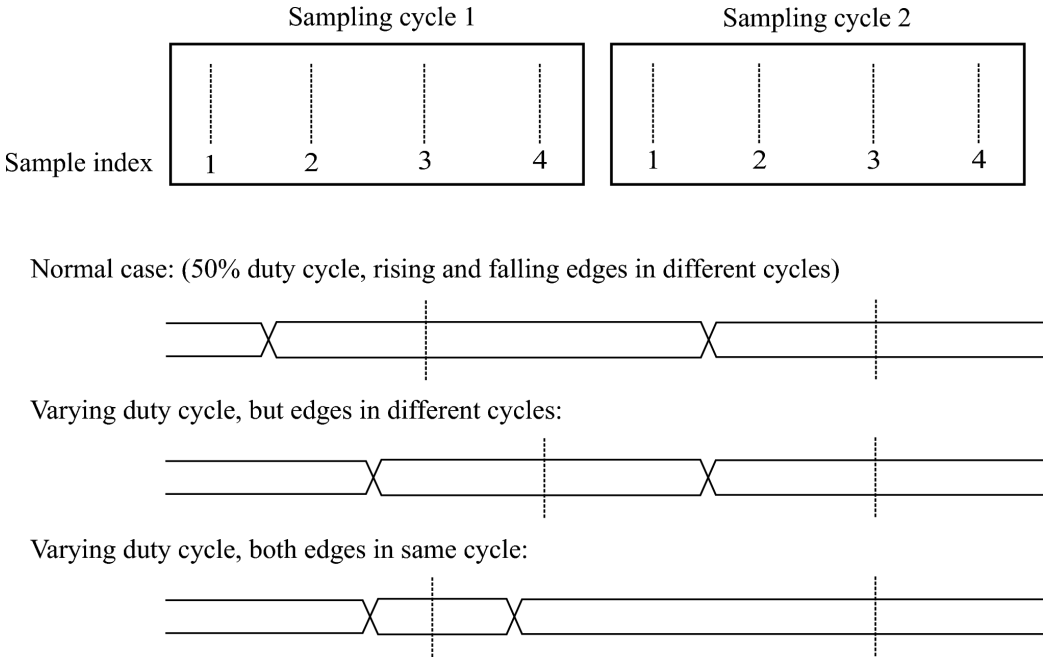

Figure 3: Oversampling data recovery by cycle-to-cycle selection of optimal sampling phase, which adapts to dynamic variations in skew and duty cycle.

3 Area and Performance Requirements

The table below summarizes the circuit performance requirements. Each requirement has its number, formulated text, and the given degree of priority. Three degrees of priority are used: high, medium, and low. High is a firm requirement with no possibility of relaxation, while medium requirements can be relaxed somewhat after good motivation.

Requirement	Requirement text	Priority
1	Data rate of 500 Mbit/s	Medium
2	Burst of comma transmission following system reset	High
3	Periodic comma insertion in the data stream	High
4	Comply with LVDS standard	Medium
5	Integrate as many system components as possible on-chip	High
6	Diagnostic output enabling calculation of error-free data rate as well as resolution of fault type in case of error transmissions	High
7	Function and timing verification of schematic and layout	High
8	Chip core area < 0.27 mm^2	Medium
9	Total project pin count <= 12	High
10	Technology is AMS 4-Metal 0.35-µm CMOS	High
11	The most important system nodes should have off-chip access	Medium
12	On-chip current densities < 1 mA/µm	Medium
13	All requirements fulfilled in *"typical"*, *"slow"*, and *"fast"* process corners and for temperatures between 25°C and 110°C	Medium

4 Available Resources

- Material given by the supervisor
- IEEE Xplore digital library, http://ieeexplore.ieee.org/, access given through LiU

4.1 Tools

- Circuit simulation and layout tools from Cadence, http://www.cadence.com/

4.2 References

- http://analog.postech.ac.kr/1.Nrl/2.NRL%20Seminar/invitation/040514_KangJG.pdf
- http://en.wikipedia.org/wiki/8b/10b_encoding - contains good tables for 8b10b coding.
- J.M. Rabaey, A. Chandrakasan, and B. Nikolic., "Digital Integrated Circuits", 2nd ed.,
- Prentice Hall, 2003, ISBN 0-13-120764-4.

For more literature references consult with your supervisor.