VLSI Chip Design Project TSEK06

Project description and requirement specification

Version 1.0

Project: PLL-based Binary Frequency Shift-Keying (BFSK) Modulator

Project number: 8

Project Group:

Name	Project members	Telephone	E-mail
	Project leader and designer 1(5)		
	Designer 2(5)		
	Designer 3(5)		
	Designer 4(5)		
	Designer 5(5)		

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1 Background

This document describes the design requirement specification of a Phased Lock Loop (PLL), which is going to be used as a binary frequency shift-keying (BFSK) modulator. A PLL is a circuit that synchronizes an output signal generated by an oscillator, with a reference signal in both frequency and phase. The PLL has a control loop that regulates the oscillator frequency so that the phase error is kept small. A PLL can be used as a frequency multiplier, which multiplies the frequency of an input signal with some ratio. If we alternate the multiplication factor between different values a FSK modulator can be built.

1.1 Project goal

The project goal is to design an integrated circuit (IC) in complementary metal-oxide semiconductor (CMOS) technology. Students, participating in this project as project members and project leaders, should learn the different steps of the IC design flow. That includes the given system architecture analysis, simulation, layout implementation and verification. The project students have an optional choice to manufacture the designed IC circuit on a chip. To test the manufactured chips, another course (TSEK11) is available after the project.

1.2 Milestones and deadline

1: Project selection	Week 3
2: Pre-study, project planning, and discussion with supervisor	Week 4
3: High-level modeling design and simulation result (report)	February 12
4: Gate/transistor level design and simulations result (report)	March 18
5: Layout, DRC, parasitic extraction, LVS, post-layout simulations, modification and chip evaluations.	May 6
6: **DEADLINE**, Delivery of the completed chip.	**May 13**
7: **DEADLINE**, Final report, and oral presentation	**May 20**

1.3 Parties

The following parties are involved in this project:

1- Customer: Omid E. Najari

2- Project supervisor: Omid E. Najari

   Tasks:

- Formulates the project requirements
- Provides technical support
- Reviews the project documents

3- Project leader: One of the members in the design team.

Tasks:

- Responsible for organization of the team and the project planning.
- Divides the design and documentation work in an efficient way
- Organizes the team meetings as well as the meetings between the team and supervisor
- Keeps the supervisor informed about the progress of the project **(at least one e-mail or meeting per week)**

4- Project design members (including the project leader)
- Are equally responsible for project planning and design.
- Participate actively in all the meetings
- Support the team and the project leader
- Keep the team and project leader informed about the progress of their tasks.

2 Project description

2.1 System description

A block schematic of a PLL is shown in Figure 1. The PLL will receive a reference clock (*Ref*) from an external source (crystal or other). A phase-detector (PD) will compare the phase of the reference with the pre-scaled version of the RF clock (*ClkRF*). The outputs of the phase detector are up/down signals. The up/down signals controls a charge-pump (CP) that outputs a current-pulse, whose pulse-width is proportional to the phase-error. The current-pulse is filtered in a loop-filter (LPF), which results in a control-voltage that is controlling a voltage controlled oscillator (VCO). Based on the control voltage the frequency of the signal *ClkRF* is changed. A pre-scaler divides the frequency down to the same as the reference, and are feed back to the PD. To implement the FSK modulation a select signal (*Select*) controls which of two different paths that is active.
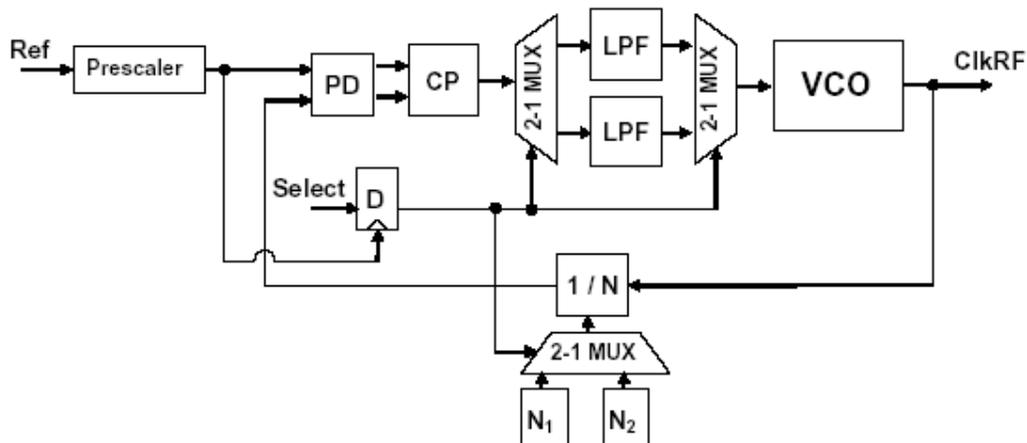
Figure 1: System Block diagram of PLL-based BFSK Modulator

2.2 Important design metrics

The VCO is a critical component in the PLL and must be designed so that the correct frequency range can be assured across process and voltage corners. The charge-pump design is crucial to increase linearity and reduce spurious fluctuations. The loop-filter needs to be

designed with the trade-off between phase-noise and PLL speed in mind. Further, the prescalers (frequency dividers) require extensive timing and performance analysis to reach required performance. Low-power is of utmost importance in this project, so all components in the PLL will be designed for lowest possible power.

3 Area, performance requirements

The table below summarizes the adder performance requirements. Each requirement has its number, formulated text, and the given degree of priority. Three degrees of priority are used: high, medium, and low. High is a firm requirement with no possibility of relaxation, while medium requirements can be relaxed somewhat after good motivation.

| Requirement	Requirement text	Priority
1	Power supply voltage 3.3 V $\pm$ 5%	High
2	All components integrated on-chip	High
3	Schematic and layout must be verified by simulation	High
4	Center frequency 400 MHz	Medium
5	Modulation frequency min 1 MHz	Medium
6	Modulation input 100 kbit/s	Medium
7	Simulated PLL power consumption < 20mW	Medium
8	Chip core area < 0.27mm^2	High
9	Total project pin count: 12	High
10	Design technology is AMS 4-Metal 0.35 mm CMOS High	High
11	The most important system nodes should have off-chip access pins	Medium
12	On-chip current densities < 1 mA/μm	High
13	All requirements fulfilled in *"typical"*, *"slow"*, and *"fast"* process corners and for temperatures between 25°C and 110°C	Medium
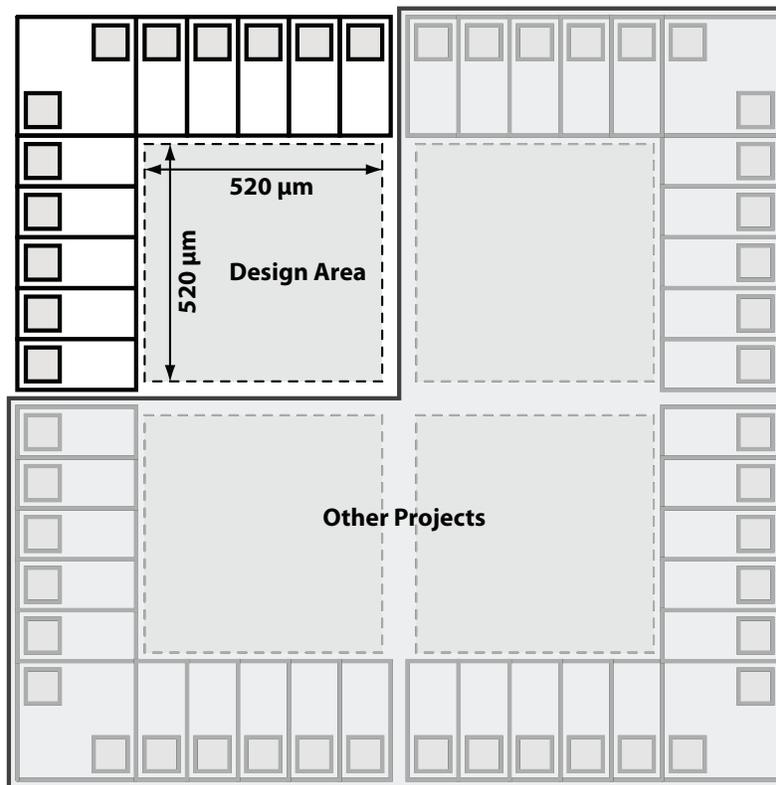
Figure 2: Schematic picture of a 3mm^2 chip with 40 generic pads four V_{DD} and four V_{SS} pads (total 48 pads), which will be shared between a number of projects.

3.1 Available resources

• Scientific publication database (available from LiU):

♦ IEL – IEEE/IEE Electronic Library, http://www.bibl.liu.se/english/databas/

3.2 Tools

♦ Circuit simulation and layout tools from Cadence®, http://www.cadence.com/

4 References

B. Razavi, "Design of Analog CMOS Integrated Circuits", McGraw-Hill, 2001.

B. Leung and C. G. Sodini, "VLSI for Wireless Communication", Pearson Education, 2004.

R.J. Baker, H.W. Li and D.E. Boyce, "CMOS Circuit Design, Layout, and Simulation", IEEE Press, 1998.

For more literature references consult with your supervisor.