VLSI Chip Design Project TSEK06

Project Description and Requirement Specification

Version 1.0

Project: A simple wide-band RF front-end

Project number: TBD

Project Group:

Name	Project members	Telephone	E-mail
	Project leader and designer 1(5)		
	Designer 2(5)		
	Designer 3(5)		
	Designer 4(5)		
	Designer 5(5)		

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1 Background

This document describes the design requirement specification of a simple wide-band RF front-end with a un-balanced input and output. One of the requirements in radio receiver systems today is a RF front-end which can work in a wide frequency range and handle multi bands and different standards. Instead of using separate LNA for each band which is an area consuming design because of matching requirements, a wide-band LNA along with a mixer can be used. Wide-band front-ends are need to have low and large gain modes. Another issue with wide-band front-ends is the need of acceptable linearity and noise performance. As one can understand there will be a trade-off between input matching and noise figure and also a trade-off between gain and linearity.

1.1 Project Goal

The project goal is to design an integrated circuit (IC) in complementary metal-oxide semiconductor (CMOS) technology. Students, participating in this project as project members and project leaders, should learn the different steps of the IC design flow. That includes the given system architecture analysis, simulation, layout implementation and verification. The project students have an optional choice to manufacture the designed IC circuit on a chip. To test the manufactured chips, another course (TSEK11) is available after the project.

1.2 Milestones and Deadline

1: Project selection	Week 3
2: Pre-study, project planning, and discussion with supervisor	Week 4
3: High-level modeling design and simulation result (report)	February 11
4: Gate/transistor level design and simulations result (report)	March 11
5: Layout, DRC, parasitic extraction, LVS, post-layout simulations, modification and chip evaluations.	May 6
6: **DEADLINE**, Delivery of the completed chip.	**May 15**
7: **DEADLINE**, Final report, and oral presentation	**May 24**

1.3 Parties

The following parties are involved in this project:

1- Customer: Omid E. Najari
2- Project supervisor: Omid E. Najari

Tasks:

- Formulates the project requirements
- Provides technical support
- Reviews the project documents.

3- Project leader: One of the members in the design team.

Tasks:

- Responsible for organization of the team and the project planning.

- Divides the design and documentation work in an efficient way
- Organizes the team meetings as well as the meetings between the team and supervisor
- Keeps the supervisor informed about the progress of the project (**at least one email or meeting per week**)

4- Project design members (including the project leader)

- Are equally responsible for project planning and design.
- Participate actively in all the meetings
- Support the team and the project leader
- Keep the team and project leader informed about the progress of their tasks.

2 Project Description

2.1 System Description

The complete system to be built should be a working wide-band RF front-end. The total system is shown in Figure 1. The main components to be designed are an inductor-less wide-band LNA, a noise and distortion cancellation stage, and a mixer. The measurements require output buffers. A schematic of a suitable buffer will be given to you in order to save some time.

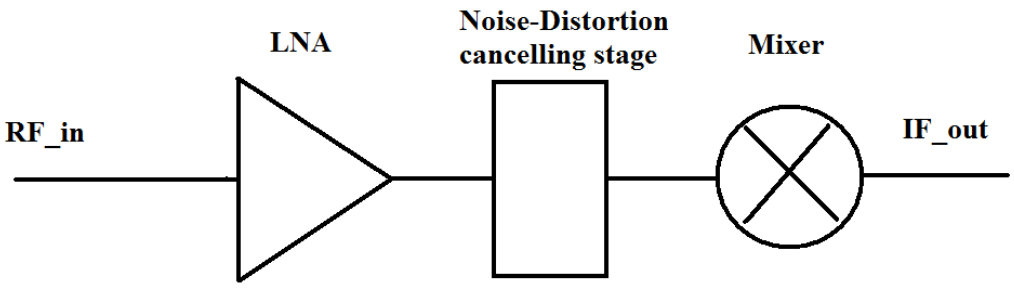

Figure 1: Simple RF front-end architecture.

The target for this design will be to achieve more than 12dB gain over at least 500MHz bandwidth. The input impedance should be matched to 50 Ohms over the whole bandwidth. Linearity requirements will be different for high and low gain modes. For high gain mode the linearity requirements will be more relaxed compare to low gain mode.

Sine wave should be used as local oscillator for the mixer. A signal generator in the lab will be used as local oscillator. The exact working frequency band for the front-end and also the local oscillator frequency will be decided in the first meeting.

2.2 Important Design Metrics

The circuit must be designed for a bandwidth of at least 500MHz. This will be translated to requirements on input impedance matching, noise figure and the gain flatness over the bandwidth. Important things to consider are:

- Wide-band input impedance matching of the LNA.
- Low noise figure of the LNA.
- High linearity for the Mixer.
- Furthermore, the power-consumption is of large interest and should be minimized.

3 Area and Performance Requirements

The table below summarizes the circuit performance requirements. Each requirement has its number, formulated text, and the given degree of priority. Three degrees of priority are used: high, medium, and low. High is a firm requirement with no possibility of relaxation, while medium requirements can be relaxed somewhat after good motivation.

Requirement	Requirement Text	**Priority**
1	Input impedance matching over 500MHz bandwidth	High
2	Low noise figure (NF < 5dB)	High
3	Schematic and layout must be verified by simulation	High
4	Integrate as many components as possible on-chip	High
5	Simulated chip power consumption < 70mW.	Medium
6	Chip core area < 0.27mm^2	High
7	Total project pin count: 12	High
8	Design technology is AMS 4-Metal 0.35μm CMOS	High
9	The most important system nodes should have off-chip access pins	Medium
10	On-chip current densities < 1 mA/μm	High
11	All requirements fulfilled in *"typical"*, *"slow"*, and *"fast"* process corners and for temperatures between 25^{o}C and 110^{o}C	Medium

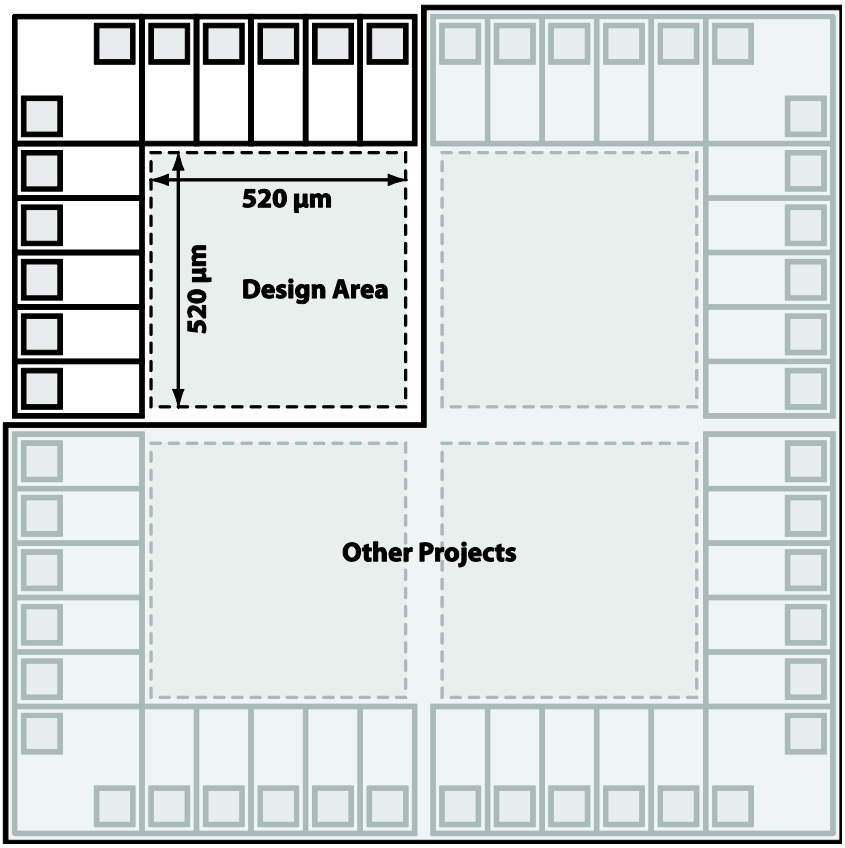

Figure 2: Schematic picture of a 3mm^2 chip with 40 generic pads four V_{DD} and four V_{SS} pads (total 48 pads), which will be shared between a number of projects.

3.1 Available Resources

- Scientific publication database (available from LiU):
- IEL – IEEE/IEE Electronic Library, http://www.bibl.liu.se/english/databas/

3.2 Tools

- Circuit simulation and layout tools from Cadence®, http://www.cadence.com/

4 References

- J.M. Rabaey, A. Chandrakasan, and B. Nikolic., "Digital Integrated Circuits", 2nd ed., Prentice Hall, 2003, ISBN 0-13-120764-4.
- Behzad Razavi, "Design of Analog CMOS Integrated Circuits", McGraw-Hill ISBN: 0072380322.
- Behzad Razavi, "RF Microelectronics", Prentice Hall PTR, ISBN 0-13-887571-5, 1998.
- Thomas H. Lee, "The Design of CMOS Radio Frequency Integrated Circuits", Cambridge University Press, ISBN 0-521-63922-0.

It is highly recommended that students taking this project also take the course TSEK37, TSEK02 and TSEK03.

For more literature references consult with your supervisor.