VLSI Chip Design Project TSEK06

Project description and requirement specification

Version 1.0

Project: DLL-Based Frequency Multiplier

Project number: 4

Project Group:

Name	Project members	Telephone	E-mail
	Project leader and designer 1(5)		
	Designer 2(5)		
	Designer 3(5)		
	Designer 4(5)		
	Designer 5(5)		

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1 Background

This document describes the design requirement specification of a DLL-based frequency multiplier. Typically PLLs are utilized for frequency synthesis purpose. Because of the stability issues, the PLL design is very challenging and time-consuming task. On the other hand DLLs utilize a first-order feedback loop enjoying ensured stability. Since in DLLs only a delayed version of the reference clock is generated, frequency multiplication requires extra circuitry. In this project the objective is to design and implement a fully integrated DLL-based frequency multiplier.

1.1 Project goal

The project goal is to design an integrated circuit (IC) in complementary metal-oxide semiconductor (CMOS) technology. Students, participating in this project as project members and project leaders, should learn the different steps of the IC design flow. That includes the given system architecture analysis, simulation, layout implementation and verification. The project students have an optional choice to manufacture the designed IC circuit on a chip. To test the manufactured chips, another course (TSEK11) is available after the project.

1.2 Milestones and deadline

1: Project selection	Week 3
2: Pre-study, project planning, and discussion with supervisor	Week 4
3: High-level modeling design and simulation result (report)	February 11
4: Gate/transistor level design and simulations result (report)	March 11
5: Layout, DRC, parasitic extraction, LVS, post-layout simulations, modification and chip evaluations.	May 6
6: **DEADLINE**, Delivery of the completed chip.	**May 15**
7: **DEADLINE**, Final report, and oral presentation	**May 24**

1.3 Parties

The following parties are involved in this project:

1- Customer: Ameya Bhide
2- Project supervisor: Ameya Bhide

Tasks:

- Formulates the project requirements
- Provides technical support
- Reviews the project documents.

3- Project leader: One of the members in the design team.

Tasks:

- Responsible for organization of the team and the project planning.
- Divides the design and documentation work in an efficient way

- Organizes the team meetings as well as the meetings between the team and supervisor
- Keeps the supervisor informed about the progress of the project (at least one e-mail or meeting per week)

4- Project design members (including the project leader)

- Are equally responsible for project planning and design.
- Participate actively in all the meetings
- Support the team and the project leader
- Keep the team and project leader informed about the progress of their tasks.

2 Project description

2.1 System description

The complete system to be built should include the frequency multiplier, on-chip evaluation circuits, and I/O circuitry. The complete system block level is shown in Figure 1.

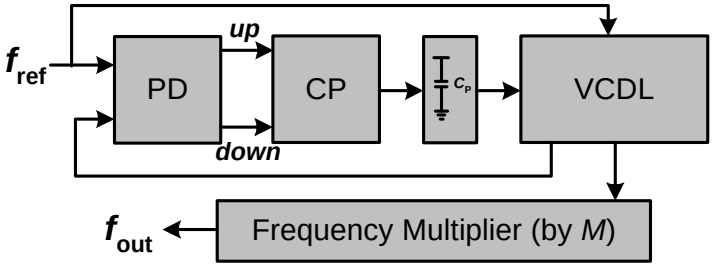

Figure 1: System Block diagram of DLL-based frequency multiplier.

The reference clock is compared to the voltage-controlled delay line (VCDL) output in the phase detector block (PD). The VCDL consists of the differential voltage-controlled inverter stages. The output of the PD controls the charge pump (CP) circuit. When DLL is locked, VCDL generates different equally spaced clock phases within one clock period. At this point the frequency multiplier block generates the multiplied version of the reference clock. A possible implementation of frequency multiplier combines the edges of clock phases to generate multiplied frequency as shown in Figure 2.

2.2 Important design metrics

The frequency multiplier should be designed for a high-performance application. It means that proper approaches must be taken to maximize the performance. However the power consumption should be held at a reasonable level. A proper circuitry to avoid false lock should be designed. During the project discussions on suitable design solutions are expected.

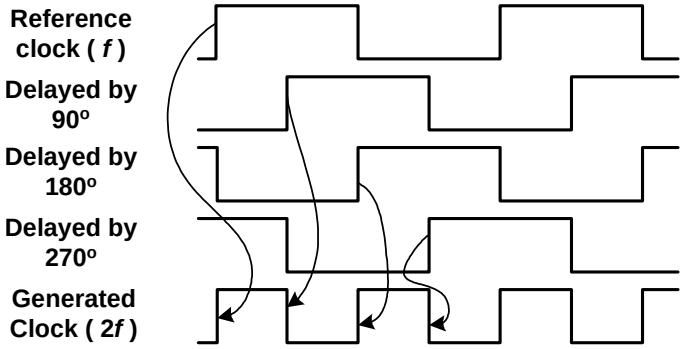

Figure 2: Example of timing for a frequency multiplier

3 Area, performance requirements

The table below summarizes the adder performance requirements. Each requirement has its number, formulated text, and the given degree of priority. Three degrees of priority are used: high, medium, and low. High is a firm requirement with no possibility of relaxation, while medium requirements can be relaxed somewhat after good motivation.

Requirement	Requirement text	Priority
1	Design for low power	Medium
2	Integrate as many system components as possible on-chip	High
3	Schematic and layout must be verified by simulation	High
4	On-chip evaluation should be implemented, for full speed testing	High
5	Multiplied clock frequency at nominal supply (3.3V)>1 GHz	High
6	Simulated chip power consumption < 100mW (3.3V supply)	Medium
7	Simulated circuit power (normal activity) < 50mW (3.3V supply)	Medium
8	Maximum transistor sizing = 20µm	Medium
9	Chip core area < 0.27mm^2	High
10	Total project pin count: 12	High
11	Design technology is AMS 4-Metal 0.35 µm CMOS	High
12	The most important system nodes should have off-chip access pins	Medium
13	On-chip current densities < 1 mA/µm	High
14	All requirements fulfilled in “typical”, “slow”, and “fast” process corners and for temperatures between 25 and 110 ^{o}C	Medium

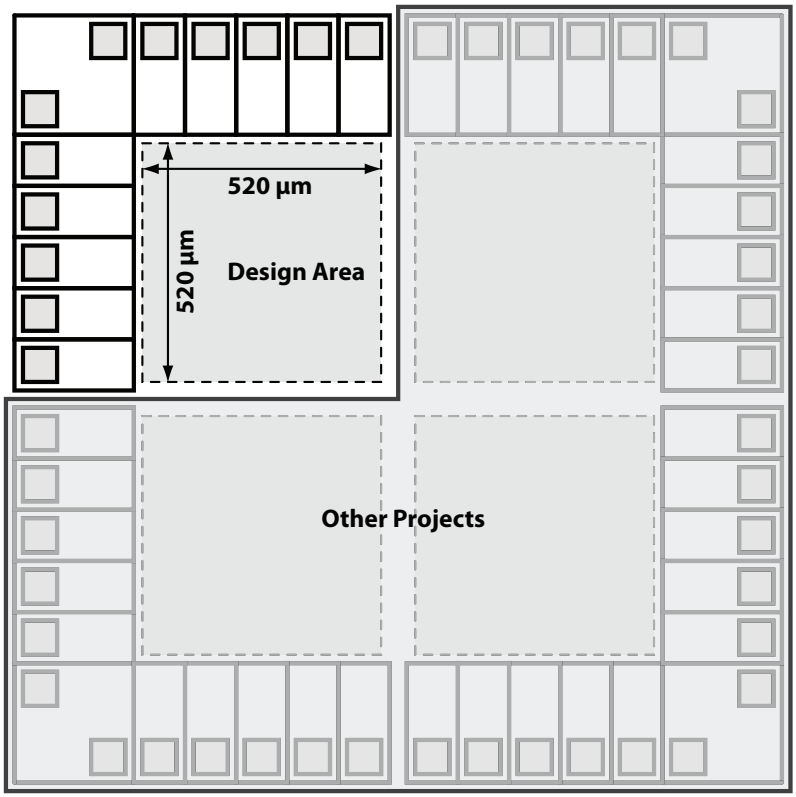

Figure 3: Schematic picture of a 3mm^2 chip with 40 generic pads four V_{DD} and four V_{SS} pads (total 48 pads), which will be shared between a number of projects.

3.1 Available resources

- Scientific publication database (available from LiU):

♦ IEL – IEEE/IEE Electronic Library, http://www.bibl.liu.se/english/databas/

3.2 Tools

♦ Circuit simulation and layout tools from Cadence®, http://www.cadence.com/

4 References

J.M. Rabaey, A. Chandrakasan, and B. Nikolic., "Digital Integrated Circuits", 2nd ed., Prentice Hall, 2003, ISBN 0-13-120764-4.

N. Waste and K. Eshraghian, "Principles of CMOS VLSI Design", Addison-Wesley, 1993.

R.J. Baker, H.W. Li and D.E. Boyce, "CMOS Circuit Design, Layout, and Simulation", IEEE Press, 1998.

S.-M. Kang and Y. Leblebici, "CMOS Digital Integrated Circuits: Analysis and Design", McGraw-Hill, 1999

For more literature references consult with your supervisor.