VLSI Chip Design Project TSEK06

Project Description and Requirement Specification

Version 1.0

Project:
An Active-RC Low-Pass Filter for Zero-IF Wireless Receivers

Project number: 3

Project Group:

Name	Project members	Telephone	E-mail
	Project leader and designer 1(5)		
	Designer 2(5)		
	Designer 3(5)		
	Designer 4(5)		
	Designer 5(5)		

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1 Background

This document describes the design requirements of a fifth-order Active-RC low-pass filter. This low-pass filter can be used as a channel select filter for direct conversion (zero-IF) receivers. The channel select filter is located after the down-converter mixer to select the desired channel and rejects the adjacent channels and strong in-band blockers. The cut-off frequency of channel select filters is equal to the channel bandwidth of the desired standard. The in-band and out-of-band linearity performances are the most important characteristics of channel select filters. The Active-RC (Op-Amp RC) filters are good candidates for implementing channel select filter thanks to their good linearity performance. Low-noise and low power consumption implementation are the other important characteristics which shoul be considered.

1.1 Project Goal

The project goal is to design an integrated circuit (IC) in complementary metal-oxide semiconductor (CMOS) technology. Students, participating in this project as project members and project leaders, should learn the different steps of the IC design flow. That includes the given system architecture analysis, simulation, layout implementation and verification. The project students have an optional choice to manufacture the designed IC circuit on a chip. To test the manufactured chips, another course (TSEK11) is available after the project.

1.2 Milestones and Deadline

1: Project selection	Week 3
2: Pre-study, project planning, and discussion with supervisor	Week 4
3: High-level modeling design and simulation result (report)	February 11
4: Gate/transistor level design and simulations result (report)	March 11
5: Layout, DRC, parasitic extraction, LVS, post-layout simulations, modification and chip evaluations.	May 6
6: **DEADLINE**, Delivery of the completed chip.	**May 15**
7: **DEADLINE**, Final report, and oral presentation	**May 24**

1.3 Parties

The following parties are involved in this project:

1- Customer: Mostafa Savadi Osgooei
2- Project supervisor: Mostafa Savadi Osgooei

Tasks:

- Formulates the project requirements
- Provides technical support
- Reviews the project documents.

3- Project leader: One of the members in the design team.

Tasks:

- Responsible for organization of the team and the project planning.
- Divides the design and documentation work in an efficient way
- Organizes the team meetings as well as the meetings between the team and supervisor
- Keeps the supervisor informed about the progress of the project (**at least one email or meeting per week**)

4- Project design members (including the project leader)

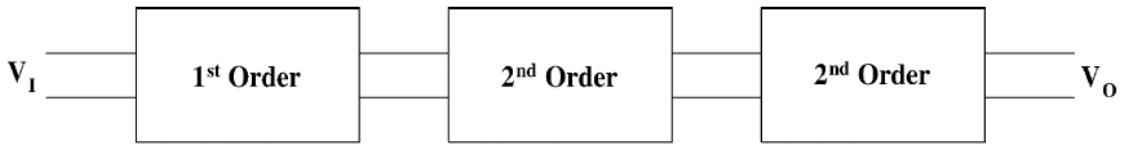
- Are equally responsible for project planning and design.
- Participate actively in all the meetings
- Support the team and the project leader
- Keep the team and project leader informed about the progress of their tasks.

2 Project Description

2.1 System Description

The complete fifth-order low-pass filter schematic is shown in Fig. 1. It consists of one first-order stage and two second-order (bi-quad) stages. The pole frequencies and quality factor of each stage can be determined by the transfer function of filter. The transfer function of filter depends on the type, order, DC gain and cutoff frequency of filter. In this project the fifth-order Chebyshef approximation is chosen due to its good selectivity. The DC gain of 0 dB and less than 0.5 dB ripple for pass band are the other specifications of the desired filter. The cut-off frequency of filter in this project is selected between 10 and 14 MHz because of the most of wireless receivers have the channel bandwidth of about 10-14 MHz.

The schematic of a single ended typical bi-quad is shown in Fig. 2. The bi-quad (value of elements and op-amp specifications) are designed according to the cutoff frequency, pass band ripple, and quality factor of bi-quad. The schematic of op-amp is given later. The gain-bandwidth, DC gain, phase margin, and noise specifications of op-amp are obtained so that the shape of filter is preserved.



$$H_{tot}(s) = \underbrace{\underbrace{\underbrace{\frac{1}{\left(1+\frac{s}{\omega_{o0}}\right)}}_{\text{1st-order}}\frac{\omega_{o1}^2}{\left(s^2+\frac{\omega_{o1}}{Q}s+\omega_{o1}^2\right)}}_{\text{3rd-order}}\frac{\omega_{o2}^2}{\left(s^2+\frac{\omega_{o2}}{Q}s+\omega_{o2}^2\right)}}_{\text{5th-order}}$$

Fig. 1. The top-level schematic of filter and division of cascade stages transfer function.

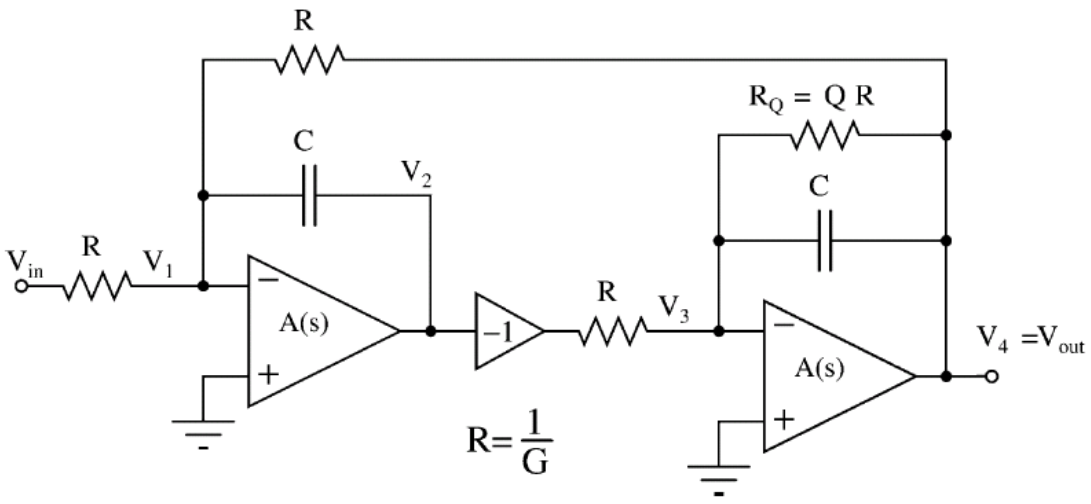


Fig. 2. Bi-quad circuit for Chebyshev approximation.

2.2 Important Design Metrics

The filter is designed for cutoff frequencies of 10- and 14 MHz. This will be translated to the requirements of op-amp. Important parameters to consider are:

- Gain-bandwidth, noise, phase margin, linearity of op-amp.
- In-band linearity of filter
- Out-of-band linearity of filter
- Input-referred noise of filetr
- Reconfiguabilty of the filter structure for 10 and 14 MHz cutoff frequencies
- Furthermore, the power-consumption is of large interest and should be minimized.

3 Area and Performance Requirements

The table below summarizes the circuit performance requirements. Each requirement has its number, formulated text, and the given degree of priority. Three degrees of priority are used: high, medium, and low. High is a firm requirement with no possibility of relaxation, while medium requirements can be relaxed somewhat after good motivation.

3.1 Available Resources

- Scientific publication database (available from LiU):
- IEL – IEEE/IEE Electronic Library, http://www.bibl.liu.se/english/databas/

3.2 Tools

- Circuit simulation and layout tools from Cadence®, http://www.cadence.com/
- Matlab

Requirement	Requirement Text	Priority
1	Cutoff frequency of filter (10 and 14 MHz)	High
2	In-band and out-of-band linearity of better than +25 dBm and +15 dBm, respectively	High
3	Input referred noise better than 50 nV/√Hz	High
4	Schematic and layout must be verified by simulation	High
5	Layout matching	High
6	Simulated chip power consumption < 8 mW at 14 MHz.	Medium
7	Chip core area < 0.27mm^2	High
8	Total project pin count: 12	High
9	Design technology is AMS 4-Metal 0.35µm CMOS	High
10	The most important system nodes should have off-chip access pins	Low
11	On-chip current densities < 1 mA/µm	High
12	All requirements fulfilled in *"typical"*, *"slow"*, and *"fast"* process corners and for temperatures between 25^{o}C and 110^{o}C	Medium

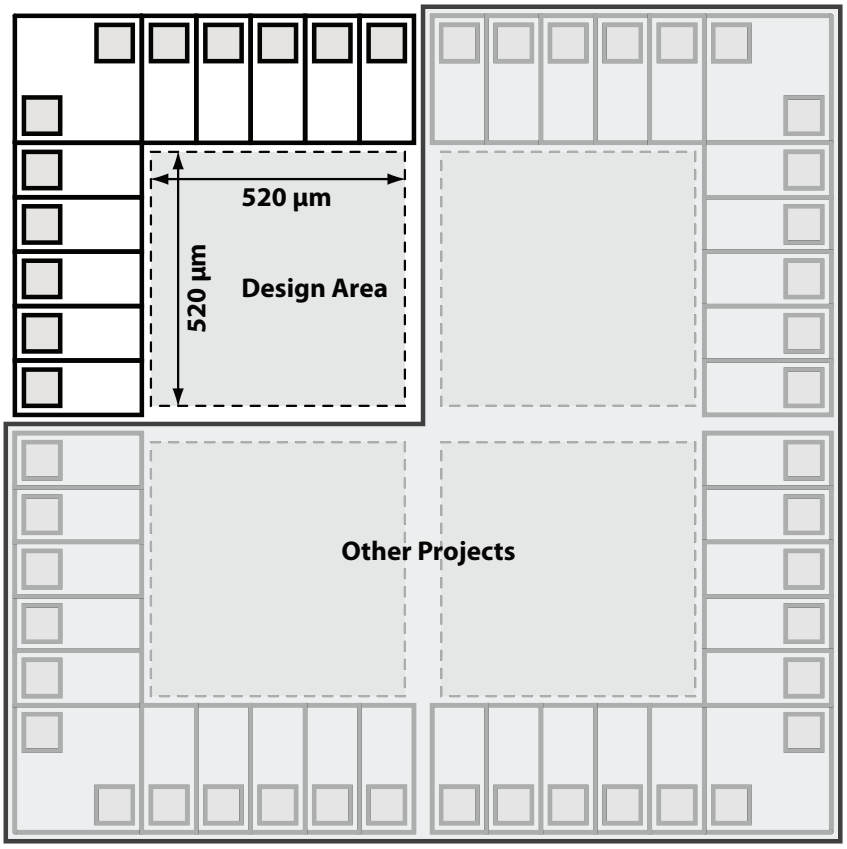


Figure 3: Schematic picture of a 3mm^2 chip with 40 generic pads four V_{DD} and four V_{SS} pads (total 48 pads), which will be shared between a number of projects.

4 References

[1] M. Banu and Y. Tsividis, "Fully integrated active RC filters in MOS technology," *IEEE J. Solid-State Circuits*, vol. SC-18, no. 6, pp. 644-651, December 1983.

[2] H. Amir-Aslanzadeh, E. J. Pankratz, and E. Sánchez-Sinencio, "A 1-V +31 dBm IIP3, reconfigurable, continuously tunable, power-adjustable active-RC LPF," *IEEE J. Solid-State Circuits,* vol. 44, no. 2, pp. 495–508, February 2009.

[3] A. Vasilopoulos, G. Vitzilaios, G. Theodoratos, and Y. Papananos, "A low-power wideband reconfigurable integrated active-RC filter with 73dB SFDR," *IEEE J. Solid-State Circuits*, vol. 41, no. 9, pp. 1997–2008, September 2006.

[4] P. R. Gray, P. J. Hurst, S. H. Lewis, and R. G. Mayer, *Analysis and Design of Analog Integrated Circuits*, Wiley, New York, 2001.

For more literature references consult with your supervisor.