VLSI Chip Design Project TSEK06

Project Description and Requirement Specification

Version 1.0

Project: A Second-Order Band-Pass Sigma-Delta Modulator with 1-Bit Quantizer

Project number: 2

Project Group:

Name	Project members	Telephone	E-mail
	Project leader and designer 1(5)		
	Designer 2(5)		
	Designer 3(5)		
	Designer 4(5)		
	Designer 5(5)		

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1 Background

An important building block of a digital receiver is an analog to digital converter. Recent trend is the use of Sigma Delta (ΣΔ) ADC instead of Nyquist rate ADC in radio receivers. ΣΔ ADC is much appreciated ADC topology in radio receiver due to its high dynamic range and linearity. ΣΔ ADC is based on the concept of "*oversampling*: sampling frequency much larger than minimum sampling frequency dictated by Nyquist criteria (OSR = $F_s/2\,\Delta f$), where *Fs* is the sampling frequency and Δf is the signal bandwidth." combined with "*noise shaping*: achieved with a feedback loop such that quantization noise is high pass filtered and signal of interest is unaffected". Oversampling and noise shaping techniques allows the use of as low as 1-bit ADC within the ΣΔ modulator loop to achieve the equivalent performance of N bits ADCs depending on the oversampling ratio and the order of ΣΔ modulator. N can as high as 20.

A/D conversion is mostly performed at baseband in a super heterodyne receiver, so that a relatively relaxed ADC in terms of dynamic range and linearity is required to perform this operation.

However the current trend is towards multi-standard receivers, in which case the ADC should be as close to antenna as possible, directly operating on a signal centered at some high frequency (opposed to a baseband ADC which operates on a signal centered at zero frequency). Further down-conversion is then achieved digitally with almost perfect matching and high accuracy between *I* and *Q* paths of *IQ* mixer. Though present at some high frequency, bandwidth of the signal itself is generally very small. GSM is a famous example, assuming a center frequency of f_c = 10 MHz (which is the IF frequency in a super-heterodyne receiver) in the frequency spectrum, channel bandwidth of this system is Δf = 200KHz only.

Bandpass ΣΔ modulator is most useful when sampling frequency $F_S = 4\ f_c$ = 40 MHz is chosen. Note that OSR in this case is OSR = $F_S / 2\Delta f$ = 100. This choice of $F_S = 4f_c$ very much simplifies the second down-conversion step to be performed in digital domain. This down-conversion process becomes as simple as multiplication of the data with a sequence of 1,-1 and 0, which means no change, two's complement and no data in other words. Block diagram of a bandpass ΣΔ modulation combined with down-conversion step is shown in Fig. 1.

1.1 Project Goal

The project goal is to design an integrated circuit (IC) in complementary metal-oxide semiconductor (CMOS) technology. Students, participating in this project as project members and project leaders, should learn the different steps of the IC design flow. This includes the given system architecture analysis, simulation, layout implementation and verification. The project students have an optional choice to manufacture the designed IC circuit on a chip. To test the manufactured chips, another course (TSEK11) is available after the project.

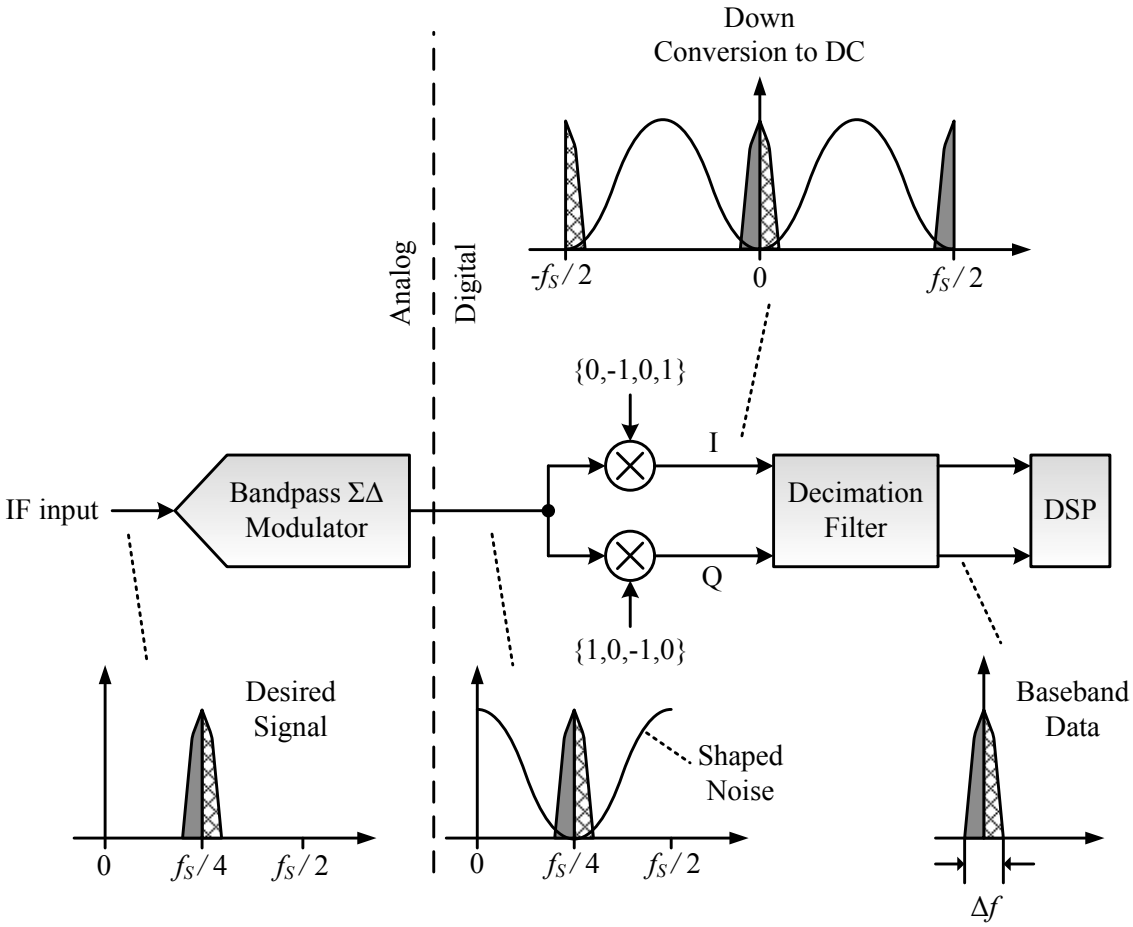

Figure 1: Bandpass ΣΔ ADC system.

1.2 Milestones and Deadline

1: Project selection	Week 3
2: Pre-study, project planning, and discussion with supervisor	Week 4
3: High-level modeling design and simulation result (report)	February 11
4: Gate/transistor level design and simulations result (report)	March 11
5: Layout, DRC, parasitic extraction, LVS, post-layout simulations, modification and chip evaluations.	May 6
6: **DEADLINE**, Delivery of the completed chip.	**May 15**
7: **DEADLINE**, Final report, and oral presentation	**May 24**

1.3 Parties

The following parties are involved in this project:

1- Customer: Fahad Qazi
2- Project supervisor: Fahad Qazi

Tasks:

- Formulates the project requirements
- Provides technical support
- Reviews the project documents.

3- Project leader: One of the members in the design team.

Tasks:

- Responsible for organization of the team and the project planning.
- Divides the design and documentation work in an efficient way
- Organizes the team meetings as well as the meetings between the team and supervisor
- Keeps the supervisor informed about the progress of the project (**at least one email or meeting per week**)

4- Project design members (including the project leader)

- Are equally responsible for project planning and design.
- Participate actively in all the meetings
- Support the team and the project leader
- Keep the team and project leader informed about the progress of their tasks.

2 Project Description

2.1 System Description

The complete system to be built should be a working second-order bandpass ΣΔ modulator. The total system is shown in Fig. 2. The main components to be designed are a switched capacitor resonator, a comparator and an optional quadrature down-conversion mixer as shown in Fig. 1. The switched-cap resonators require an Operational amplifier (OP). A schematic of a suitable OP will be given to you in order to save some time. The digital filter that is needed after the ΣΔ modulator can be done in Matlab when doing chip measurements.

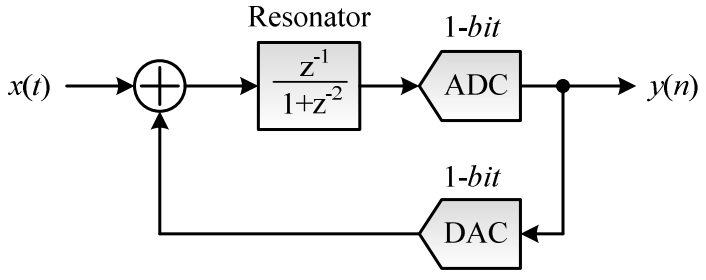

Figure 2: Second-order bandpass Sigma-Delta modulator architecture.

The bandpass ΣΔ ADC has to be designed for a center frequency of f_c = 10 MHz and sampling frequency of $F_s = 4f_c$ = 40 MHz. The target for this design will be to achieve about 55-60dB dynamic range over a 200 kHz bandwidth. The dynamic range (SNR=Signal-to-

noise ratio) that can achieved with a second-order bandpass ΣΔ modulator can be calculated as

$$SNR = 6.02N + 1.76 - 5.17 + 30\log(OSR)$$

Note that the above relation is the same as *SNR* relation for first-order lowpass ΣΔ modulator. Where *N* is the number of bits from the quantizer, and *OSR* is the oversampling ratio (the ratio of input bandwidth and the Nyquist frequency). For our case *OSR* = 40 MHz / (2 x 200 kHz) = 100 gives an *SNR* of about 60dB. This is equivalent to a 9.6-bit ADC. For a second-order bandpass sigma delta modulator an increase of the oversampling ratio by a factor of two means an increase of the equivalent number of bits by 1.5.

Resonator is the main building block of bandpass sigma delta modulator. Different resonators topologies exist in literature. They vary in complexity and performance. Some are prone to component mismatches while others are immune to a reasonable extent. Three different discrete time resonators can be

- Forward Euler Resonator
- Lossless Discrete Integrator (LDI)
- Double Delay Resonator (DD)

Generally two op-amps are required to build a resonator circuit. Some resonators can be build using one opamp and more than two phase clocking schemes. In this way power and area can be saved by reducing the number of operation amplifiers. You will choose the type of resonator after investing different resonator circuits on system level.

You will go through the following four project phases in this course.

1. Modeling the bandpass ΣΔ ADC in matlab.
2. High level simulation in verilogA.
3. Schematic level simulation (Cadence)
4. Layout and tap-out (Cadence)

2.2 Important Design Metrics

The circuit must be designed for a sampling frequency of at least 40 MHz. This will be translated to requirements on the resonators and comparator. Important things to consider are:

- Timing, settling, and internal noise in the resonators.
- Resonators are sensitive to change in their center frequency ($F_S/4$) which degrade the overall ADC performance.
- Switches in switch-cap circuits are very critical and can be a cause of strong non-linearity if not designed properly.
- Precision in the ADC.
- Furthermore, the power-consumption is of large interest and should be minimized.

3 Area and Performance Requirements

The table below summarizes the circuit performance requirements. Each requirement has its number, formulated text, and the given degree of priority. Three degrees of priority are used: high, medium, and low. High is a firm requirement with no possibility of relaxation, while medium requirements can be relaxed somewhat after good motivation.

Requirement	**Requirement Text**	**Priority**
1	Sampling frequency at least 40MHz	Medium
2	Integrate as many system components as possible on-chip	High
3	Schematic and layout must be verified by simulation	High
4	Layout matching	High
5	Simulated chip power consumption < 100mW at max. freq.	Medium
6	Chip core area < 0.27mm^2	High
7	Total project pin count: 12	High
8	Design technology is AMS 4-Metal 0.35μm CMOS	High
9	The most important system nodes should have off-chip access pins	Low
10	On-chip current densities < 1 mA/μm	High
11	All requirements fulfilled in *"typical"*, *"slow"*, and *"fast"* process corners and for temperatures between 25^{o}C and 110^{o}C	Medium

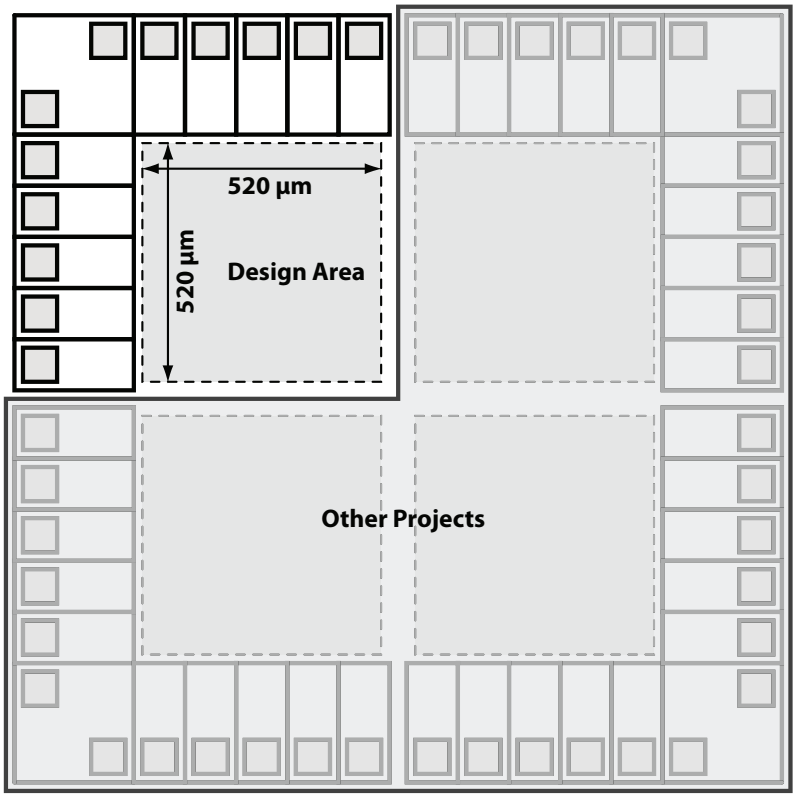

Figure 2: Schematic picture of a 3mm^2 chip with 40 generic pads four V_{DD} and four V_{SS} pads (total 48 pads), which will be shared between a number of projects.

3.1 Available Resources

- Scientific publication database (available from LiU):
- IEL – IEEE/IEE Electronic Library, http://www.bibl.liu.se/english/databas/

3.2 Tools

- Circuit simulation and layout tools from Cadence®, http://www.cadence.com/

4 References

- Richard Schreier Gabor C. Temes "Understanding Delta Sigma Data Converters" John Wiley and Sons, 2005, ISBN 0-471-46585-2.
- J.M. Rabaey, A. Chandrakasan, and B. Nikolic., "Digital Integrated Circuits", 2nd ed., Prentice Hall, 2003, ISBN 0-13-120764-4.
- D.A. Johns and K. Martin, "Analog Integrated Circuit Design", John Wiley & Sons, 1997.
- Delta-sigma data conversion in wireless transceivers *Galton, I.;* Microwave Theory and Techniques, IEEE Transactions on , Volume: 50 , Issue: 1 , Jan. 2002 Pages:302 - 315

For more literature references consult with your supervisor.