VLSI Chip Design Project TSEK06

Project description and requirement specification

Version 1.0

Project: IF Digitization with Second-Order Passive Sigma-Delta Modulator

Project number: 7

Project Group:

Name	Project members	Telephone	E-mail
	Project leader and designer 1(5)		
	Designer 2(5)		
	Designer 3(5)		
	Designer 4(5)		
	Designer 5(5)		

Customer and supervisor: Fahad Qazi
Office: B-house 229:212, Phone: 013-282254, Fax: 013-139282
Email: qazi@isy.liu.se

1 Background

This document describes the design requirement specification of a second-Order Sigma-Delta modulator with a 1-bit quantizer (1-bit ADC). One of the bottlenecks in systems today is the data converters (A/D and D/A) required to move between analog and digital domain. Instead of using an ADC with a large number of bits, which is tough to design because of matching requirements, an oversampled low resolution ADC together with noise-shaping can be used. Using the concept of bandpass sampling, a passive sigma-delta modulator can down-convert the IF signal to baseband. Thus a passive sigma-delta converter can replace the IF mixer and baseband ADC in a typical super-heterodyne receiver. The main issue with Sigma-Delta ADCs is the need of oversampling. As one can understand there is of course a limit what we can do in terms of oversampling ratio.

1.1 Project goal

The project goal is to design an integrated circuit (IC) in complementary metal-oxide semiconductor (CMOS) technology. Students, participating in this project as project members and project leaders, should learn the different steps of the IC design flow. That includes the given system architecture analysis, simulation, layout implementation and verification. The project students have an optional choice to manufacture the designed IC circuit on a chip. To test the manufactured chips, another course (TSEK11) is available after the project.

1.2 Milestones and deadline

1: Project selection	Week 3
2: Pre-study, project planning, and discussion with supervisor	Week 4
3: High-level modeling design and simulation result (report)	February 19
4: Gate/transistor level design and simulations result (report)	March 5
5: Layout, DRC, parasitic extraction, LVS, post-layout simulations, modification and chip evaluations.	April 30
6: **DEADLINE**, Delivery of the completed chip.	**May 7**
7: **DEADLINE**, Final report, and oral presentation	**May 21**

1.3 Parties

The following parties are involved in this project:

1- Customer: Fahad Qazi
2- Project supervisor: Fahad Qazi

Tasks:

- Formulates the project requirements
- Provides technical support
- Reviews the project documents.

3- Project leader: One of the members in the design team.

Tasks:

- Responsible for organization of the team and the project planning.
- Divides the design and documentation work in an efficient way
- Organizes the team meetings as well as the meetings between the team and supervisor
- Keeps the supervisor informed about the progress of the project (**at least one email or meeting per week**)

4- Project design members (including the project leader)

- Are equally responsible for project planning and design.
- Participate actively in all the meetings
- Support the team and the project leader
- Keep the team and project leader informed about the progress of their tasks.

2 Project description

2.1 System description

The complete system to be built should be a working second-order passive Sigma-Delta modulator. The total system is shown in Figure 1. The main components to be designed are the passive integrators, comparator and also a buffer if needed. The ratios of the capacitors in passive integrators will decide its bandwidth. Note that passive integrators do not require an Operational amplifier (OP). Capacitor values in passive sigma delta modulators should be chosen properly and should be optimized for maximum SNR. The digital filter that is needed after the Sigma-Delta modulator can be done in Matlab when doing chip measurements.

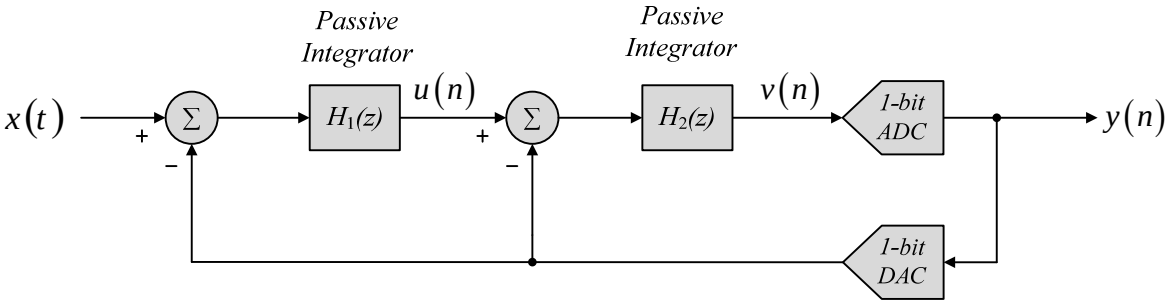

Figure 1: Second-order Sigma-Delta modulator architecture.

The target for this design will be to achieve about 70-75dB dynamic range over a 100 kHz bandwidth which translates to the Effective number of bits, ENOB =12. The dynamic range (SNR=Signal-to-noise ratio) that can achieved with an ideal second-order Sigma-Delta modulator can be calculated as

$$SNR = 6.02 \cdot N + 1.76 - 12.9 + 50\log(OSR)$$

Where N is the number of bits from the quantizer, and OSR is the oversampling ratio (the ratio of input bandwidth and the nyquist frequency). Using a sampling frequency of 50MHz (OSR = 50 MHz / (2 x 100 kHz) = 250) gives an SNR of about 115dB. However a passive sigma delta modulator does not directly follow this relation. Typically second-order passive sigma delta follows the relation for first order ideal sigma delta modulator. The main advantage of passive sigma delta is the high linearity and mixer integration within the sigma delta loop. This allows it to be used as a direct IF digitizer.

2.2 Important design metrics

The circuit must be designed for a sampling frequency of at least 50MHz. This will be translated to requirements on the integrators, 1-bit quantizer, and the 1-bit DAC. Important things to consider are:

- Timing, settling, and internal noise in the integrators
- Precision in the comparator
- Optimum capacitor values for the integrators should be chosen for maximum SNR.
- Furthermore, the power-consumption is of large interest and should be minimized.

3 Area and performance requirements

The table below summarizes the circuit performance requirements. Each requirement has its number, formulated text, and the given degree of priority. Three degrees of priority are used: high, medium, and low. High is a firm requirement with no possibility of relaxation, while medium requirements can be relaxed somewhat after good motivation.

Requirement	**Requirement text**	**Priority**
1	Sampling frequency at least 50MHz	High
2	Integrate as many system components as possible on-chip	High
3	Schematic and layout must be verified by simulation	High
4	Layout matching	High
5	Simulated chip power consumption < 50mW at max. freq.	Medium
6	Chip core area < $0.6mm^2$	High
7	Total project pin count: 12	High
8	Design technology is AMS 4-Metal 0.35μm CMOS	High
9	The most important system nodes should have off-chip access pins	Low
10	On-chip current densities < 1 mA/μm	High
11	All requirements fulfilled in *"typical"*, *"slow"*, and *"fast"* process corners and for temperatures between 25^oC and 110^oC	Medium

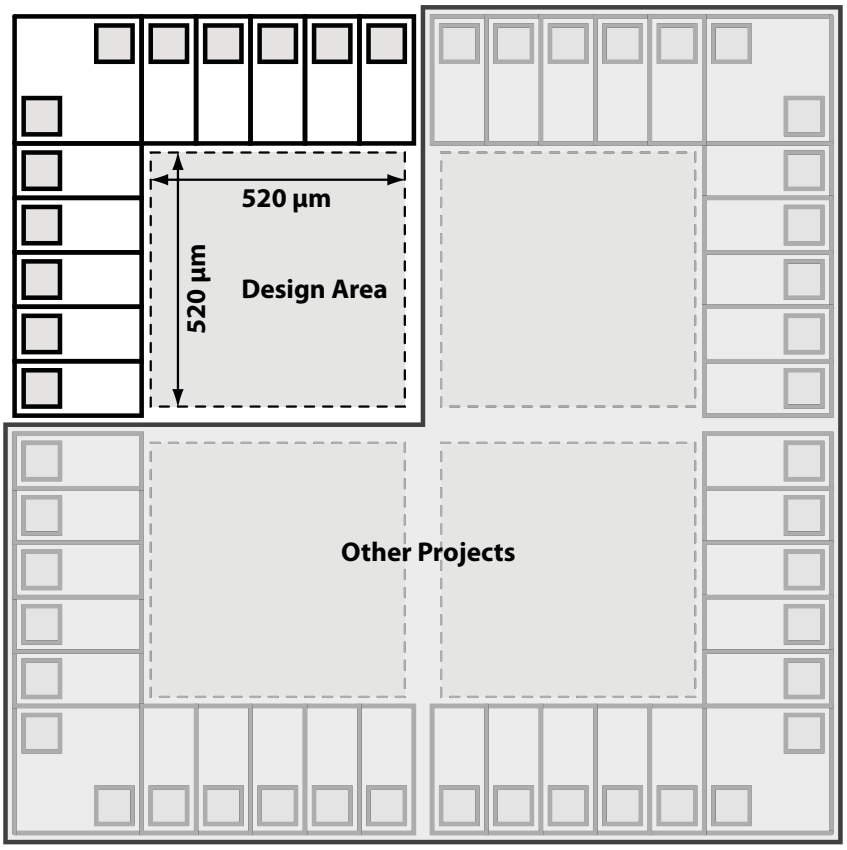

Figure 2: Schematic picture of a 3mm^2 chip with 40 generic pads four V_{DD} and four V_{SS} pads (total 48 pads), which will be shared between a number of projects.

3.1 Available resources

- Scientific publication database (available from LiU):
- IEL – IEEE/IEE Electronic Library, http://www.bibl.liu.se/english/databas/

3.2 Tools

- Circuit simulation and layout tools from Cadence®, http://www.cadence.com/

4 References

- J.M. Rabaey, A. Chandrakasan, and B. Nikolic., “Digital Integrated Circuits”, 2nd ed., Prentice Hall, 2003, ISBN 0-13-120764-4.
- D.A. Johns and K. Martin, “Analog Integrated Circuit Design”, John Wiley & Sons, 1997.
- A 0.25-mW Low-Pass Passive Sigma–Delta Modulator with Built-In Mixer for a 10-MHz IF Input. Feng Chen, Bosco Leung.
- A 12-mW ADC delta-sigma modulator with 80 dB of dynamic range integrated in a single-chip Bluetooth transceiver; Grilo,J.;Galton,I.;Wang,K.;Montemayor,R.G.; Solid-State Circuits, IEEE Journal of , Volume:37, Issue:3, March2002 Pages:271 – 278

- Delta-sigma data conversion in wireless transceivers *Galton, I.;* Microwave Theory and Techniques, IEEE Transactions on , Volume: 50 , Issue: 1 , Jan. 2002 Pages:302 - 315

For more literature references consult with your supervisor.