VLSI Chip Design Project TSEK06

Project description and requirement specification

Version 1.0

Project: High Speed Serial Link Transceiver

Project number: 6

Project Group:

Name	Project members	Telephone	E-mail
	Project leader and designer 1(5)		
	Designer 2(5)		
	Designer 3(5)		
	Designer 4(5)		
	Designer 5(5)		

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1 Background

This document describes the design requirement specification of a high speed serial link transceiver. Serial link interfaces are used to transmit high speed data on a single link to avoid skew issues when transmitting parallel words. The receiver must be able to extract the clock from the transmitted data and use this to successfully sample the incoming data. Coding is often used to guarantee a certain amount of transitions on the data line for the clock extraction to work, and for the decoding to work correct detection of the word boundaries will be necessary.

1.1 Project goal

The project goal is to design an integrated circuit (IC) in complementary metal-oxide semiconductor (CMOS) technology. Students, participating in this project as project members and project leaders, should learn the different steps of the IC design flow. That includes the given system architecture analysis, simulation, layout implementation and verification. The project students have an optional choice to manufacture the designed IC circuit on a chip. To test the manufactured chips, another course (TSEK11) is available after the project.

1.2 Milestones and deadline

1: Project selection	Week 3
2: Pre-study, project planning, and discussion with supervisor	Week 4
3: High-level modeling design and simulation result (report)	February 12
4: Gate/transistor level design and simulations result (report)	March 5
5: Layout, DRC, parasitic extraction, LVS, post-layout simulations, modification and chip evaluations.	April 30
6: **DEADLINE**, Delivery of the completed chip.	**May 7**
7: **DEADLINE**, Final report, and oral presentation	**May 21**

1.3 Parties

The following parties are involved in this project:

1- Customer: Timmy Sundström
2- Project supervisor: Timmy Sundström

Tasks:

- Formulates the project requirements.
- Provides technical support.
- Reviews the project documents.

3- Project leader: One of the members in the design team.

Tasks:

- Responsible for organization of the team and the project planning.
- Divides the design and documentation work in an efficient way

- Organizes the team meetings as well as the meetings between the team and supervisor
- Keeps the supervisor informed about the progress of the project (**at least one email or meeting per week**)

4- Project design members (including the project leader)

- Are equally responsible for project planning and design.
- Participate actively in all the meetings.
- Support the team and the project leader.
- Keep the team and project leader informed about the progress of their tasks.

2 Project description

2.1 System description

The complete system, as seen in Figure 1, to be built should be a working serial link transceiver. The transmitter will send random byte words over the link and after processed by the receiver these should be compared against the transmitted data in order to estimate the word error rate at high throughputs.

The transmitter should be able to either send out a continuous stream of random data words or so called comma symbols which are used by the receiver to both estimate the optimal sampling point as well as to detect the beginning and end of each transmitted symbol. The 8b data words are then coded to 10b with a 8b10b encoder in order to control the DC signal level and guarantee enough signal transitions for clock recovery.

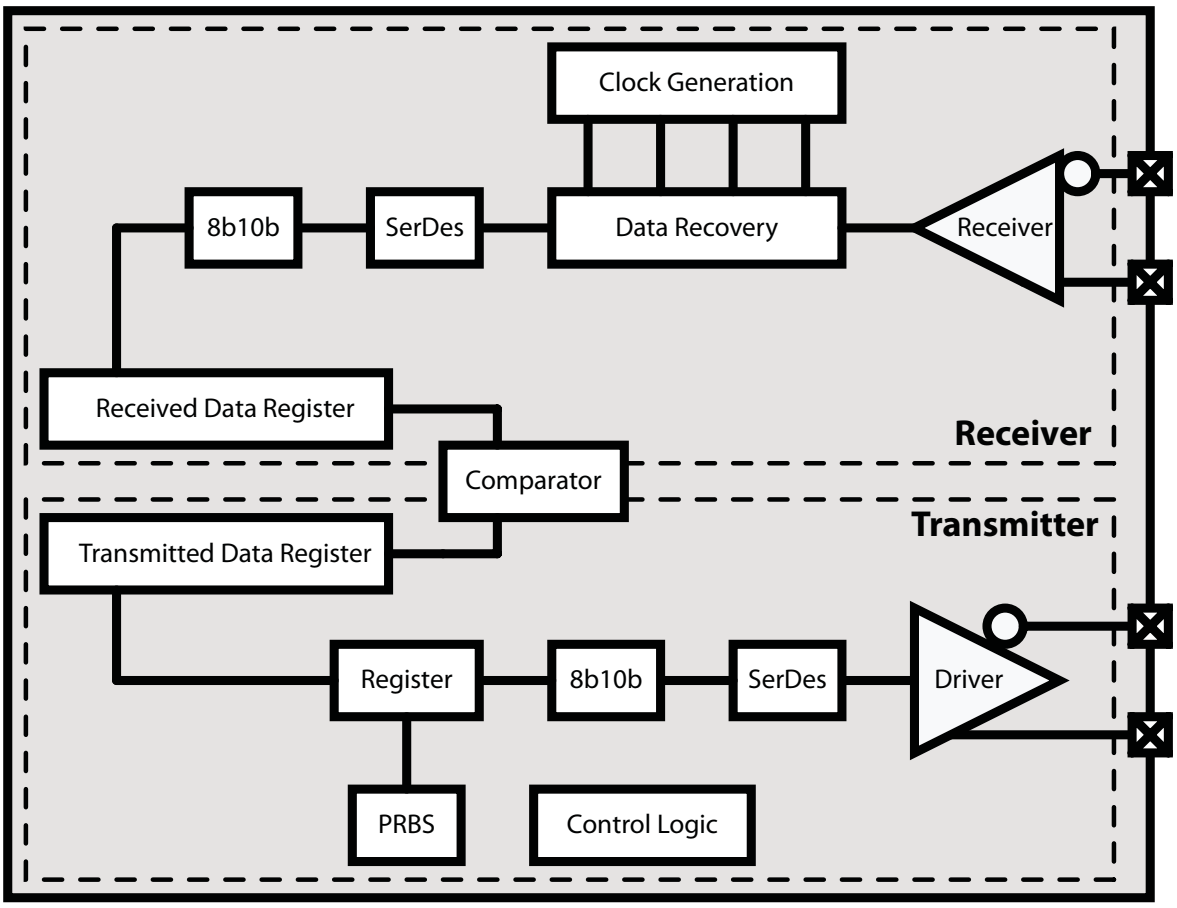

Figure 1: Serial Link Transceiver Architecture.

The receiver works by oversampling the incoming data by a factor of 4x, from these samples the rising and falling edges are detected and an optimal sampling instance is decided upon and is continuously up-dated to compensate for drift. With the help of the comma sequences the correct word boundaries are detected and the 10 bit words are then passed to the 8b10b decoder to generate the corresponding 8b digital incoming data or a signal showing that is was a comma symbol.

Once data is sent from the transmitter and received they are checked for parity errors and then the received word is compared to the transmitted one generating a pulse on either one of two output pins depending on if the words matched or not. These pulses can be counted to estimate the word error rate as a function of the data rate.

2.2 Important design metrics

The design target for this project is to reach a data rate, limited by the on-chip clock frequency at around 500 MBit/s over a 10 cm PCB track. Lower data rates should also be supported over longer network cables.

During comma transmission mode the detection of comma sequences should cause pulses on one of the output pins. During data mode, the same pin is used to send out a pulse if the received word matches the transmitted, otherwise a pulse is sent on another pin to signify a faulty transmission. These pulses are used to calculate the word error rate.

The purposes for the twelve pins in the project can be found in the table below.

Pins	**Pin Description**
1,2	Differential Output
3,4	Differential Input
5	Clock Input
6	V_{DD}
7	V_{SS}
8,9	Outputs for: Faulty Transmission, Correct Transmission, Comma detection and Parity Error
10	Biasing pin
11	Input: Mode select
12	Input: Reset

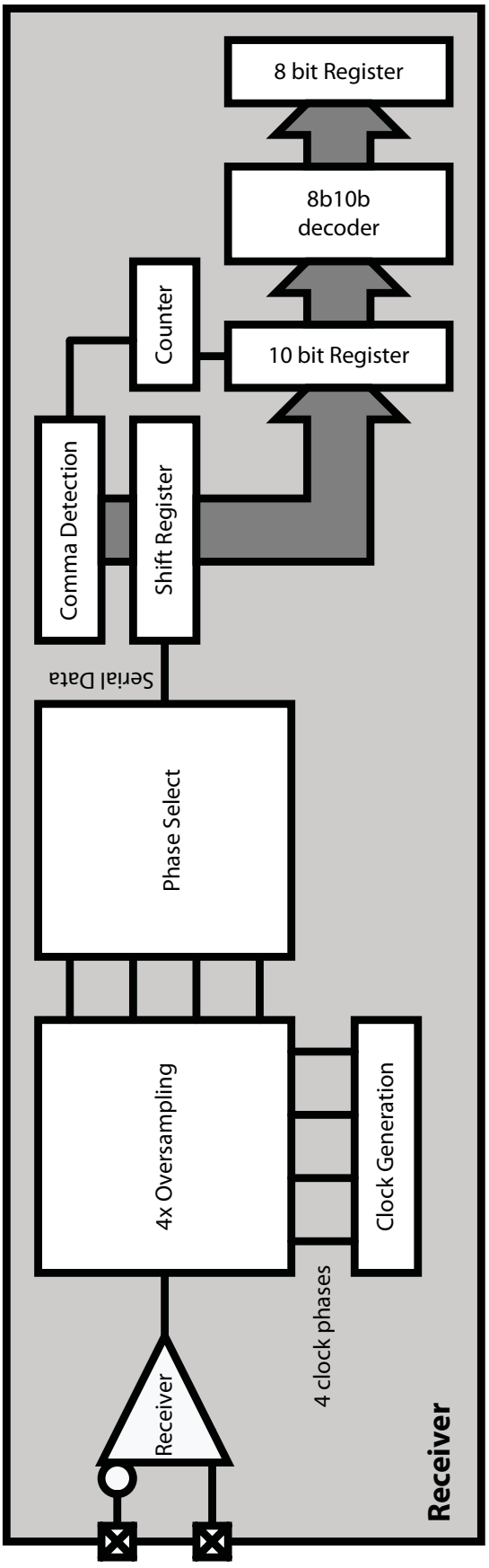

Figure 2: Receiver architecture

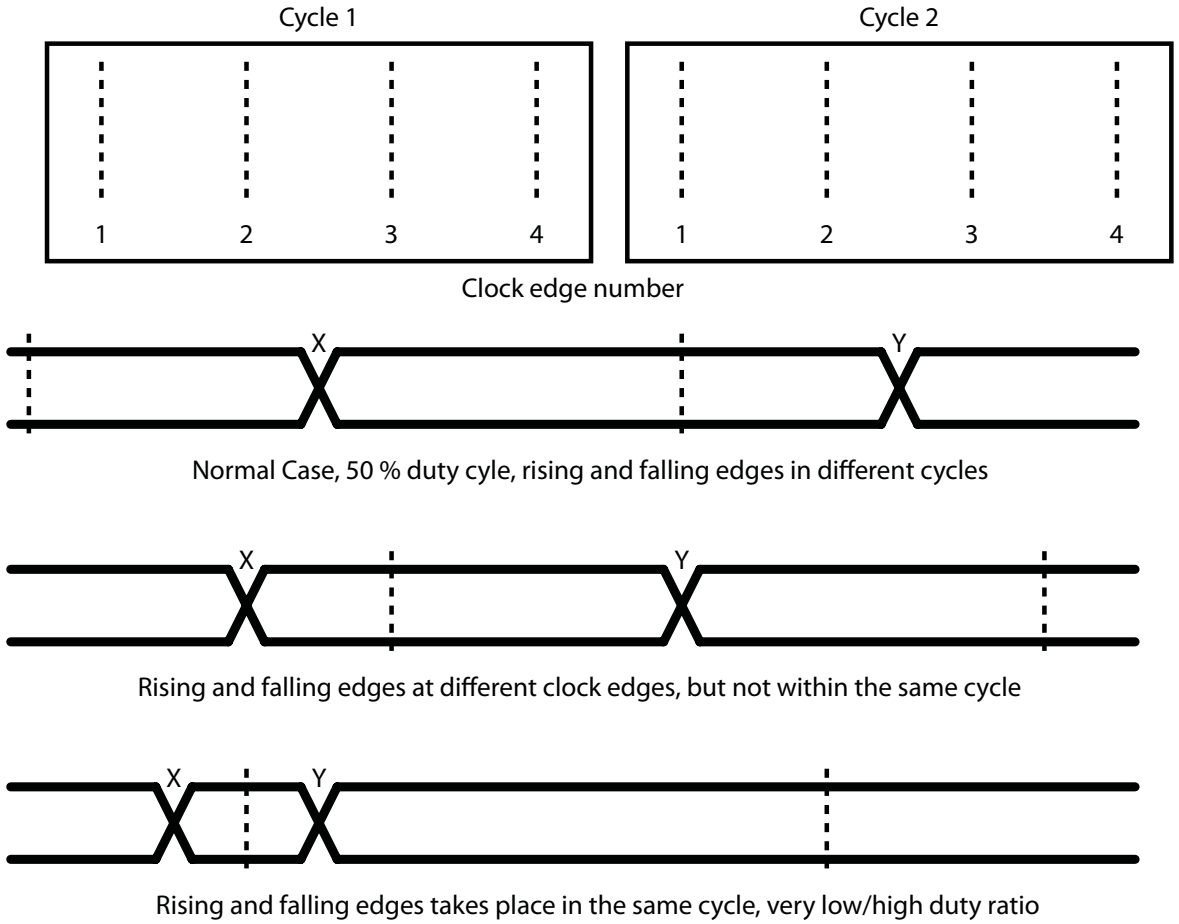

Figure 3: Phase Select

2.3 Design Details

The receiver implementation can be seen in Figure 2, the incoming data is oversampled by a factor of 4 and the correct clock phase for data sampling is determined based on the location of the rising and falling data edges in the phase select block. The concept of the phase selection is seen in Figure 3 showing how to calculate the optimal sampling instance depending on the transition points. This will compensate for skew and duty ratio variations of the incoming serial data sequence.

3 Area and performance requirements

The table below summarizes the circuit performance requirements. Each requirement has its number, formulated text, and the given degree of priority. Three degrees of priority are used: high, medium, and low. High is a firm requirement with no possibility of relaxation, while medium requirements can be relaxed somewhat after good motivation.

Requirement	Requirement text	Priority
1	Data rate of 500 MBit/s	Medium
2	Two modes of operation, transmit comma and transmit PRBS data	High
3	Comply with LVDS Standard	Medium
4	Integrate as many system components as possible on-chip	High
5	Schematic and layout must be verified by simulation	High
6	Chip core area < 0.27mm^2	High
7	Total project pin count: 12	High
8	Design technology is AMS 4-Metal 0.35μm CMOS	High
9	The most important system nodes should have off-chip access pins	Low
10	On-chip current densities < 1 mA/μm	High
11	All requirements fulfilled in *"typical"*, *"slow"*, and *"fast"* process corners and for temperatures between 25^{o}C and 110^{o}C	Medium

3.1 Available resources

- Scientific publication database (available from LiU):
- IEL – IEEE/IEE Electronic Library, http://www.bibl.liu.se/english/databas/

3.2 Tools

- Circuit simulation and layout tools from Cadence®, http://www.cadence.com/

4 References

- http://analog.postech.ac.kr/1.Nrl/2.NRL%20Seminar/invitation/040514_KangJG.pdf
- http://en.wikipedia.org/wiki/8b/10b_encoding

  contains good tables for 8b10b coding.
- J.M. Rabaey, A. Chandrakasan, and B. Nikolic., "Digital Integrated Circuits", 2nd ed., Prentice Hall, 2003, ISBN 0-13-120764-4.

For more literature references consult with your supervisor.

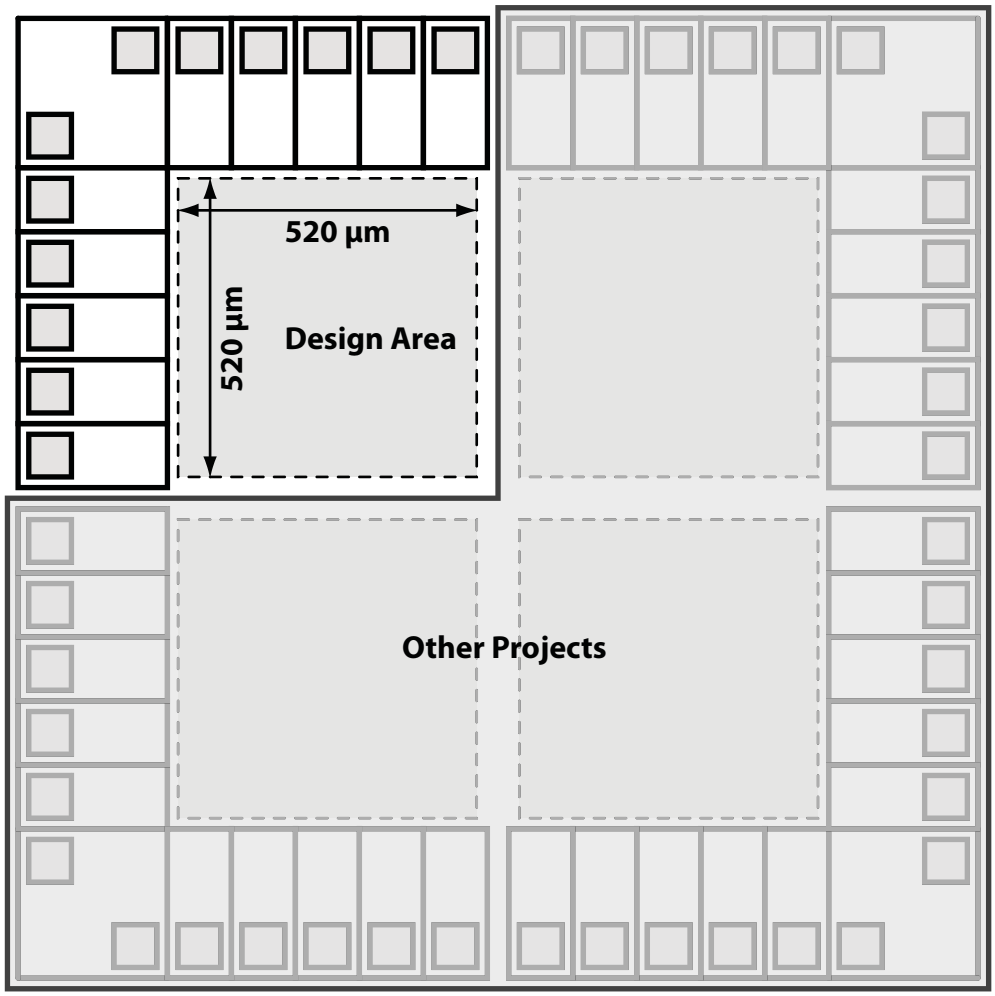

Figure 4: Schematic picture of a 3mm^2 chip highlighting one corner with 10 generic pads, one V_{DD} and one V_{SS} pad (total 12 per group). Four groups will then share one chip.