VLSI Chip Design Project TSEK06

Project description and requirement specification

Project: High-Speed 6-bit Digital-to-Analog Converter

Project number: 4

Project Group:

Name	Project members	Telephone	E-mail
	Project leader and designer 1(5)		
	Designer 2(5)		
	Designer 3(5)		
	Designer 4(5)		
	Designer 5(5)		

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1 Background

This document describes the design requirement specification of a 6-bit thermometer coded current steered digital-to-analog converter (DAC). The DAC is intended to operate at a frequency 700-1000 MHz and is to be implemented in a 0.35 um CMOS process. The 6-bit DAC should be implemented using a 4x4-switched current source matrix and 2 additional switched current sources, to realize a 6-bit conversion.

1.1 Project goal

The project goal is to design an integrated circuit (IC) in complementary metal-oxide semiconductor (CMOS) technology. Students, participating in this project as project members and project leaders, should learn the different steps of the IC design flow. That includes the given system architecture analysis, simulation, layout implementation and verification. The project students have an optional choice to manufacture the designed IC circuit on a chip. To test the manufactured chips, another course (TSEK11) is available after the project.

1.2 Milestones and deadline

1: Project selection	Week 3
2: Pre-study, project planning, and discussion with supervisor	Week 4
3: High-level modeling design and simulation result (report)	February 12
4: Gate/transistor level design and simulations result (report)	March 5
5: Layout, DRC, parasitic extraction, LVS, post-layout simulations, modification and chip evaluations.	April 30
6: **DEADLINE**, Delivery of the completed chip.	**May 7**
7: **DEADLINE**, Final report, and oral presentation	**May 21**

1.3 Parties

The following parties are involved in this project:
1. Customer: Jonas Fritzin
2. Project supervisor: Jonas Fritzin

Tasks:

- Formulates the project requirements
- Provides technical support
- Reviews the project documents

3. Project leader: One of the members in the design team
   Tasks:
   - Responsible for organization of the team and the project planning
   - Divides the design and documentation work in an efficient way
   - Organizes the team meetings as well as the meetings between the team and supervisor
   - Keeps the supervisor informed about the progress of the project (at least one e-mail or meeting per week
4. Project design members (including the project leader)
   Tasks:
   - Are equally responsible for project planning and design
   - Participate actively in all the meetings
   - Support the team and the project leader
   - Keep the team and project leader informed about the progress of their task

2 Project description

2.1 System description

A 6-bit DAC implemented with a switched current matrix is shown in figure 1. It consists of the current matrix controlled by the four most significant digital bits, and of a conventional 2-bit current source DAC. The conventional 2-bit DAC consists of two current sources, each with current I_0 and $2xI_0$, controlled by D0 and D1, respectively. The two LSB's directly controls two current sources, leading to that a current between 0 and $3xI_0$ floats to the analog output.

Making a 6-bit DAC using this conventional approach would lead to that the MSB current source would have to be very large to be able to handle a current of $32xI_0$. The current matrix approach instead makes it possible to use uniform size current sources, and then control how many current sources that should be active using D5-D2. The current that each current source in the matrix needs to handle is $4xI_0$. The 4 MSB then control the current source matrix, and by coding the four input bits to a thermometer code, that can control the matrix, a current between 0 and $60xI_0$ floats out to analog output, thus a total current region is 0 to $63xI_0$.

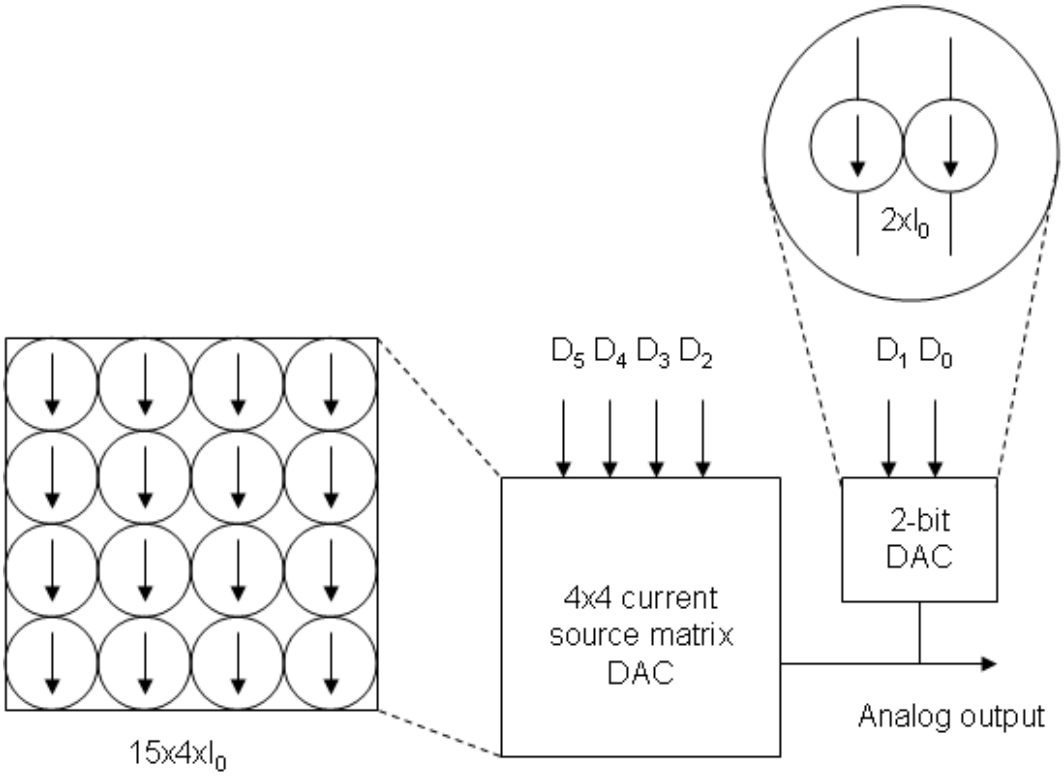

Figure 1. 6-bit DAC divided in 4x4 matrix DAC and a 2-bit DAC

The DAC should also include a calibration function on the current sources in the matrix, which uses an external calibration current to set the bias of the unit current sources. The calibration should be made on-the-fly, which means that the matrix needs one additional current source. In Figure 2 a block representation of the current source matrix including calibration is shown. The thermometer coder translates the four input bits to a 15-bit thermometer code. The control block then synchronizes the calibration, and determines which of the current sources that can be used, and which one is currently being calibrated. The calibration block then calibrates each current source, synchronously.

2.2 Important design metrics

The complete DAC should be optimized for high-speed, which sets high timing requirements for the digital parts of the design. The DAC should have good linearity, which further increases the demands on both the digital and analog parts.

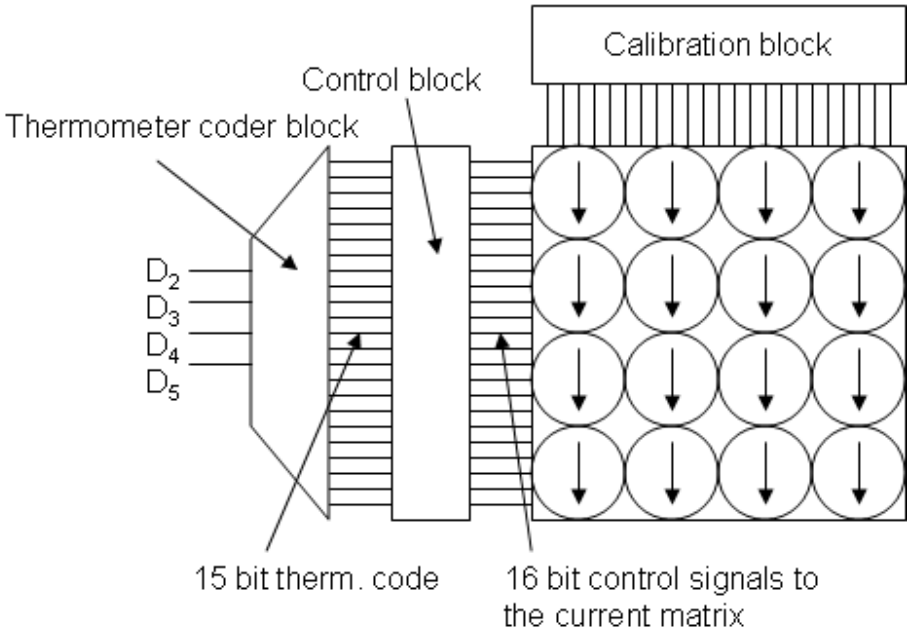

Figure 2. Block description of the current matrix, including control and calibration blocks

3 Area and performance requirements

The table below summarizes the DAC performance requirements. Each requirement has its number, date of change, formulated text and the given degree of priority. Three degrees of priority are used: high, low and medium. High is a firm requirement with no possibility of relaxation, while medium requirements can be relaxed somewhat after good motivation.

Requirement	**Requirement text**	**Priority**
1	Operation frequency 700 – 1000 MHz	High
2	Calibration of current source matrix	Medium
3	Integrate as many system components as possible on-chip	Medium
4	Design schematic and layout must be verified by simulation	High
5	Simulated chip power consumption < 400 mW at max. frequency	High
6	Chip core area < 0.150mm^2 (based on 5-6 projects per chip)	High
7	Total project pin count < 10-12 (prepare to share inputs)	High
8	Design technology is AMS 4-metal 0.35 um CMOS	High
9	The most important system nodes should have off-chip access pins	Low
10	On-chip current densities < 1mA/um	High
11	All requirements fulfilled in *"typical"*, *"slow"*, and *"fast"* process corners and for temperatures between 25^{o}C and 110^{o}C	Medium

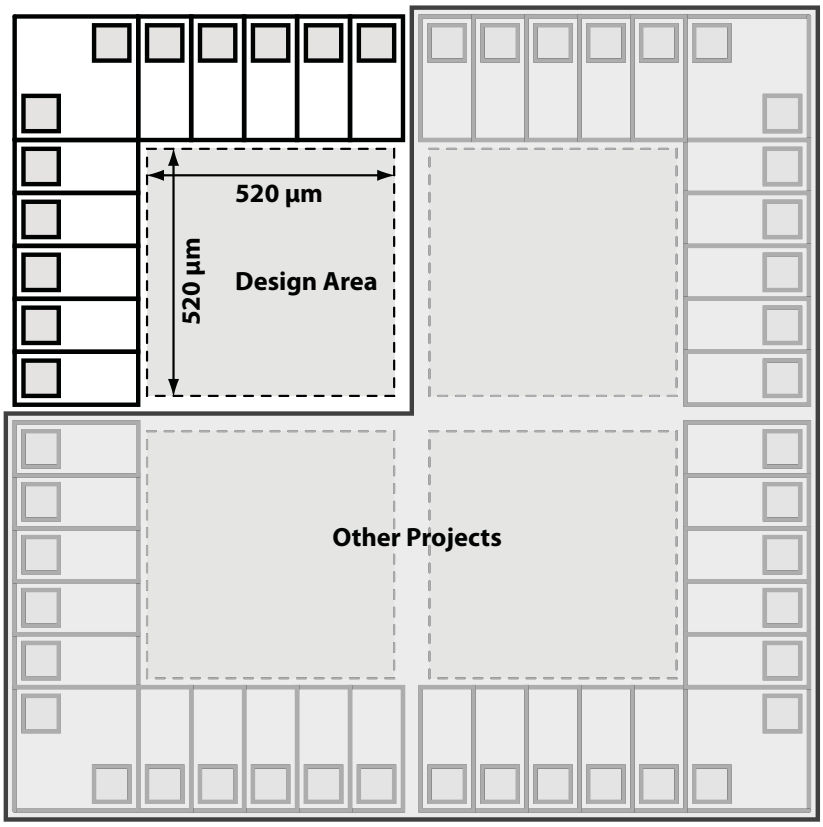

Figure 3. Schematic picture of a 3mm^2 chip with 40 generic pads four V_{DD} and four V_{SS} pads (total 48 pads), which will be shared between a number of projects.

3.1 Available resources

- Scientific publication database (available from LiU):
- IEL – IEEE/IEE Electronic Library, http://www.bibl.liu.se/english/databas/

3.2 Tools

- Circuit simulation and layout tools from Cadence®, http://www.cadence.com/

4 References

- J.M. Rabaey, A. Chandrakasan, and B. Nikolic., “Digital Integrated Circuits”, 2nd ed., Prentice Hall, 2003, ISBN 0-13-120764-4.
- N. Waste and K. Eshraghian, “Principles of CMOS VLSI Design”, Addison-Wesley, 1993.
- S.-M. Kang and Y. Leblebici, “CMOS Digital Integrated Circuits: Analysis and Design”, McGraw-Hill, 1999.
- B. Parhami, “Computer Arithmetic”, Oxford University Press, 2000.