VLSI Chip Design Project TSEK06

Project description and requirement specification

Project: Low Power PA

Project number: 8

Project Group:

Name	Project members	Telephone	E-mail
	Project leader and designer 1(5)		
	Designer 2(5)		
	Designer 3(5)		
	Designer 4(5)		
	Designer 5(5)		

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1 Background

This document describes the design requirement specification of a novel low power PA. The PA is found in the transmitter part of a radio transceiver, and is driving the antenna. The power amplifier is intended to transmit at 400 MHz with QPSK modulation.

The PA applies direct modulation, which dramatically reduces the complexity of a transmitter. All inputs, apart from the DC bias currents, to the PA are digital. With an external resonance circuit, harmonics are suppressed. The symbol value for a QPSK modulated signal depends on the phase. To reduce spectral regrowth, before the symbol value is changed, the PA power output amplitude is ramped down. Then the new phase is set and the output power is ramped up.

1.1 Research cooperation

The Low Power PA project is part of transmitter research cooperation between Zarlink Semiconductor Medical Product Group and Electronic Devices LiTH.

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1.2 Project goal

The project goal is to design an integrated circuit (IC) in complementary metal-oxide semiconductor (CMOS) technology. Students, participating in this project as project members and project leaders, should learn the different steps of the IC design flow. That includes the given system architecture analysis, simulation, layout implementation and verification. The project students have an optional choice to manufacture the designed IC circuit on a chip. To test the manufactured chips, another course (TSEK11) is available after the project.

1.3 Milestones and deadline

1: Project selection	Week 4
2: Pre-study, project planning, and discussion with supervisor	Week 5
3: High-level modeling design and simulation result (report)	February 6
4: Gate/transistor level design and simulations result (report)	March 6
5: Layout, DRC, parasitic extraction, LVS, post-layout simulations, modification, chip evaluations, and delivery of the completed chip	May 8
6: **DEADLINE**, Final report, and oral presentation	**May 20**

1.4 Parties

The following parties are involved in this project:

1. Customer: Jonas Fritzin

2. Project supervisor: Jonas Fritzin, Håkan Bengtsson
   Tasks:
   - Formulates the project requirements
   - Provides technical support
   - Reviews the project documents

3. Project leader: One of the members in the design team
   Tasks:
   - Responsible for organization of the team and the project planning
   - Divides the design and documentation work in an efficient way
   - Organizes the team meetings as well as the meetings between the team and supervisor
   - Keeps the supervisor informed about the progress of the project (at least one e-mail or meeting per week

4. Project design members (including the project leader)
   Tasks:
   - Are equally responsible for project planning and design
   - Participate actively in all the meetings
   - Support the team and the project leader
   - Keep the team and project leader informed about the progress of their task

2 Project description

2.1 System description

The PA chip is direct bonded on a pcb. The PA system, see figure 1, consists of the PA chip, a matching network and resonance circuit. As the parasitics for the bondpads, bondwires and pcb will affect the resonance frequency, the parasitics must be included during simulations. The chosen effective resonance frequency is 400 MHz.

The PA chip consists of a digital control, a current mirror and the amplifier. See figure 1. The digital control generates the internal clocks clk_p, clkb_p, clk_n and clkb_n, which clock the amplifier. The digital control also controls the ramping sequence by controlling the current mirror. The current mirror generates the internal currents ibias_int_source and ibias_int_sink, which bias the amplifier. The amplifier consists of two cmos inverters in a positive feedback configuration, see figure 2.

I, Q, IQ_clk, RF_clk and Ramptime are digital input signals to the PA chip. Ramptime can be one digital signal or a digital bus depending on desired ability to trim the ramptime. The digital baseband data signals, I and Q, are clocked with IQ_clk. The baseband data is modulated with RF_clk. The I and Q values set the phase of the QPSK RF_sig. The ramp time is set with Ramptime.

The analog bias currents are controlled with Ibias_source and Ibias_sink.

Vdd and Vss are the power supply.

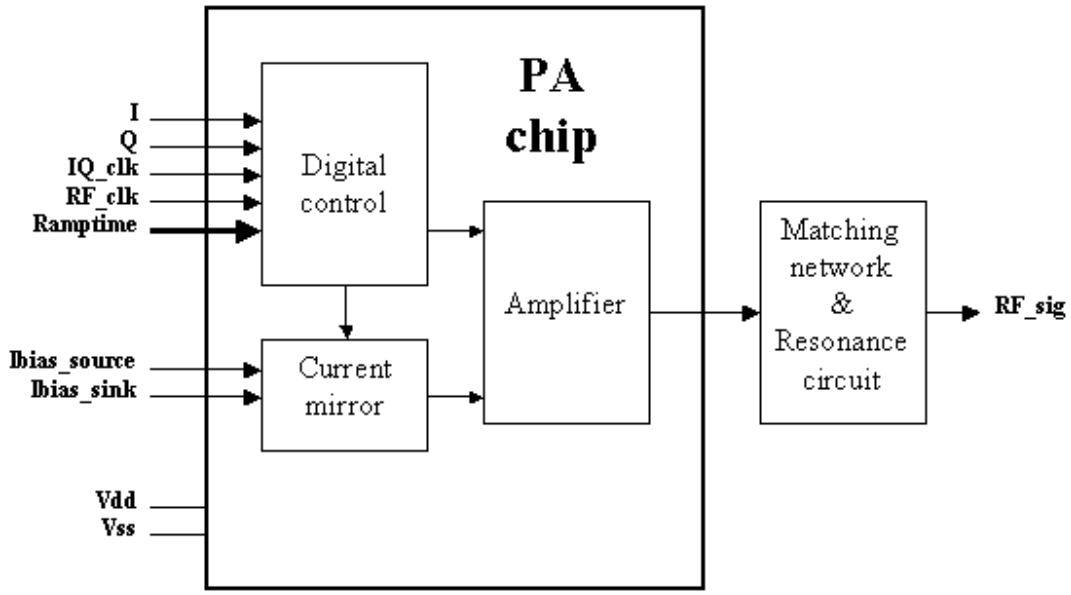

Figure 1. PA system.

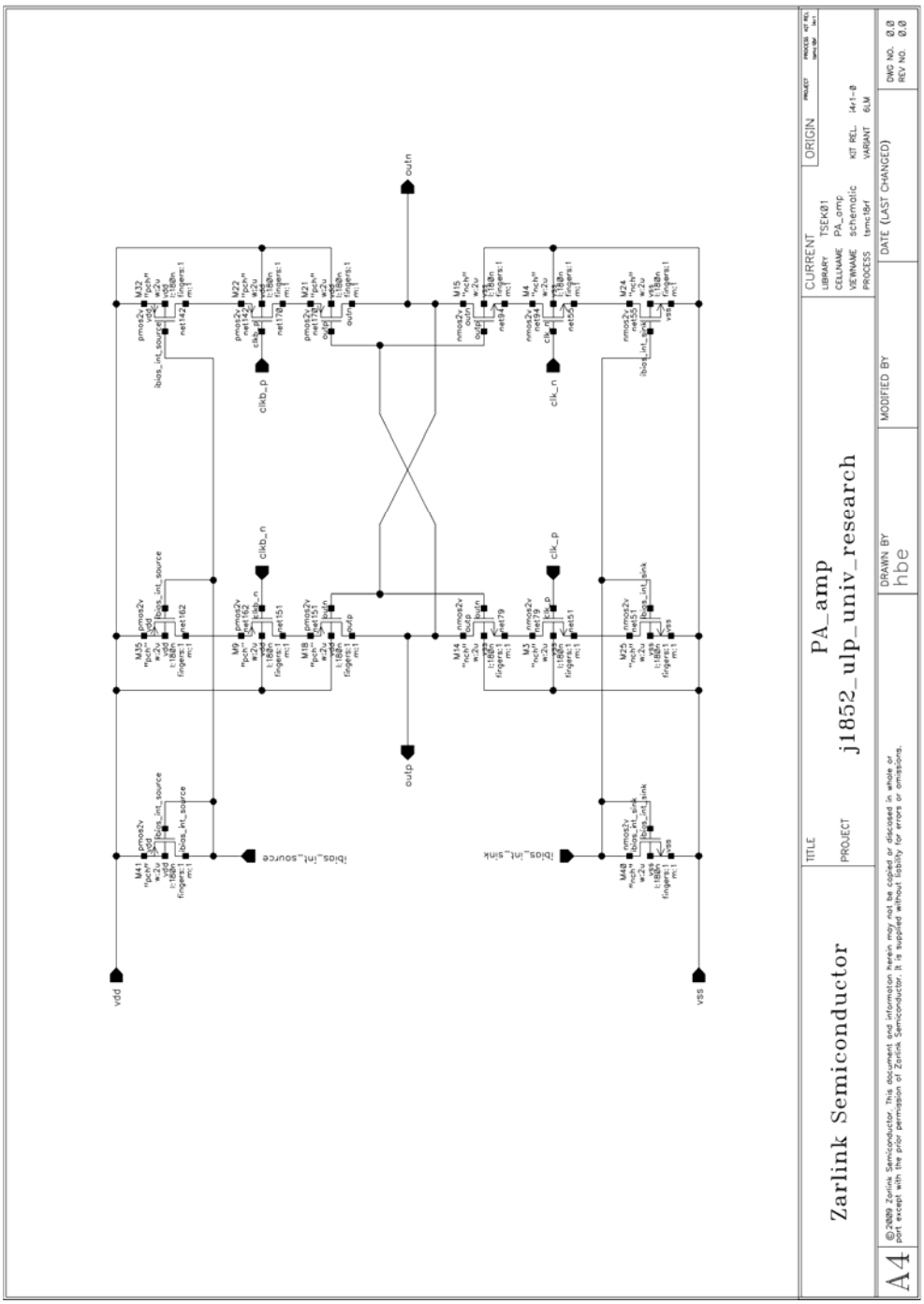

Figure 2. PA amplifier.

2.2 Important design metrics

During the design follow the following design metrics.

- Let the symbol rate be 1 Msymbol/s.
- Let the ramp up and ramp down times be able to trim between 20n to 320n.
- Let the ramping be linear staircase consisting of 16 steps.
- Design for 100 ohm differential load at the PA output RF_sig.
- Try to reach 50 % drain efficiency.
- Try to reach 30 dBc suppression of the third output harmonic.

3 Area and performance requirements

The table below summarizes the Low Power PA performance requirements. Each requirement has its number, date of change, formulated text and the given degree of priority. Three degrees of priority are used: high, low and medium. High is a firm requirement with no possibility of relaxation, while medium requirements can be relaxed somewhat after good motivation.

Requirement	Requirement text	Priority
1	Operation frequency 400 MHz	High
2	Design schematic and layout must be verified by simulation	High
3	Simulated chip power consumption < 400 mW at max. frequency	High
4	Chip core area < 0.150mm^2 (based on 5-6 projects per chip)	High
5	Total project pin count < 10-12 (prepare to share inputs) ?!?	High
6	Design technology is AMS 4-metal 0.35 um CMOS	High
7	On-chip current densities < 1mA/um	High
8	All requirements fulfilled in *"typical"*, *"slow"*, and *"fast"* process corners and for temperatures between 25^{o}C and 110^{o}C	Medium

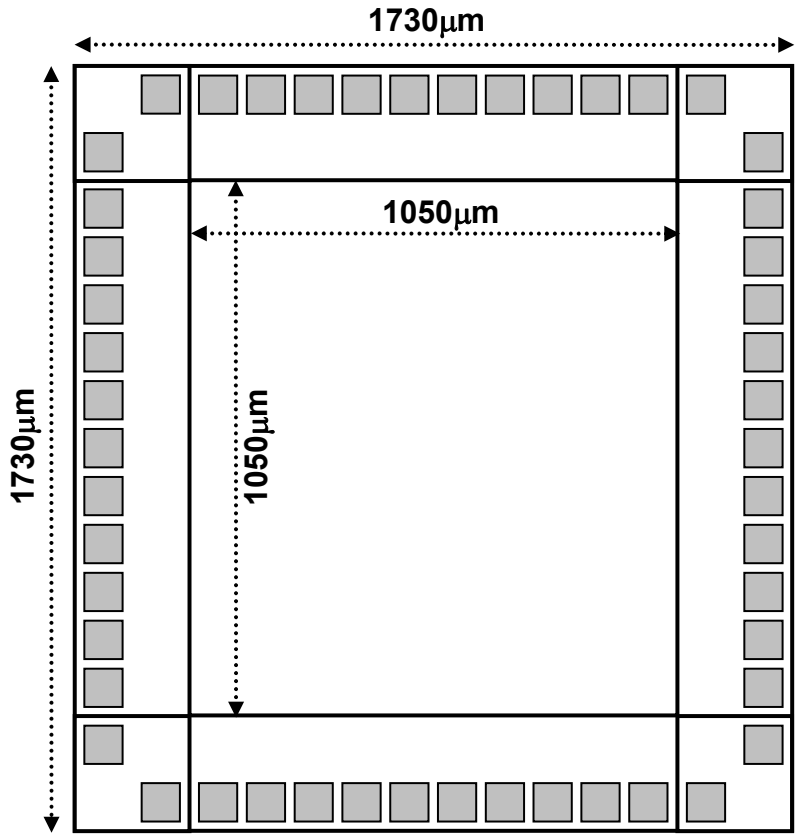

Figure 3. Schematic picture of a 3mm^2 chip with 40 generic pads four V_{DD} and four V_{SS} pads (total 48 pads), which will be shared between a number of projects.

3.1 Available resources

- Scientific publication database (available from LiU):
- IEL – IEEE/IEE Electronic Library, http://www.bibl.liu.se/english/databas/

3.2 Tools

- Circuit simulation and layout tools from Cadence®, http://www.cadence.com/

4 References

- J.M. Rabaey, A. Chandrakasan, and B. Nikolic., "Digital Integrated Circuits", 2nd ed., Prentice Hall, 2003, ISBN 0-13-120764-4.
- N. Waste and K. Eshraghian, "Principles of CMOS VLSI Design", Addison-Wesley, 1993.
- B. Razavi, "Design of analog cmos integrated circuits", McGraw-Hill, 2001.
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