VLSI Chip Design Project TSEK06

Project description and requirement specification

Version 1.0

Project: High Speed Current Mode Pipelined Analog-to-Digital Converter

Project number: 5

Project Group:

Name	Project members	Telephone	E-mail
	Project leader and designer 1(5)		
	Designer 2(5)		
	Designer 3(5)		
	Designer 4(5)		
	Designer 5(5)		

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1 Background

This document describes the design requirement specification of a High Speed Current Mode Pipelined Analog-to-Digital Converter. One of the bottlenecks in systems today is the data converters (A/D and D/A) required to move between analog and digital domain. A pipelined structure offers low power dissipation at medium-to-high resolutions. A further advantage of pipelined ADCs is the low input capacitance compared to fully parallel (flash) structures.

1.1 Project goal

The project goal is to design an integrated circuit (IC) in complementary metal-oxide semiconductor (CMOS) technology. Students, participating in this project as project members and project leaders, should learn the different steps of the IC design flow. That includes the given system architecture analysis, simulation, layout implementation and verification. The project students have an optional choice to manufacture the designed IC circuit on a chip. To test the manufactured chips, another course (TSEK11) is available after the project.

1.2 Milestones and deadline

1: Project selection	Week 4
2: Pre-study, project planning, and discussion with supervisor	Week 5
3: High-level modeling design and simulation result (report)	February 6
4: Gate/transistor level design and simulations result (report)	March 6
5: Layout, DRC, parasitic extraction, LVS, post-layout simulations, modification, chip evaluations, and delivery of the completed chip	May 8
6: **DEADLINE**, Final report, and oral presentation	**May 20**

1.3 Parties

The following parties are involved in this project:

1- Customer: Timmy Sundström
2- Project supervisor: Timmy Sundström

Tasks:

- Formulates the project requirements
- Provides technical support
- Reviews the project documents.

3- Project leader: One of the members in the design team.

Tasks:

- Responsible for organization of the team and the project planning.
- Divides the design and documentation work in an efficient way
- Organizes the team meetings as well as the meetings between the team and supervisor
- Keeps the supervisor informed about the progress of the project (**at least one email or meeting per week**)

4- Project design members (including the project leader)
- Are equally responsible for project planning and design.
- Participate actively in all the meetings
- Support the team and the project leader
- Keep the team and project leader informed about the progress of their tasks.

2 Project description

2.1 System description

The complete system to be built should be a working current-mode pipelined analog-to-digital converter. This project is a research project in that there will be no documented books or research papers describing the functionality and theory of the implemented solution.

A pipelined ADC is based on an iterative binary search for the analog value. The first stage compares the input signal to a reference voltage and then amplifies the residue. This is shown in Figure 1 for a 3-bit ADC, with an input voltage corresponding to the binary value 110. After comparing versus the first reference voltage the residue is multiplied by a factor of 2 and then the procedure is repeated.

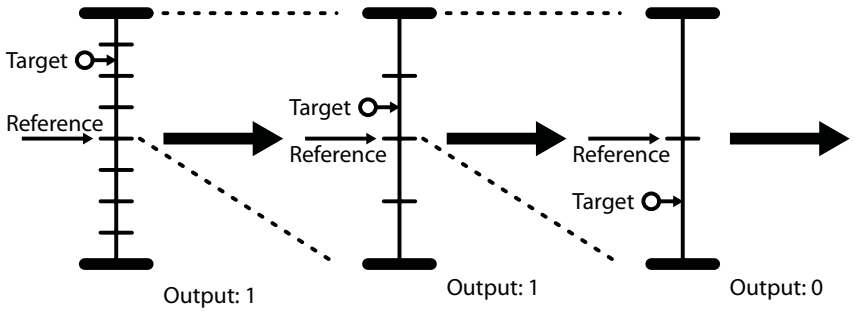

Figure 1: Pipelined functionality.

This has the advantage that all the stages of a pipelined ADC will be identical and we can add more stages until noise or mismatch will dominate the signal and we have reached the maximum resolution. A traditional pipelined ADC uses operational amplifiers connected in feed-back to implement the multiplication of two whereas the current-mode pipelined will utilize the straight forward approach of adding currents together to implement the multiplication. This will achieve a significant increase in conversion speed at the cost of increased sensitivity to mismatch and the need for accurate balance of the transistors.

When actually implemented not only 1 bit per stage is used but actually 1.5 bits is the most common choice as this will eliminate any errors caused by mismatch in the comparator circuits.

The current-mode principle is shown in Figure 2. The DC level of the input current is ignored and only the signal component, Δ, is amplified.

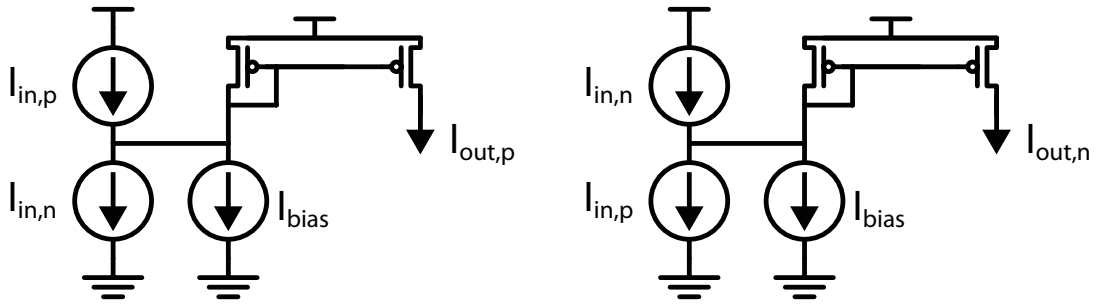

Figure 2: Differential current-mode pipeline stage.

$$I_{in,p} = I_{DC,input} + \Delta\,,\ I_{in,n} = I_{DC,input} - \Delta$$

$$I_{out,p} = I_{bias} + I_{in,n} - I_{in,p}\,,\ I_{out,n} = I_{bias} + I_{in,p} - I_{in,n}$$

$$I_{out,p} = I_{bias} + 2\Delta\,,\ I_{out,p} = I_{bias} - 2\Delta$$

2.2 Important design metrics

The circuit should be designed to for a sampling frequency of at least 100 MHz at an effective resolution of 8 bits

Important things to consider are:

- Timing, settling, and internal noise
- Precision in the ADC
- Finite transistor output impedance causing imperfect current mirrors
- Circuit techniques to improve linearity

3 Area and performance requirements

The table below summarizes the circuit performance requirements. Each requirement has its number, formulated text, and the given degree of priority. Three degrees of priority are used: high, medium, and low. High is a firm requirement with no possibility of relaxation, while medium requirements can be relaxed somewhat after good motivation.

Requirement	**Requirement text**	**Priority**
1	Sampling frequency at least 100MHz	High
2	Integrate as many system components as possible on-chip	High
3	Schematic and layout must be verified by simulation	High
4	Layout matching	High
5	Effective resolution of 8 bits	High
6	Chip core area < 0.27mm^2 (based on 4 projects per chip)	High
7	Total project pin count < 10-12 (prepare to share inputs)	High
8	Design technology is AMS 4-Metal 0.35µm CMOS	High
9	The most important system nodes should have off-chip access pins	Low
10	On-chip current densities < 1 mA/µm	High
11	All requirements fulfilled in *"typical"*, *"slow"*, and *"fast"* process corners and for temperatures between 25^{o}C and 110^{o}C	Medium

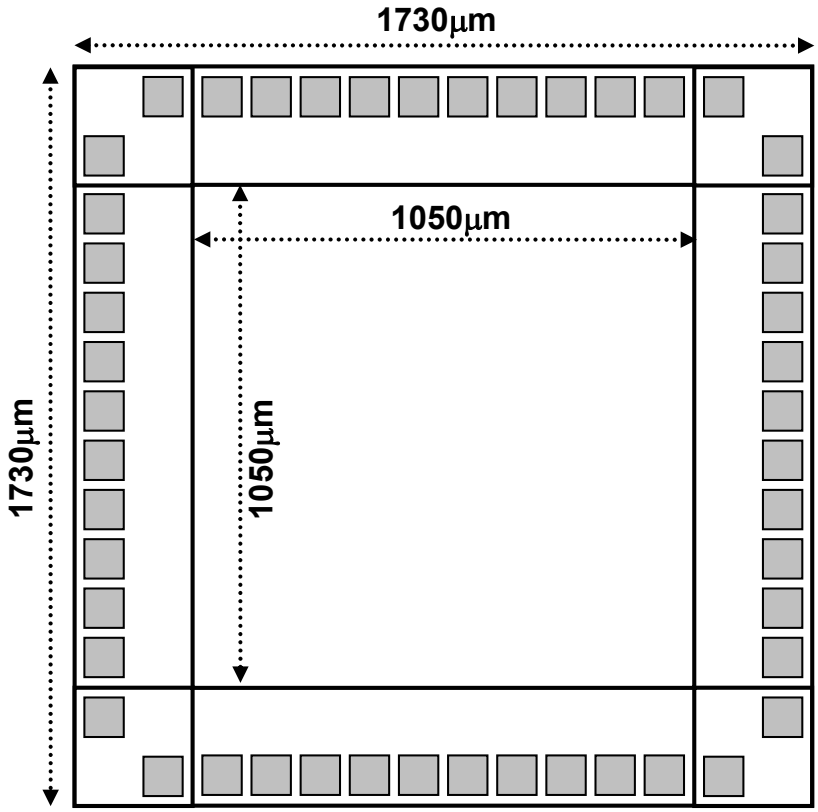

Figure 3: Schematic picture of a 3mm^2 chip with 40 generic pads four V_{DD} and four V_{SS} pads (total 48 pads), which will be shared between a number of projects.

3.1 Available resources

- Scientific publication database (available from LiU):
- IEL – IEEE/IEE Electronic Library, http://www.bibl.liu.se/english/databas/

3.2 Tools

- Circuit simulation and layout tools from Cadence®, http://www.cadence.com/

4 References

- http://pdfserv.maxim-ic.com/en/an/AN1023.pdf
- K, Poulton, "A 4Gsample/s 8b ADC in 0.35µm CMOS", in proceedings of International Solid-State Circuits Conference (ISSCC) 2002.
- B. Razavi, "Design of Analog CMOS Integrated Circuits", McGraw-Hill, 2001, ISBN 0-07-118839-8.
- J.M. Rabaey, A. Chandrakasan, and B. Nikolic., "Digital Integrated Circuits", 2nd ed., Prentice Hall, 2003, ISBN 0-13-120764-4.
- D.A. Johns and K. Martin, "Analog Integrated Circuit Design", John Wiley & Sons, 1997.

For more literature references consult with your supervisor.