VLSI Chip Design Project TSEK01

Project description and requirement specification

Version 1.0

Project: Beat Frequency Oscillator

Project number: 4

Project Group:

Name	Project members	Telephone	E-mail
	Project leader and designer 1(5)		
	Designer 2(5)		
	Designer 3(5)		
	Designer 4(5)		
	Designer 5(5)		

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1 Background

This document describes the design requirement specification of a beat frequency oscillator operating in RF range based on a phase-lock loop (PLL). The oscillator provides two tones spaced by the predefined frequency called the beat frequency, that can be used for on-chip test of radio front-ends and RF-blocks for linearity by measureing IM3 and IP3. In this design a PLL is used to synchronize an output signal generated by the summation of two different oscillators, with a reference signal in both frequency and phase. The PLL has a control loop that regulates the difference of two oscillator frequencies, so that the phase error is kept small. In this way the PLL can be used to generate two tones in RF range separated by the reference frequency (beat frequency). The beat frequency can be altered by changing the reference frequency while the tones can be shifted in frequency by the input control voltage of one of the oscillators.

1.1 Project goal

The project goal is to design an integrated circuit (IC) in complementary metal-oxide semiconductor (CMOS) technology. Students, participating in this project as project members and project leaders, should learn the different steps of the IC design flow. That includes the given system architecture analysis, simulation, layout implementation and verification. The project students have an optional choice to manufacture the designed IC circuit on a chip. To test the manufactured chips, another course (TSEK11) is available after the project.

1.2 Milestones and deadline

1: Project selection	Week 3
2: Pre-study, project planning, and discussion with supervisor	Week 4
3: High-level modeling design and simulation result (report)	February 15
4: Gate/transistor level design and simulations result (report)	March 5
5: Layout, DRC, parasitic extraction, LVS, post-layout simulations, modification, chip evaluations, and delivery of the completed chip	May 9
6: **DEADLINE**, Final report, and oral presentation	**May 23**

1.3 Parties

The following parties are involved in this project:

1- Customer: Shakeel Ahmad

2- Project supervisor: Shakeel Ahmad

Tasks:

- Formulates the project requirements
- Provides technical support
- Reviews the project documents

3- Project leader: One of the members in the design team.

Tasks:

- Responsible for organization of the team and the project planning.
- Divides the design and documentation work in an efficient way
- Organizes the team meetings as well as the meetings between the team and supervisor
- Keeps the supervisor informed about the progress of the project **(at least one e-mail or meeting per week)**

4- Project design members (including the project leader)

- Are equally responsible for project planning and design.
- Participate actively in all the meetings
- Support the team and the project leader
- Keep the team and project leader informed about the progress of their tasks.

2 Project description

2.1 System description

A block schematic of a PLL-based beat frequency oscillator is shown in Figure 1. The PLL will receive a reference clock (*Ref*) from an external source (signal generator). A phase-frequency detector (PFD) will compare the reference input with the beat frequency (*beat*). The outputs of the phase-frequency detector are up/down signals. The up/down signals controls a charge-pump (CP) that outputs a current-pulse, whose pulse-width is proportional to the phase/frequency-error. The current-pulse is filtered in a loop-filter (LPF1), which results in a control-voltage to control a voltage controlled oscillator (VCO2). The final output is generated as the summation of the two VCOs. Based on control voltage the beat frequency of the output signal *RF* is changed. The output is rectified using a diode, filtered in a low-pass filter (LPF2) and voltage level translated (LT) to generate the beat frequency. The input control-voltage of VCO1 is kept fixed for one set of tones and can be changed to shift the frequency spectrum.

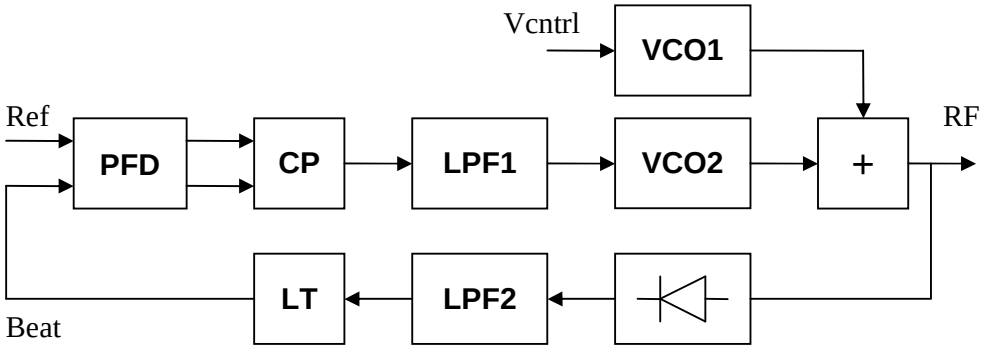

Figure 1: System Block diagram of Beat Frequency Oscillator

2.2 Important design metrics

Two identical VCOs will be used in the design. The VCO is a critical component in the PLL and must be designed so that the correct gain and frequency range can be assured across process and voltage corners. The charge-pump design is crucial to increase linearity and reduce spurious fluctuations. The loop-filter (LPF1) needs to be designed with the trade-off between phase-noise and PLL lock-time in mind, while low-pass filter (LPF2) must be

designed to suppress the high frequency components significantly. Further, the linearity of the rectifying component is also a major factor to achieve the desired phase-noise of output tones. Low-power is of utmost importance in this project, so all components in the PLL will be designed for lowest possible power.

3 Area, performance requirements

The table below summarizes the adder performance requirements. Each requirement has its number, formulated text, and the given degree of priority. Three degrees of priority are used: high, medium, and low. High is a firm requirement with no possibility of relaxation, while medium requirements can be relaxed somewhat after good motivation.

Requirement	**Requirement text**	**Priority**
1	Power supply voltage 3.3 V ± 5%	High
2	All components integrated on-chip	High
3	Schematic and layout must be verified by simulation	High
4	Output tone frequency range: 100 MHz to 1 GHz	Medium
5	Beat frequency range: 2 to 10 MHz	Medium
6	Stability of loop for different beat frequencies	High
7	Simulated PLL power consumption < 20mW	Medium
8	Chip core area < 0.150mm^2 (based on 5-6 projects per chip)	High
9	Total project pin count < 10-12 (be prepared to share inputs)	High
10	Design technology is AMS 4-Metal 0.35 µm CMOS High	High
11	The most important system nodes should have off-chip access pins	Medium
12	On-chip current densities < 1 mA/µm	High
13	All requirements fulfilled in *"typical"*, *"slow"*, and *"fast"* process corners and for temperatures between 25^{o}C and 110^{o}C	Medium

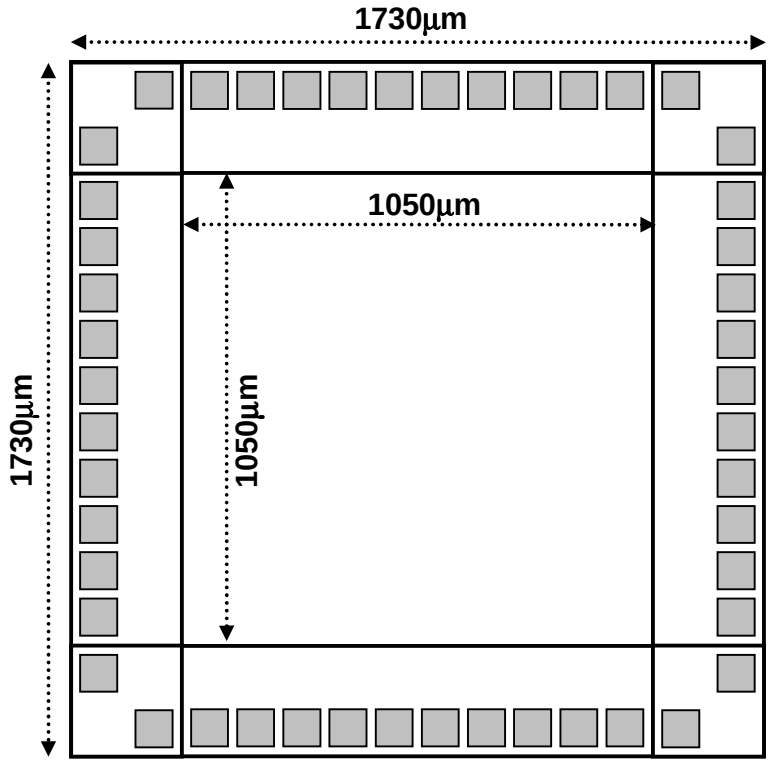

Figure 2: Schematic picture of a 3mm^2 chip with 40 generic pads four V_{DD} and four V_{SS} pads (total 48 pads), which will be shared between a number of projects.

3.1 Available resources

- Scientific publication database (available from LiU):

♦ IEL – IEEE/IEE Electronic Library, http://www.bibl.liu.se/english/databas/

3.2 Tools

♦ Circuit simulation and layout tools from Cadence®, http://www.cadence.com/

4 References

B. Razavi, “Design of Analog CMOS Integrated Circuits”, McGraw-Hill, 2001.

R.J. Baker, H.W. Li and D.E. Boyce, “CMOS Circuit Design, Layout, and Simulation”, IEEE Press, 1998.

For more literature references consult with your supervisor.