VLSI Chip Design Project TSEK01

Project description and requirement specification

Version 1.0

Project: Automatic gain control using VGA and Log Amplifier

Project number: 3

Project Group:

Name	Project members	Telephone	E-mail
	Project leader and designer 1(5)		
	Designer 2(5)		
	Designer 3(5)		
	Designer 4(5)		
	Designer 5(5)		

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1 Background

This document describes the design requirement specification of an Automatic gain control circuit that utilizes a broadband variable gain amplifier and a Log Amplifier. Automatic gain control (AGC) circuitry is an important building block in modern wireless communication systems. In a receiver (RX), it is desirable to maintain the same input level for the A/D converter at the receiver backend despite large input RF signal variations. AGC helps the receiver to adjust the gain to get the desired signal level at the intermediate frequency (IF) or baseband. In a transmitter (TX), the final transmit power level needs to be regulated due to the temperature and process variations. Wireless systems such as CDMA dynamically adjust the transmitter's power level to improve efficiency. Before AGC takes effect in either a TX or a RX, a way of monitoring the power level is needed. There are many ways to implement a power detector (PD). In this project, we will utilize a Log Amplifier with high dynamic range as a power detector along with a broadband VGA to implement the AGC function.

1.1 Project goal

The project goal is to design an integrated circuit (IC) in complementary metal-oxide semiconductor (CMOS) technology. Students, participating in this project as project members and project leaders, should learn the different steps of the IC design flow. That includes the given system architecture analysis, simulation, layout implementation and verification. The project students have an optional choice to manufacture the designed IC circuit on a chip. To test the manufactured chips, another course (TSEK11) is available after the project.

1.2 Milestones and deadline

1: Project selection	Week 3
2: Pre-study, project planning, and discussion with supervisor	Week 4
3: High-level modeling design and simulation result (report)	February 15
4: Gate/transistor level design and simulations result (report)	March 5
5: Layout, DRC, parasitic extraction, LVS, post-layout simulations, modification, chip evaluations, and delivery of the completed chip	May 9
6: **DEADLINE**, Final report, and oral presentation	**May 23**

1.3 Parties

The following parties are involved in this project:

1- Customer: Naveed Ahsan
2- Project supervisor: Naveed Ahsan

Tasks:

- Formulates the project requirements
- Provides technical support
- Reviews the project documents

3- Project leader: One of the members in the design team.

Tasks:

- Responsible for organization of the team and the project planning.
- Divides the design and documentation work in an efficient way
- Organizes the team meetings as well as the meetings between the team and supervisor
- Keeps the supervisor informed about the progress of the project **(at least one e-mail or meeting per week)**

4- Project design members (including the project leader)

- Are equally responsible for project planning and design.
- Participate actively in all the meetings
- Support the team and the project leader
- Keep the team and project leader informed about the progress of their tasks.

2 Project description

2.1 System description

In modern wireless communication systems there is a requirement to monitor and control signal power in the *transmit* and *receive* sections of the circuit, Transmitted power must be controlled to protect the power amplifier (PA) from overheating if it transmits too much power or consumes an excessive amount of current, and to satisfy Federal Communications Commission (FCC) standards for maximum emissions. Receive power must also be measured and controlled due to the wide dynamic range of the signals appearing at the antenna. This wide range is typically caused by movement of the signal source towards or away from the receiver, and by changes in weather conditions. In the end, the goal is to present the analog-to-digital converter (ADC) with a signal that has the highest possible signal-to-noise ratio (SNR). This is generally done using variable gain amplifiers (VGA) in an automatic gain control (AGC) loop.

This project will focus on an automatic gain control circuit based on broadband VGA and a Log amplifier. The system block level diagram is shown in Figure 1. For receiver AGC the proposed IF frequency band is from 1MHz to 10MHz. For transmitter case, the max TX frequency is set to be 500MHz. Therefore, the proposed circuit should perform well from 1MHz to 500MHz in order to meet both TX and RX AGC requirements.

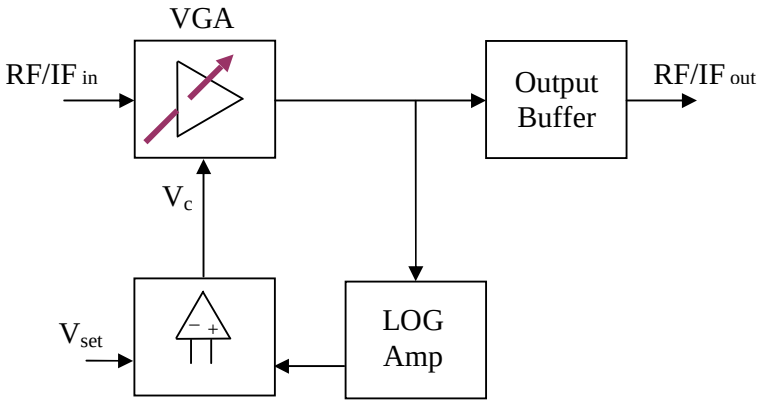

Figure 1: Block diagram of AGC using VGA and log amplifier detector.

Figure 2 shows the block diagram of a Log Amplifier detector. The Log Amplifier is made from a cascaded chain of amplifiers. These amplifiers have linear gain, usually around 10dB. For simplicity, Figure 2 shows a chain of five amplifiers, each with a gain of 10dB. With a small signal at the input, the first amplifier will provide a gain of 10dB. As the signal passes through each subsequent stage, it is amplified by an additional 10dB. At some point the log amp will no longer be able to apply additional gain to the input signal, and will begin to clip or limit at a precise level set by the designer. Once the signal has gone into limiting in one of the stages, the limited signal continues down the signal chain, maintaining its same peak amplitude. The output of each amplifier stage is also connected to a rectifier (marked Det in Figure 2). All of the rectifier outputs are added together, and the resultant sum is low-pass filtered to remove the ripple of the rectified signal. This produces the logarithmic output (often referred to as the *video* output), which will be a steady state dc output for a steady-state ac input signal. The number of cascaded amplifier stages will be decided after initial simulation results and as a rough estimate, it would be between 5 and 10 in order to get 60dB dynamic range.

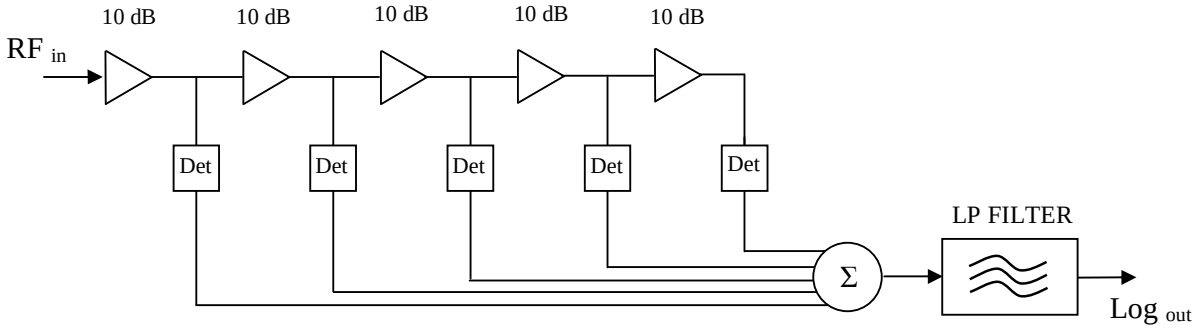

Figure 2: Block diagram of Log Amplifier detector.

2.2 Important design metrics

The proposed idea is to implement the AGC function and also to characterize the broad band Amplifier and Log Amplifier separately. The important design parameters for a power detector include: dynamic range, linearity, operating frequency, power consumption, and ease of integration. Following are some of the design specifications:

Vdd	= 3.0V
Amplifier BW	= 1MHz-500MHz
Input Impedance	= 50Ω
Output Impedance	= 50Ω
Dynamic range	= 60dB
Detector response time	= <20ns
Power consumption	= < 500 mW

This project covers many important design challenges that are present in analog circuit design. Design of a low power and a linear AGC circuit would be a nice challenge for the students.

3 Area, performance requirements

The table below summarizes the adder performance requirements. Each requirement has its number, formulated text, and the given degree of priority. Three degrees of priority are used: high, medium, and low. High is a firm requirement with no possibility of relaxation, while medium requirements can be relaxed somewhat after good motivation.

Requirement	**Requirement text**	**Priority**
1	Design for full functionality	Medium
2	Linearity test	Medium
3	Integrate as many system components as possible on-chip	High
4	Schematic and layout must be verified by simulation	High
5	Separate testing of VGA and Log Amplifier	High
6	Chip core area < 0.150mm^2 (based on 5-6 projects per chip)	High
7	Total project pin count < 10-12 (prepare to share inputs)	High
8	Design technology is AMS 4-Metal 0.35µm CMOS	High
9	The most important system nodes should have off-chip access pins	Medium
10	On-chip current densities < 1mA/µm	High
11	All requirements fulfilled in *"typical"*, *"slow"*, and *"fast"* process corners and for temperatures between 25^{o}C and 110^{o}C	Medium

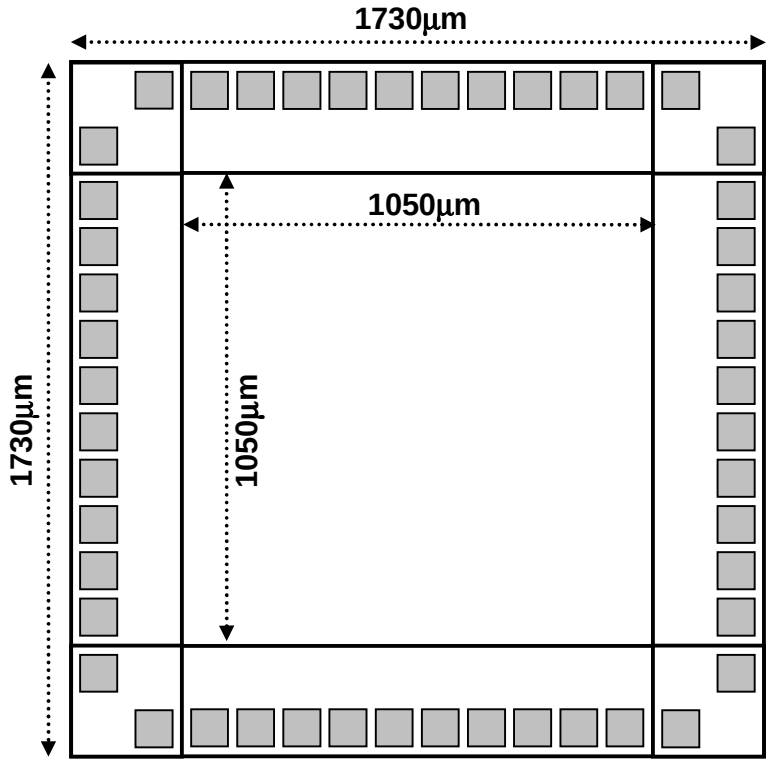

Figure 2: Schematic picture of a 3mm^2 chip with 40 generic pads four V_{DD} and four V_{SS} pads (total 48 pads), which will be shared between a number of projects.

3.1 Available resources

- Scientific publication database (available from LiU):

♦ IEL – IEEE/IEE Electronic Library, http://www.bibl.liu.se/english/databas/

3.2 Tools

♦ Circuit simulation and layout tools from Cadence®, http://www.cadence.com/

4 References

J.M. Rabaey, A. Chandrakasan, and B. Nikolic., "Digital Integrated Circuits", 2nd ed., Prentice Hall, 2003, ISBN 0-13-120764-4.

N. Waste and K. Eshraghian, "Principles of CMOS VLSI Design", Addison-Wesley, 1993.

S.-M. Kang and Y. Leblebici, "CMOS Digital Integrated Circuits: Analysis and Design", McGraw-Hill, 1999.

For more literature references consult with your supervisor.