# VLSI Chip Design Project TSEK01

## Project description and requirement specification

**Version 1.0**

## Project: Fractional Dividing Phase-Locked Loop (PLL)

## Project number: 4

### Project Group:

| Name | Project members | Telephone | E-mail |
|---|---|---|---|
| | Project leader and designer 1(5) | | |
| | Designer 2(5) | | |
| | Designer 3(5) | | |
| | Designer 4(5) | | |
| | Designer 5(5) | | |

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# 1 Background

This document describes the design requirement specification of a fractional dividing Phase Lock Loop (PLL). A PLL is a circuit that synchronizes an output signal generated by an oscillator, with a reference signal in both frequency and phase. The PLL has a control loop that regulates the oscillator frequency so that the phase error is kept small. A PLL can be used as a frequency multiplier, which multiplies the frequency of an input signal with some ratio. A fractional division circuit divides on average by a fractional number N/M, where N and M are integers.

## *1.1 Project goal*

The project goal is to design an integrated circuit (IC) in complementary metal-oxide semiconductor (CMOS) technology. Students, participating in this project as project members and project leaders, should learn the different steps of the IC design flow. That includes the given system architecture analysis, simulation, layout implementation and verification. The project students have an optional choice to manufacture the designed IC circuit on a chip. To test the manufactured chips, another course (TSEK11) is available after the project.

## *1.2 Milestones and deadline*

| | |
|---|---|
| 1: Project selection | Week 3 |
| 2: Pre-study, project planning, and discussion with supervisor | Week 4 |
| 3: High-level modeling design and simulation result (report) | February 16 |
| 4: Gate/transistor level design and simulations result (report) | March 7 |
| 5: Layout, DRC, parasitic extraction, LVS, post-layout simulations, modification, chip evaluations, and delivery of the completed chip | May 11 |
| 6: **DEADLINE**, Final report, and oral presentation | **May 25** |

## *1.3 Parties*

The following parties are involved in this project:

1- **Customer:** Henrik Fredriksson

2- **Project supervisor:** Henrik Fredriksson
Tasks:
- Formulates the project requirements
- Provides technical support
- Reviews the project documents.

3- **Project leader:** One of the members in the design team.
Tasks:
- Responsible for organization of the team and the project planning.
- Divides the design and documentation work in an efficient way
- Organizes the team meetings as well as the meetings between the team and supervisor

- Keeps the supervisor informed about the progress of the project (at least one email or meeting per week)

**4- Project design members (including the project leader)**

Tasks:

- Are equally responsible for project planning and design.
- Participate actively in all the meetings
- Support the team and the project leader
- Keep the team and project leader informed about the progress of their tasks.

# 2 Project description

## *2.1 System description*

A block schematic of a fractional dividing PLL is shown in Figure 1. The PLL will receive a reference clock (*Ref*) from an external source (crystal or other). A phase-detector (PD) will compare the phase of the reference with the divided version of the RF clock (*ClkRF*). The outputs of the phase detector are up/down signals. The up/down signals controls a charge-pump (CP) that outputs a current-pulse, whose pulse-width is proportional to the phase-error. The current-pulse is filtered in a loop-filter (LPF), which results in a control-voltage that is controlling a voltage-controlled oscillator (VCO). Based on the control voltage the frequency of the signal *ClkRF* is changed. The "1/N or 1/N+1"-block and the "Modulus counter" block divides the RF signal with an integer value. The fractional accumulator change the division value to create a divided frequency that on the average is a fractional value. The compensation DAC compensates for phase errors that will appear because of the fractional division.

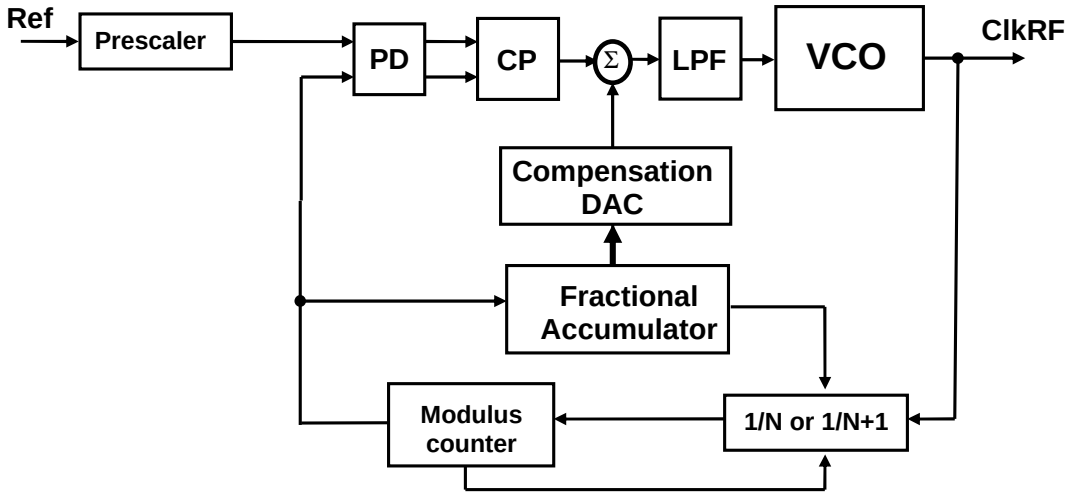


**Figure 1: Block diagram of PLL-based BFSK modulator**

## *2.2 Important design metrics*

The VCO is a critical component in the PLL and must be designed for high linearity and good frequency tunability across different process and voltage corners. The charge-pump design is crucial to reduce spurious fluctuations on the output clock signal. The loop-filter needs to be designed with the trade-off between phase-noise and PLL speed in mind. Further, the prescalers and dividers (frequency dividers) require extensive timing and performance

analysis to reach required performance. Low-power is of utmost importance in this project, so all components in the PLL will be designed for lowest possible power.

# 3 Area, performance requirements

The table below summarizes the adder performance requirements. Each requirement has its number, formulated text, and the given degree of priority. Three degrees of priority are used: high, medium, and low. High is a firm requirement with no possibility of relaxation, while medium requirements can be relaxed somewhat after good motivation.

| **Requirement** | **Requirement text** | **Priority** |
|---|---|---|
| **1** | Power supply voltage 3.3 V ± 5% | High |
| **2** | All components integrated on-chip | High |
| **3** | Schematic and layout must be verified by simulation | High |
| **4** | Center frequency 400MHz | Medium |
| **5** | Simulated PLL power consumption < 20mW | Medium |
| **6** | Chip design area < 0.75 $mm^2$ (see Figure 2) | High |
| **7** | Chip core area < 500μm x 550μm = 0.275$mm^2$ (see Figure 2) | High |
| **8** | Total project pin count < 12-13 (max 10-11 active+2 power supply) | High |
| **9** | Design technology is AMS 4-Metal 0.35 μm CMOS | High |
| **10** | The most important system nodes should have off-chip access pins | Medium |
| **11** | On-chip current densities < 1 mA/μm | High |

- All requirements in the table should be fulfilled in “typical”, “slow”, and “fast” process corners and temperature between 25 and 110 $^oC$.

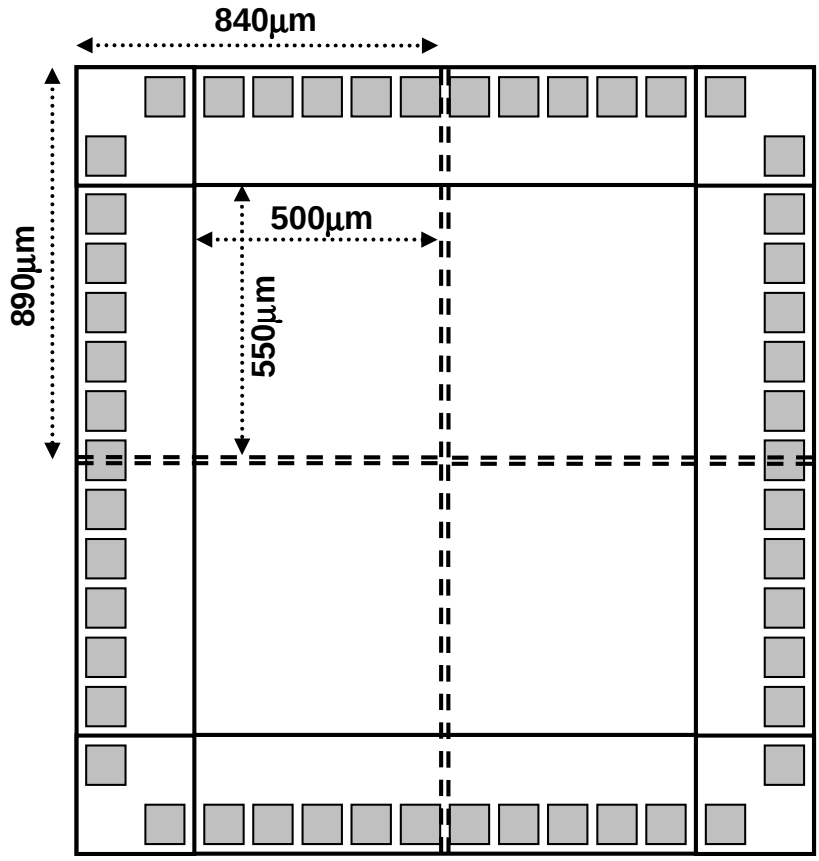


**Figure 2: A 3mm$^2$ chip will be shared by 4 independent projects (4 teams). Each project will utilize a 500x550µm$^2$ area for core layout and 12-13 pads.**

### *3.1 Available resources*

- Scientific publication database (available from LiU):

♦ IEL – IEEE/IEE Electronic Library, http://www.bibl.liu.se/english/databas/

### *3.2 Tools*

♦ Circuit simulation and layout tools from Cadence®, http://www.cadence.com/

# 4 References

B. Razavi, “Design of Analog CMOS Integrated Circuits”, McGraw-Hill, 2001.

R.J. Baker, H.W. Li and D.E. Boyce, ”CMOS Circuit Design, Layout, and Simulation”, IEEE Press, 1998.

For more literature references consult with your supervisor.