# VLSI design project, TSEK01

## Project description and requirement specification

**Version 1.0**

## Project: A First-Order Sigma-Delta Modulator with 3-bit Quantizer

## Project number: 5

### Project Group:

| Name | Project members | Telephone | E-mail |
|---|---|---|---|
| | Project leader and designer 1(4) | | |
| | Designer 2(4) | | |
| | Designer 3(4) | | |
| | Designer 4(4) | | |

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# 1 Background

This document describes the design requirement specification of a First-Order Sigma-Delta modulator with a 3-bit quantizer (3-bit ADC). One of the bottlenecks in systems today is the data converters (A/D and D/A) required to move between analog and digital domain. Instead of using an ADC with a large number of bits, which is tough to design because of matching requirements, an oversampled low resolution ADC together with noise-shaping can be used. Sigma-Delta converters are commonly used today when the bandwidth of the input signal is less than 1MHz. The main issue with Sigma-Delta ADCs is the need of oversampling. As one can understand there is of cause a limit what we can do in terms of oversampling frequency.

## *1.1 Project goal*

The project goal is to design an integrated circuit (IC) in complementary metal-oxide semiconductor (CMOS) technology. Students, participating in this project as project members and project leaders, should learn the different steps of the IC design flow. That includes the given system architecture analysis, simulation, layout implementation and verification. The project students have an optional choice to manufacture the designed IC circuit on a chip. To test the manufactured chips, another course (TSEK10) is available after the project.

## *1.2 Milestones and deadline*

| | |
|---|---|
| 1: Project selection | Week 3 |
| 2: Pre-study, project planning, and discussion with supervisor | Week 4 |
| 3: High-level modeling design and simulation result (report) | February 10 |
| 4: Gate/transistor level design and simulations result (report) | March 10 |
| 5: Layout, DRC, parasitic extraction, LVS, post-layout simulations, modification, chip evaluations, and delivery of the completed chip | May 12 |
| 6: **DEADLINE**, Final report, and oral presentation | May 26 |

## *1.3 Parties*

The following parties are involved in this project:

1- Customer: Stefan Andersson
2- Project supervisor: Stefan Andersson

Tasks:

- Formulates the project requirements
- Provides technical support
- Reviews the project documents.

3- Project leader: One of the members in the design team.

Tasks:

- Responsible for organization of the team and the project planning.

- Divides the design and documentation work in an efficient way
- Organizes the team meetings as well as the meetings between the team and supervisor
- Keeps the supervisor informed about the progress of the project (at least one email or meeting per week)

4- Project design members (including the project leader)

- Are equally responsible for project planning and design.
- Participate actively in all the meetings
- Support the team and the project leader
- Keep the team and project leader informed about the progress of their tasks.

# 2 Project description

## *2.1 System description*

The complete system to be built should be a working first-order Sigma-Delta modulator. The total system is shown in Figure 1. The main components to be designed are an integrator, a 3-bit flash-ADC, and a 3-bit DAC. The switched-cap integrators require an Operational amplifier (OP). A schematic of a suitable OP will be given to you in order to save some time. The digital filter that is needed after the Sigma-Delta modulator can be done in Matlab when doing chip measurements.

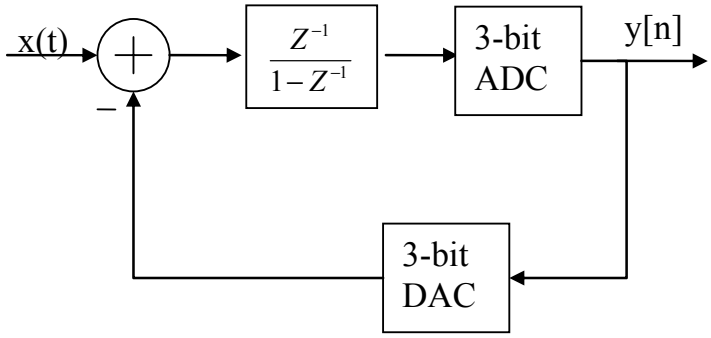


**Figure 1: First-order Sigma-Delta modulator architecture.**

The target for this design will be to achieve about 55-60dB dynamic range over a 500kHz bandwidth. The dynamic range (SNR=Signal-to-noise ratio) that can achieved with a first-order Sigma-Delta modulator can be calculated as

$$SNR = 6.02 \cdot N + 1.76 - 5.17 + 30\log(OSR)$$

Where N is the number of bits from the quantizer, and OSR is the oversampling ratio (X times the nyquist frequency). Using a sampling frequency of 32MHz (OSR = 32 MHz / (2 * 500 kHz) = 32) gives an SNR of about 60dB. This is equivalent with a 9.6-bit ADC!

### *2.2 Important design metrics*

The circuit must be designed for a sampling frequency of at least 32MHz. This will be translated to requirements on the integrators, 3-bit quantizer, and the 3-bit DAC. Important things to consider are:

- Timing, settling, and internal noise in the integrators
- Precision in the ADC
- The structure is also sensitive to settling- and matching-errors in the DAC
- Furthermore, the power-consumption is of large interest and should be minimized.

# 3 Area, performance requirements

The table below summarizes the circuit performance requirements. Each requirement has its number, formulated text, and the given degree of priority. Three degrees of priority are used: high, medium, and low. High is a firm requirement with no possibility of relaxation, while medium requirements can be relaxed somewhat after good motivation.

| Requirement | Requirement text | Priority |
|---|---|---|
| 1 | Sampling frequency at least 32MHz | High |
| 2 | Integrate as many system components as possible on-chip | High |
| 3 | Schematic and layout must be verified by simulation | High |
| 4 | Layout matching | High |
| 5 | Simulated chip power consumption < 100mW at max. freq. | Medium |
| 6 | Cooperation with the group designing the digital decimation filter | Low |
| 7 | Chip design area ~ 1.2 $mm^2$ (see Figure 2) | Medium |
| 8 | Chip core area < 700μm x 800μm = 0.56$mm^2$ (see Figure 2) | High |
| 9 | Total project pin count < 17 (max 15 active + 2 power supply) | High |
| 10 | Design technology is AMS 4-Metal 0.35 μm CMOS | High |
| 11 | The most important system nodes should have off-chip access pins | Low |
| 12 | On-chip current densities < 1 mA/μm | High |

- All requirements in the table should be fulfilled in “typical”, “slow”, and “fast” process corners and temperature between 25 and 110 $^oC$

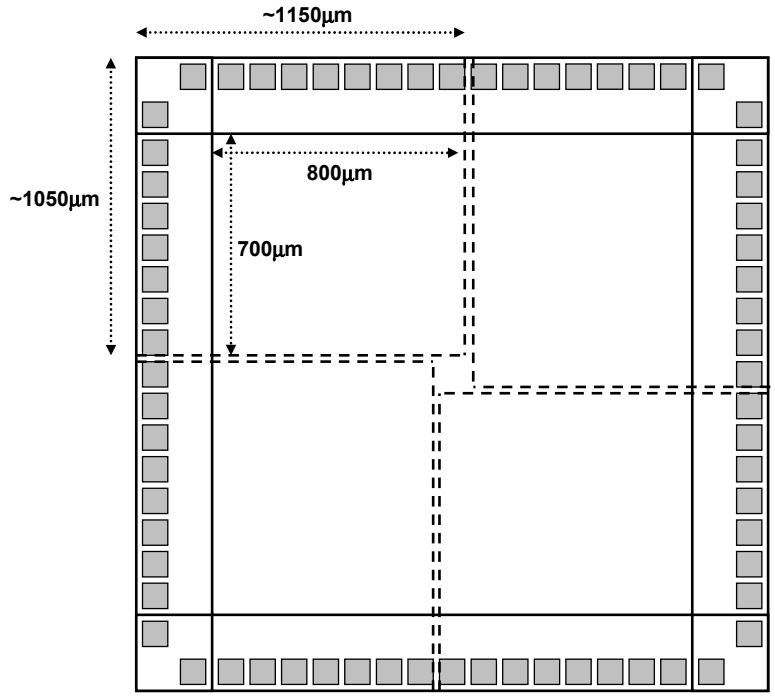


**Figure 2: A 5mm$^2$ chip will be shared by 4 independent projects (4 teams). Each project will utilize a 700x800µm$^2$ area for core layout and 17 pads.**

### *3.1 Available resources*

- Scientific publication database (available from LiU):

♦ IEL – IEEE/IEE Electronic Library, http://www.bibl.liu.se/english/databas/

### *3.2 Tools*

♦ Circuit simulation and layout tools from Cadence®, http://www.cadence.com/

# 4 References

- J.M. Rabaey, A. Chandrakasan, and B. Nikolic., "Digital Integrated Circuits", 2nd ed., Prentice Hall, 2003, ISBN 0-13-120764-4.

- D.A. Johns and K. Martin, "Analog Integrated Circuit Design", John Wiley & Sons, 1997.

- A 12-mW ADC delta-sigma modulator with 80 dB of dynamic range integrated in a single-chip Bluetooth transceiver; Grilo,J.;Galton,I.;Wang,K.;Montemayor,R.G.; Solid-State Circuits, IEEE Journal of , Volume:37, Issue:3, March2002 Pages:271 – 278

- Delta-sigma data conversion in wireless transceivers
  *Galton, I.;* Microwave Theory and Techniques, IEEE Transactions on , Volume: 50 , Issue: 1 , Jan. 2002 Pages:302 - 315

For more literature references consult with your supervisor.