VLSI Chip Design Project TSEK01

Project description and requirement specification

Version 1.0

Project: 250mW ISM Band Class D/E Power Amplifier

Project number: 4

Project Group:

Name	Project members	Telephone	E-mail
	Project leader and designer 1(5)		
	Designer 2(5)		
	Designer 3(5)		
	Designer 4(5)		
	Designer 5(5)		

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1 Background

This document describes the system design requirement specification of a Low power voice, data and picture transmitter for mobile robots. It also describes the Power Amplifier (PA) which is the integral part of this transmitter. Mobile robots have two way communication links with the base station. Usually this good design practice to assume that major complexities and the tasks requiring the high power are built in the base station due to the obvious reason of scares energy recourses in mobile robot and its soul dependence on rechargeable battery.

Power Supply	3.3V ±5%
Transmitter Frequency	403 MHz (ISM Band)
Out Put Power	24 dBm (251mW in 50 Ohm Load)
Range (Outdoors)	>2 Km
Modulation Frequency	100Hz – 5 KHz (Audio)
Modulation Index	For good PA efficiency select after simulation
Modulation Type Data	FSK (Data),
Modulation Type Voice	AM with Small Modulation Index
Data Rate	100Kbps
Frequency Deviation	Narrow Band FM
Spurious Emissions	Better than -30 dBc (with ref to carrier)
Total System Efficiency	Better than 65%
Power Amp Efficiency	> 70%
Power Amp Type	Class –D or E

This complete design for Low power transmitter is divided in to three projects, which together will form a power efficient radio transmitter. One project will design a BFSK (Binary Frequency Shift Keying) modulator (this project) in form of an all digital PLL (phase lock loop), which will generate a BFSK modulated carrier signal. A second project will design a class D or class E power amplifier which will transmit the BFSK modulated signal over the antenna. A third project will generate the supply voltage to the power amplifier and modulate the supply voltage with a signal from a microphone. The three designs will together form a radio transmitter which simultaneously transmits a BFSK modulated bit stream an amplitude modulated speech signal.

1.1 Project goal

The project goal is to design an integrated circuit (IC) in complementary metal-oxide semiconductor (CMOS) technology. Students, participating in this project as project members and project leaders, should learn the different steps of the IC design flow. That includes the given system architecture analysis, simulation, layout implementation and verification. The project students have an optional choice to manufacture the designed IC circuit on a chip. To test the manufactured chips, another course (TSEK10) is available after the project.

1.2 Milestones and deadline

1: Project selection	Week 3
2: Pre-study, project planning, and discussion with supervisor	Week 4
3: High-level modeling design and simulation result (report)	February 10
4: Gate/transistor level design and simulations result (report)	March 10

5: Layout, DRC, parasitic extraction, LVS, post-layout simulations, modification, chip evaluations, and delivery of the completed chip	May 12
6: **DEADLINE**, Final report, and oral presentation	**May 26**

1.3 Parties

The following parties are involved in this project:

1- Customer: Rashad.M.Ramzan
2- Project supervisor: Rashad.M.Ramzan

Tasks:

- Formulates the project requirements
- Provides technical support
- Reviews the project documents.

3- Project leader: One of the members in the design team.

Tasks:

- Responsible for organization of the team and the project planning.
- Divides the design and documentation work in an efficient way
- Organizes the team meetings as well as the meetings between the team and supervisor
- Keeps the supervisor informed about the progress of the project (at least one email or meeting per week)

4- Project design members (including the project leader)

- Are equally responsible for project planning and design.
- Participate actively in all the meetings
- Support the team and the project leader
- Keep the team and project leader informed about the progress of their tasks.

2 Project description

2.1 System description

The complete system to be built should include the on-chip audio amplifier, Low Pass Filter (LPF), FSK modulator (ALL Digital PLL or Analog VCO as back up option) and power amplifier. The off-chip components include microphone coupling circuit, VCO inductor (if

needed) and matching circuit for antenna. The total system block level diagram is shown in

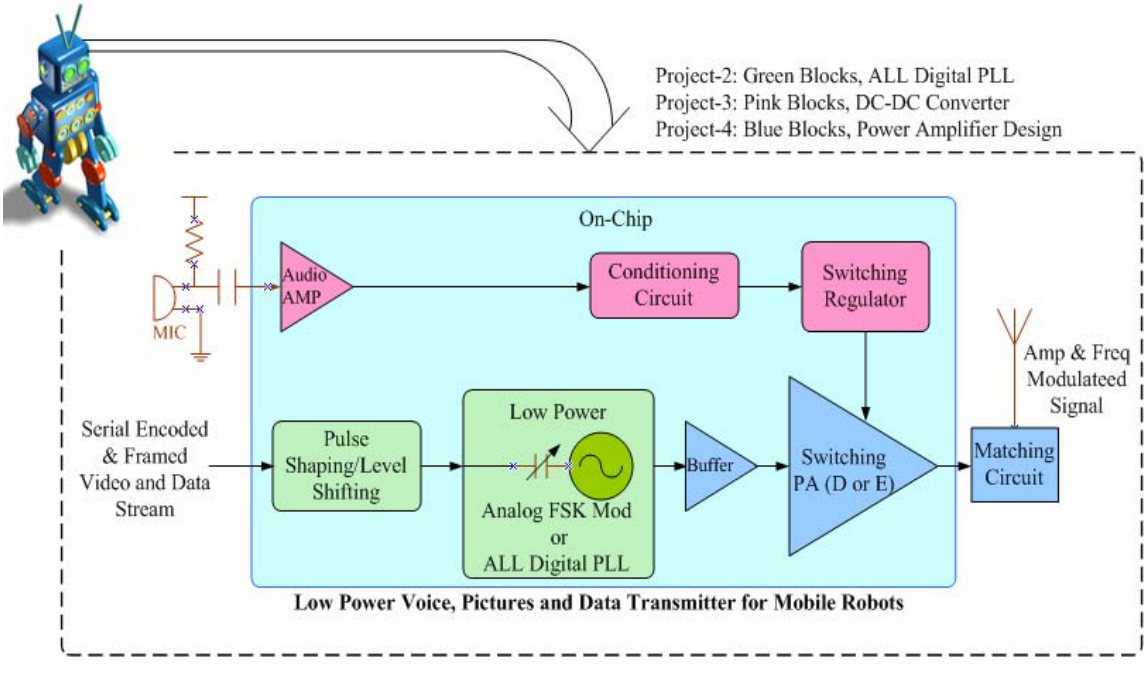

Figure 1. The MIC is ELECTRET Microphone with SNR better than 50dB available in the MEAD LAB, you can download the data sheet from ELFA web pages.

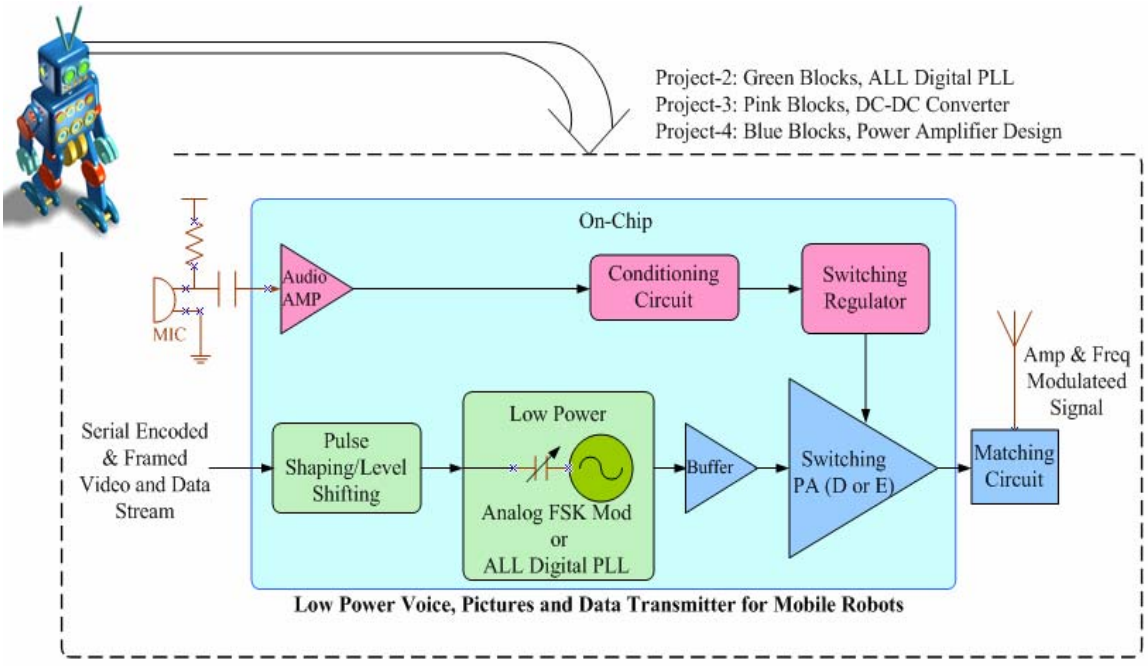

Figure 1: System Block diagram of Complete ISM band Radio Transmitter

2.2 Important design metrics

In this project you have to design the Buffer and Switching PA (Blue Blocks) as shown in Figure.1. The class D, E and F power amplifier is good candidate for this application. The matching circuit can be inductor-capacitor circuit depending upon the topology of the power amplifier used. Standard L and C components are avail in the MEAD LAB, you should note down those components values available before you design the matching circuit. Especially one should be very careful with the parasitic capacitances (can be calculated from self resonance frequency) and Q values of Inductors used for matching and filtering purposes.

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Power Amp Efficiency	> 70%

3 Area, performance requirements

The table below summarizes the adder performance requirements. Each requirement has its number, formulated text, and the given degree of priority. Three degrees of priority are used: high, medium, and low. High is a firm requirement with no possibility of relaxation, while medium requirements can be relaxed somewhat after good motivation.

Requirement	Requirement text	Priority
1	Power supply voltage 3.3 V ± 5%	High
2	All components integrated on-chip	Low
3	Schematic and layout must be verified by simulation	High
4	Frequency of operation 403MHz	High
5	Efficiency = 70% or better	Medium
6	Spurs better than 30 dB w.r.t carrier	Low
7	Output Power = 24dbm, 51mW in 50 Ohm load	High
8	Chip design area ≤ ~ 1.2 mm^2 (see Figure 2)	High
9	Chip core area < 700µm x 800µm = 0.56mm^2 (see Figure 2)	High
10	Total project pin count < 17 (max 14 active + 3 power supply)	High
11	Design technology is AMS 4-Metal 0.35 µm CMOS	High
12	The most important system nodes should have off-chip access pins	Medium
13	On-chip current densities < 1 mA/µm	High

- All requirements in the table should be fulfilled in "typical", "slow", and "fast" process corners and temperature between 25 and 110 ^oC

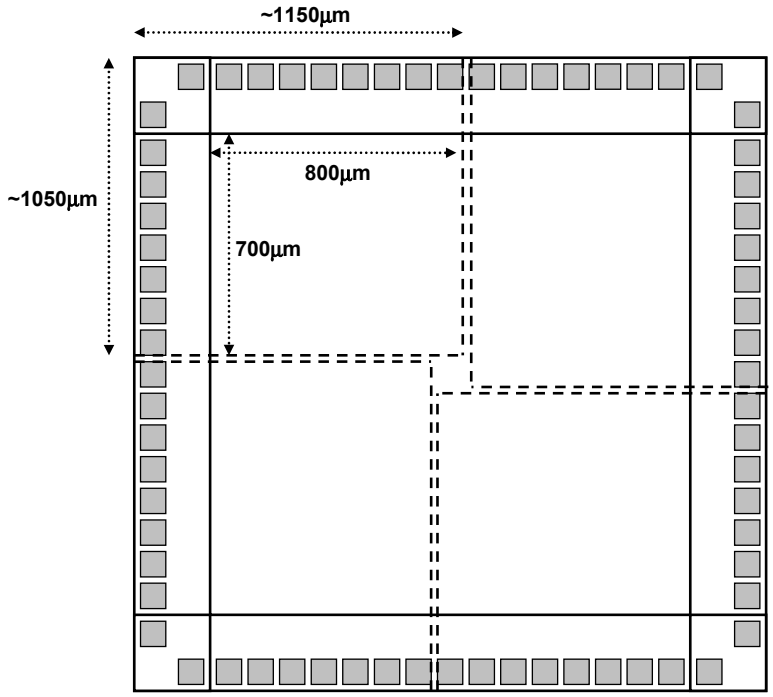

Figure 2: A 5mm^2 chip will be shared by 4 independent projects (4 teams). Each project will utilize a 700x800µm^2 area for core layout and 17 pads.

3.1 Available resources

- Scientific publication database (available from LiU):

♦ IEL – IEEE/IEE Electronic Library, http://www.bibl.liu.se/english/databas/

3.2 Tools

♦ Circuit simulation and layout tools from Cadence®, http://www.cadence.com/

4 References

T.H.Lee, The Design of CMOS Radio-Frequency Integrated Circuits, Cambridge Univ.Press, 2004 (Power Amplifier Chapter)

Behzad Razavi, "RF Microelectronics", Prentice Hall PTR, ISBN 0-13-887571-5, 1998 (Power Amplifier Chapter)

It is highly recommended that students taking this project also take the course TSEK-26.

For more literature references consult with your supervisor.