VLSI Chip Design Project TSEK01

Project description and requirement specification

Version 1.0

Project: Modulating, step-down DC-DC converter

Project number: 3

Project Group:

Name	Project members	Telephone	E-mail
	Project leader and designer 1(5)		
	Designer 2(5)		
	Designer 3(5)		
	Designer 4(5)		
	Designer 5(5)		

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1 Background

This document describes the design requirement specification of a DC-DC converter with amplitude modulating functionality. DC-DC converters are very frequently used in all kinds of system on chip systems to generate different supply-voltages with high power efficiency.

In this course we have three projects which together will form a power efficient radio transmitter. One project will design a BFSK (Binary Frequency Shift Keying) modulator in form of an all digital PLL (phase-lock loop), which will generate a BFSK modulated carrier signal. A second project will design a class D or class E power amplifier, which will transmit the BFSK modulated signal over the antenna. A third project (this project) will generate the supply voltage to the power amplifier and modulate the supply voltage with a signal from a microphone. The three designs will together form a radio transmitter which simultaneously transmits a BFSK modulated bit stream and an amplitude modulated speech signal.

We aim to design a radio transmitter with high power efficient. Therefore this project will use the high power efficiency of a DC-DC converter to design a power efficient amplitude modulator.

1.1 Project goal

The project goal is to design an integrated circuit (IC) in complementary metal-oxide semiconductor (CMOS) technology. Students, participating in this project as project members and project leaders, should learn the different steps of the IC design flow. That includes system architecture analysis, simulation, layout implementation and verification. The project students have an optional choice to manufacture the designed IC circuit on a chip. To test the manufactured chips, another course (TSEK10) is available after the project.

1.2 Milestones and deadline

1: Project selection	Week 3
2: Pre-study, project planning, and discussion with supervisor	Week 4
3: High-level modeling design and simulation result (report)	February 10
4: Gate/transistor level design and simulations result (report)	March 10
5: Layout, DRC, parasitic extraction, LVS, post-layout simulations, modification, chip evaluations, and delivery of the completed chip	May 12
6: **DEADLINE**, Final report, and oral presentation	**May 26**

1.3 Parties

The following parties are involved in this project:

1- Customer: Henrik Fredriksson
2- Project supervisor: Henrik Fredriksson

Tasks:

- Formulates the project requirements

- Provides technical support
- Reviews the project documents.

3- Project leader: One of the members in the design team.

Tasks:

- Responsible for organization of the team and the project planning.
- Divides the design and documentation work in an efficient way
- Organizes the team meetings as well as the meetings between the team and supervisor
- Keeps the supervisor informed about the progress of the project (at least one email or meeting per week)

4- Project design members (including the project leader)

- Are equally responsible for project planning and design.
- Participate actively in all the meetings
- Support the team and the project leader
- Keep the team and project leader informed about the progress of their tasks.

2 Project description

2.1 System description

A step down DC-DC converter (Buck converter) consists of two switches that switch one terminal of an inductor (L) between a supply voltage (V_{SUP}) and ground. The other terminal is connected to the output node (V_{OUT}). The output voltage can be changed by changing the duty cycle or frequency of the switching. This is controlled by a control loop in a regulator, locking at the difference between the output voltage (V_{OUT}) and a reference voltage (V_{REF}). If the current through the load (R_L) changes, the output voltage will change, causing an error signal in the control loop. This will cause the control loop to force the output voltage back. In short the regulator will force the output voltage to be the same as the reference voltage. In this project we will use a speech signal as the reference voltage and hereby let the speech signal modulate the output voltage. The parts that should be designed in this project are the microphone amplifier and the DC-DC regulator, including switches.

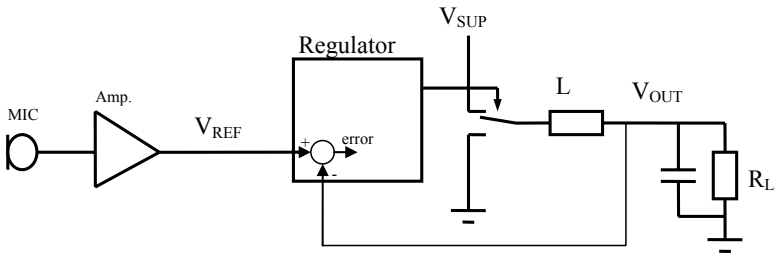

Figure 1: Block diagram of project parts

3 Area, performance requirements

The table below summarizes the adder performance requirements. Each requirement has its number, formulated text, and the given degree of priority. Three degrees of priority are used: high, medium, and low. High is a firm requirement with no possibility of relaxation, while medium requirements can be relaxed somewhat after good motivation.

Requirement	Requirement text	Priority
1	Power supply voltage 3.3V ±5%	High
2	Modulated output voltage range 1.5 V – 3.0 V	High
3	Load impedance 25 Ω -70 Ω	High
4	Power efficiency > 80%	Medium
5	Modulation frequency range 100 Hz – 5 KHz	High
6	Spurious levels at the output < -30 dBc	Medium
7	Microphone signal level >= 10 mV	Medium
8	Microphone impedance 2 kΩ	High
9	Schematic and layout must be verified by simulation	High
10	Chip design area ≤ ~ 1.2 mm^2 (see Figure 2)	High
11	Chip core area < 700μm x 800μm = 0.56mm^2 (see Figure 2)	High
12	Total project pin count < 17 (max 14 active + 3 power supply)	High
13	Design technology is AMS 4-Metal 0.35 μm CMOS	High
14	The most important system nodes should have off-chip access pins	Medium
15	On-chip current densities < 1 mA/μm	High
16	All requirements in the table should be fulfilled in “typical”, “slow”, and “fast” process corners and temperature between 25 and 110 ^oC	High

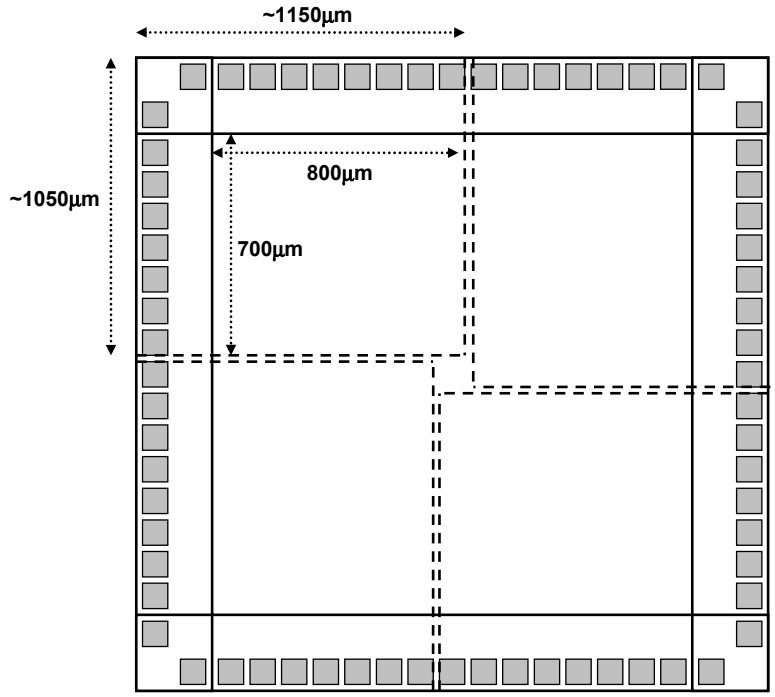

Figure 2: A 5mm^2 chip will be shared by 4 independent projects (4 teams). Each project will utilize a 700x800µm^2 area for core layout and 17 pads.

3.1 Available resources

- Scientific publication database (available from LiU):

♦ IEL – IEEE/IEE Electronic Library, http://www.bibl.liu.se/english/databas/

3.2 Tools

♦ Circuit simulation and layout tools from Cadence®, http://www.cadence.com/

4 References

J.M. Rabaey, A. Chandrakasan, and B. Nikolic., "Digital Integrated Circuits", 2nd ed., Prentice Hall, 2003, ISBN 0-13-120764-4.

N. Waste and K. Eshraghian, "Principles of CMOS VLSI Design", Addison-Wesley, 1993.

R.J. Baker, H.W. Li and D.E. Boyce, "CMOS Circuit Design, Layout, and Simulation", IEEE Press, 1998.

For more literature references consult with your supervisor.