VLSI Chip Design Project TSEK01

Project description and requirement specification

Version 1.0

Project: Low-Power All-Digital PLL (FSK Modulator)

Project number: 2

Project Group:

Name	Project members	Telephone	E-mail
	Project leader and designer 1(5)		
	Designer 2(5)		
	Designer 3(5)		
	Designer 4(5)		
	Designer 5(5)		

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1 Background

In this course we have three projects, which together will form a power efficient radio transmitter. One project will design a BFSK (Binary Frequency Shift Keying) modulator (this project) in form of an all digital PLL (phase lock loop), which will generate a BFSK modulated carrier signal. A second project will design a class D or class E power amplifier which will transmit the BFSK modulated signal over the antenna. A third project will generate the supply voltage to the power amplifier and modulate the supply voltage with a signal from a microphone. The three designs will together form a radio transmitter which simultaneously transmits a BFSK modulated bit-stream and an amplitude modulated speech signal.

This document describes the design requirement specification of an All-Digital Phased Lock Loop (PLL). A PLL is a circuit that synchronizes an output signal generated by an oscillator, with a reference or input signal in both frequency and phase. The PLL has a control loop that regulates the oscillator frequency so that the phase error is kept low. A PLL can be used as a frequency multiplier, which multiplies the frequency of an input signal with some ratio. The main advantage of the all-digital approach for a PLL compared to the conventionally analog, is that sensitive analog circuitry in mainly filters can be avoided.

1.1 Project goal

The project goal is to design an integrated circuit (IC) in complementary metal-oxide semiconductor (CMOS) technology. Students, participating in this project as project members and project leaders, should learn the different steps of the IC design flow. That includes the given system architecture analysis, simulation, layout implementation and verification. The project students have an optional choice to manufacture the designed IC circuit on a chip. To test the manufactured chips, another course (TSEK10) is available after the project.

1.2 Milestones and deadline

1: Project selection	Week 3
2: Pre-study, project planning, and discussion with supervisor	Week 4
3: High-level modeling design and simulation result (report)	February 10
4: Gate/transistor level design and simulations result (report)	March 10
5: Layout, DRC, parasitic extraction, LVS, post-layout simulations, modification, chip evaluations, and delivery of the completed chip	May 12
6: **DEADLINE**, Final report, and oral presentation	**May 26**

1.3 Parties

The following parties are involved in this project:

1- Customer: Martin Hansson
2- Project supervisor: Martin Hansson

Tasks:

- Formulates the project requirements
- Provides technical support
- Reviews the project documents.

3- Project leader: One of the members in the design team.

Tasks:

- Responsible for organization of the team and the project planning.
- Divides the design and documentation work in an efficient way
- Organizes the team meetings as well as the meetings between the team and supervisor
- Keeps the supervisor informed about the progress of the project (at least one email or meeting per week)

4- Project design members (including the project leader)

- Are equally responsible for project planning and design.
- Participate actively in all the meetings
- Support the team and the project leader
- Keep the team and project leader informed about the progress of their tasks.

2 Project description

2.1 System description

A block schematic of an All-Digital PLL (ADPLL) is shown in Figure 1. The ADPLL will receive a reference clock from an external source (crystal or other). A phase-detector (PD) will compare the phase of the reference with the pre-scaled version of the RF clock (ClkRF). The outputs of the phase detector are up/down signals. The up/down signals controls an up/down-counter that outputs a binary word that gives the phase-error. This control word is decoded in a decoder that outputs switch control signals to the Digital Controlled Oscillator (DCO). Based on the control signals to the DCO the frequency of the signal ClkRF is changed. A pre-scaler divides the frequency down to the same as the reference, and are feed back to the PD. To implement the FSK modulation a select signal (Select) controls which of two different paths that is active.

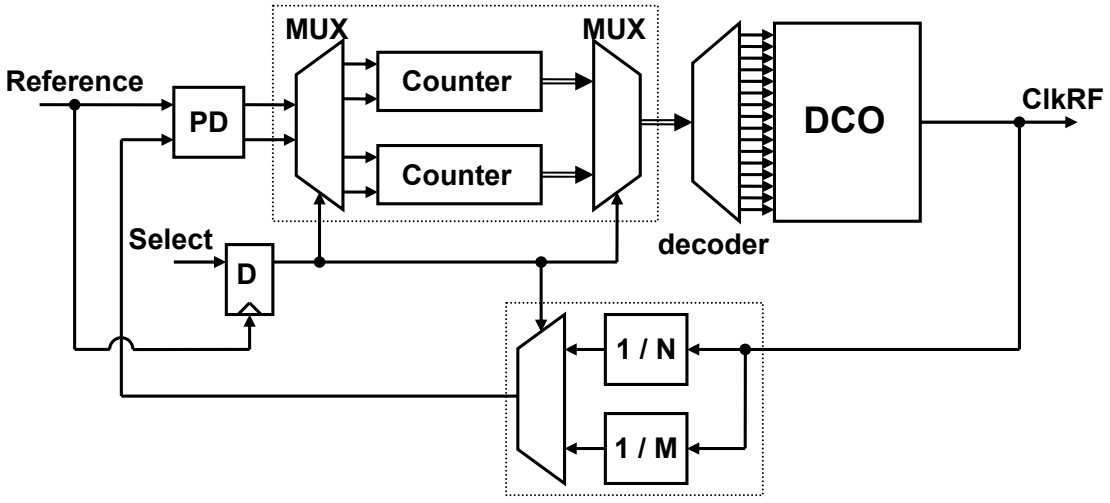

Figure 1: Block diagram of ADPLL

2.2 Important design metrics

The DCO is a critical component in the PLL and must be designed so that the correct frequency range can be assured. Moreover, design decisions about integrated or off-chip inductors for the oscillator need to be considered. The bit-range of the counters needs to be enough to assure enough dynamic range of the PLL. Further, the pre-scalers (frequency dividers) require extensive timing and performance analysis to reach required performance. Low-power is of utmost importance in this project, so all components in the PLL will be designed for lowest possible power.

3 Area, performance requirements

The table below summarizes the adder performance requirements. Each requirement has its number, formulated text, and the given degree of priority. Three degrees of priority are used: high, medium, and low. High is a firm requirement with no possibility of relaxation, while medium requirements can be relaxed somewhat after good motivation.

Requirement	Requirement text	Priority
1	Power supply voltage 3.3 V ± 5%	High
2	All components integrated on-chip	High
3	Schematic and layout must be verified by simulation	High
4	Center frequency 403 MHz	High
5	Modulation input 100 kbit/s	High
6	Modulation frequency max 1 MHz	High
7	Simulated PLL power consumption < 10mW	Medium
8	Chip design area ≤ ~ 1.2 mm^2 (see Figure 2)	High
9	Chip core area < 700μm x 800μm = 0.56mm^2 (see Figure 2)	High
10	Total project pin count < 17 (max 14 active + 3 power supply)	High
11	Design technology is AMS 4-Metal 0.35 μm CMOS	High
12	The most important system nodes should have off-chip access pins	Medium
13	On-chip current densities < 1 mA/μm	High

- All requirements in the table should be fulfilled in “typical”, “slow”, and “fast” process corners and temperature between 25 and 110 ^oC

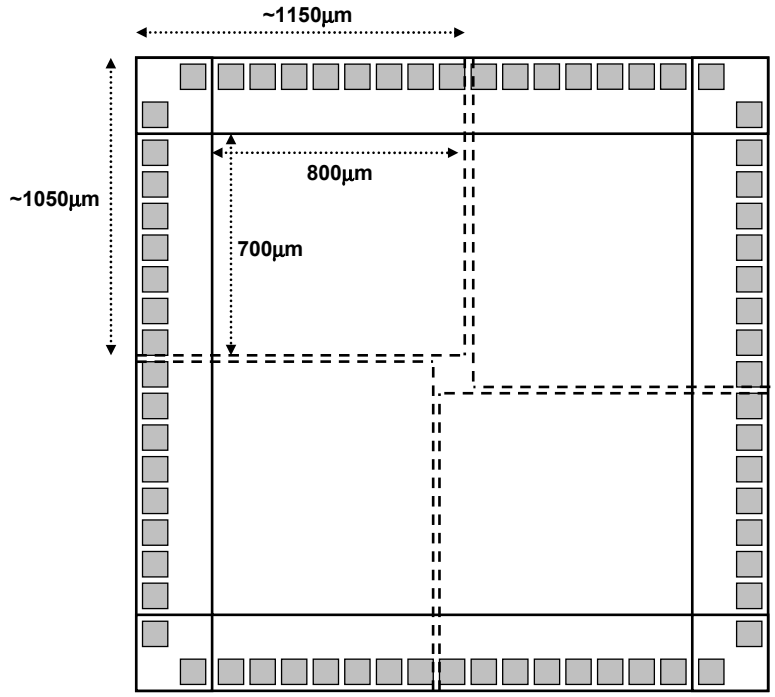

Figure 2: A 5mm^2 chip will be shared by 4 independent projects (4 teams). Each project will utilize a 700x800µm^2 area for core layout and 17 pads.

3.1 Available resources

- Scientific publication database (available from LiU):

♦ IEL – IEEE/IEE Electronic Library, http://www.bibl.liu.se/english/databas/

3.2 Tools

♦ Circuit simulation and layout tools from Cadence®, http://www.cadence.com/

4 References

J.M. Rabaey, A. Chandrakasan, and B. Nikolic., "Digital Integrated Circuits", 2nd ed., Prentice Hall, 2003, ISBN 0-13-120764-4.

N. Waste and K. Eshraghian, "Principles of CMOS VLSI Design", Addison-Wesley, 1993.

R.J. Baker, H.W. Li and D.E. Boyce, "CMOS Circuit Design, Layout, and Simulation", IEEE Press, 1998.

For more literature references consult with your supervisor.