VLSI design project, TSEK01

Project description and requirement specification

Version 1.0

Project: An all digital DLL-based multi-phase clock generator

Project number: 7

Project Group:

Name	Project members	Telephone	E-mail
	Project leader and designer 1(4)		
	Designer 2(4)		
	Designer 3(4)		
	Designer 4(4)		

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1 Background

Execution engines of multi-gigahertz superscalar processors require multiphase clock signals with accurate edge-position to trigger dynamic datapath circuits. A high-speed local multiphase clock generator is therefore essential to maximize processor performance. The intermediate clock-phases need automatic stretch-ability in proportion with the core clock period. For a narrow or discrete frequency-range, programmable delay-lines are efficient phase-generators enabling: (i) instantaneous (zero-time) response to step-like changes in core clock frequency due to any potential clock gating scheme for energy saving, (ii) low power consumption, and (iii) maximum clock integrity with zero-tolerance for clock delivery failure.

However, today's advanced processors are designed to operate within a wide range of supply voltages and clock frequencies supporting different target power-performance operating points and slow frequency test/debug . This necessitates delay-lines with wide delay-range and high time-resolution, which is beyond the capability of programmable delay-lines.

1.1 Project goal

The goal of this project is to design a low power multi-phase clock generator supporting a frequency range of 400MHz to 800MHz in a 0.35mm CMOS technology.

1.2 Milestones and deadline

1- Project selection	Week 3
2- Pre-study, project planning, and discussion with supervisor	Week 4
3- High-level modeling design and simulation result (report)	February 11
4- Gate/transistor level design and simulations result (report)	March 7
5- Layout, DRC, parasitic extraction, LVS, post-layout simulations, modification, chip evaluations, and delivery of the completed chip	May 17
6- **DEADLINE**, Final report, and oral presentation	May 25

1.3 Parties

The following parties are involved in this project:

1- Customer: Course instructor Atila Alvandpour
2- Project supervisor: Atila Alvandpour

Tasks:

- Formulates the project requirements
- Provides technical support
- Reviews the project documents.

3- Project leader: One of the members in the design team.

Tasks:

- Responsible for organization of the team and the project planning.
- Divides the design and documentation work in an efficient way
- Organizes the team meetings as well as the meetings between the team and supervisor
- Keeps the supervisor informed about the progress of the project (at least one email or meeting per week)

4- Project design members (including the project leader)

- Are equally responsible for project planning and design.
- Participate actively in all the meetings
- Support the team and the project leader
- Keep the team and project leader informed about the progress of their task.

2 Project description

Fig.1 shows the organization of the multiphase clock generator. A phase detector compares the reference clock (phase 0^o) with the last output of the delay-line (360^o phase). The binary output of the phase detector forces the 5-bit counter to count up or down, and the output of the counter controls the delay-line (in the closed loop mode).

The loop sampling frequency is 1/8 of the clock frequency to ensure that the loop is updated and settled before the phase-detector continues with the next phase-comparison. The loop continues to operate until the length of the delay-line is aligned with the reference clock period time. Once the loop is locked, the counter's output starts to dither around the correct value by at least +/-1 LSB.

At locked condition, an averaging unit starts to average the counter's output over 128 cycles of the loop-sampling frequency. The averaging unit does not add to the accuracy of the phase-generator in the closed-loop mode; however, it is a necessary component to determine the optimum control code for the open-loop mode. A sufficiently long averaging time can cover the code variations due to the response of the closed-loop to potential low-frequency components of the supply voltage variations.

Following the averaging period, if the closed-loop mode is not requested, the loop opens and the stored 5-bit binary code controls the delay-line. Once the system enters into open loop, the clock generator is effectively a chain of binary-weighted delay elements, hence eliminating dithering activity during lock.

The phase detector, counter and averaging unit are all gated-off and therefore consume only leakage power consumption. A synchronous control unit controls the above closed-to-open loop timing. It is first activated with an external reset signal, "activate". The control unit completes the above close-to-open loop procedure (Fig. 2), which ends if the activation signal is deactivated.

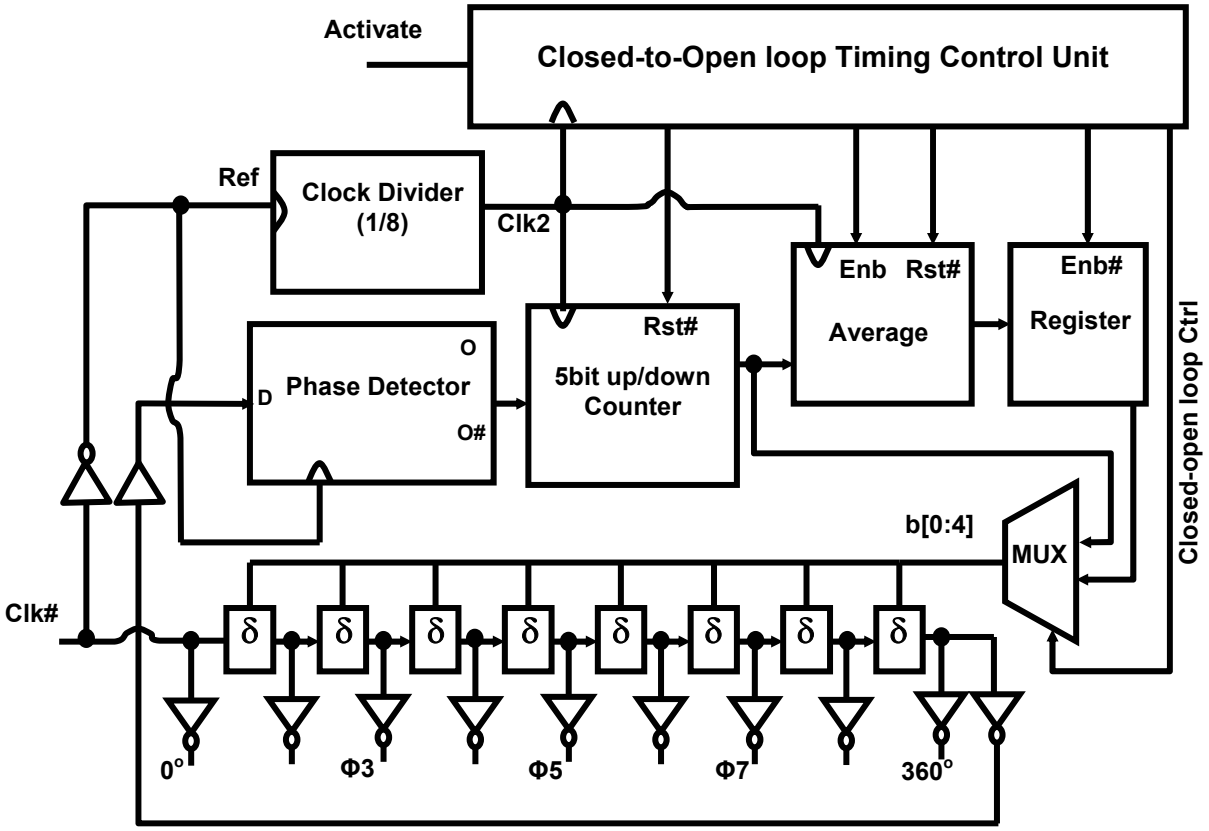

Fig.1: Organization of the multiphase clock generator

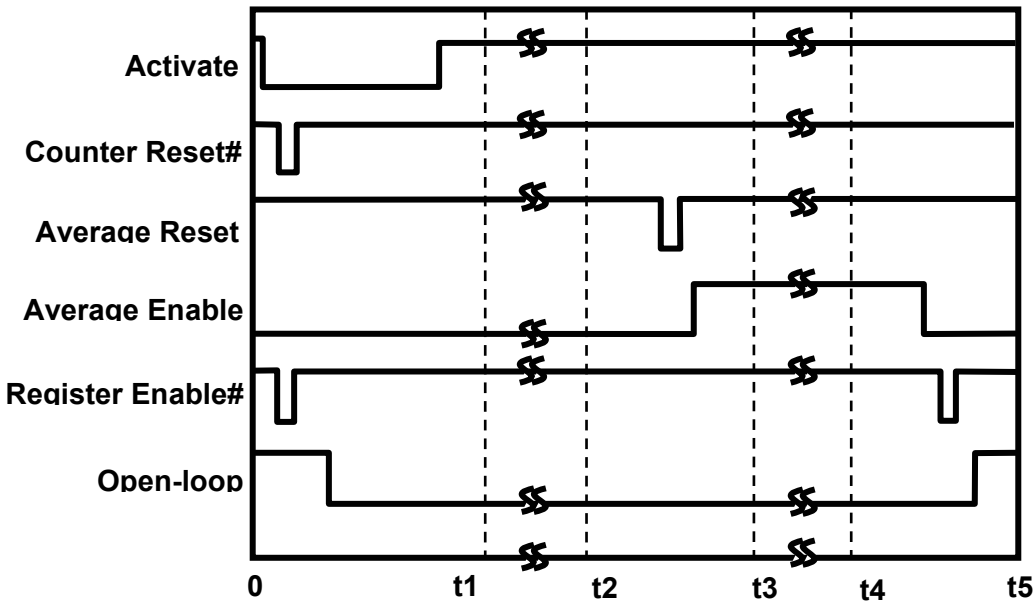

Fig.2: Timing diagram of the closed-to-open loop control unit.

3 Area, performance requirements

Process	**0.35µm, 3.3V, CMOS**
Die area	**< 0.7 X 0.8 mm^2 (see Fig.3)**
Number of PAD's	**< 16**
Total power in closed-loop	**< 100mW**
Total power in open-loop	**< 30mW at 110^{o}C**
Total power in open-loop (clock gated off)	***O*(µW)**
Frequency Range at 3.3V, 110^{o}C	**300- 600MHz (about 2X)**
Lock time after closed-loop activation	**< 256 clock cycles**

- **All requirements in the table should be fulfilled in "typical", "slow", and "fast" process corners and temperature between 25 and 110^{o}C**

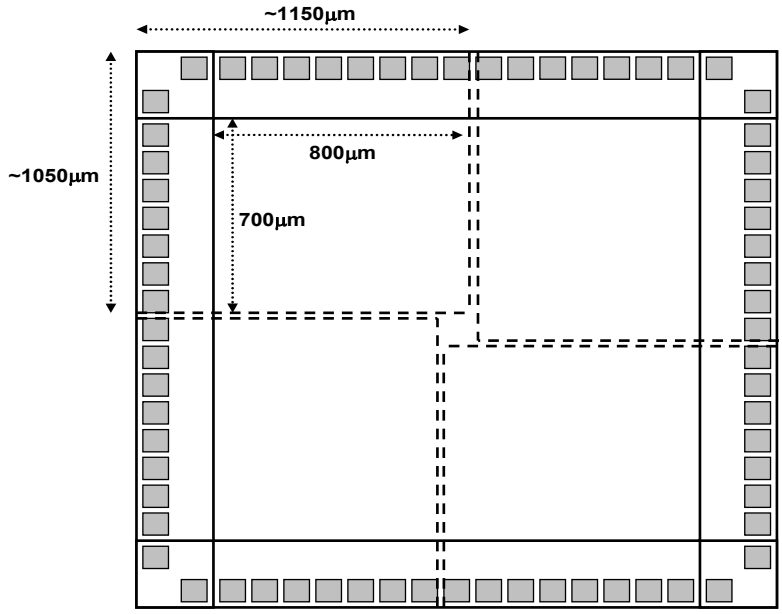

Fig 3: A 5mm^2 chip will be shared by 4 independent projects (4 teams). Each project will utilize a 700x800µm^2 area for core layout and 17 pads.

3.1 Available resources

• Scientific publication database (available from LiU):

♦ IEL – IEEE/IEE Electronic Library, http://www.bibl.liu.se/english/databas/

3.2 Tools

♦ Circuit simulation and layout tools from Cadence®, http://www.cadence.com/

♦ MathWorks® Matlab, http://www.mathworks.com/