# VLSI design project, TSEK01

## Project description and requirement specification

**Version 1.0**

## Project: High-Speed 32-bit Kogge-Stone Adder

## Project number: 3

### Project Group:

| Name | Project members | Telephone | E-mail |
|---|---|---|---|
| | Project leader and designer 1(5) | | |
| | Designer 2(5) | | |
| | Designer 3(5) | | |
| | Designer 4(5) | | |
| | Designer 5(5) | | |

**Customer and supervisor**: Martin Hansson
Office: B-house 3A:515, Phone.: 013-282859, Fax: 013-139282
Email: martinh@isy.liu.se

# 1 Background

This document describes the design requirement specification of a 32-bit Kogge-Stone Adder. The Kogge-Stone adder utilizes a parallel-prefix topology to reduce the critical path in the adder. The critical path, which is the carry generation path, has a logarithmic dependence of the bit-width, which should be compared to the linear dependence in the ripple carry adder. There are many ways to implement the carry generation tree for parallel prefix adders, but Kogge-Stone implementation is the most straightforward, and also it has one of the shortest critical paths of all tree adders. The drawback with the Kogge-Stone implementation is the area and interconnects that is needed.

## *1.1 Project goal*

The project goal is to design an integrated circuit (IC) in complementary metal-oxide semiconductor (CMOS) technology. Students, participating in this project as project members and project leaders, should learn the different steps of the IC design flow. That includes the given system architecture analysis, simulation, layout implementation and verification. The project students have an optional choice to manufacture the designed IC circuit on a chip. To test the manufactured chips, another course (TSEK10) is available after the project.

## *1.2 Milestones and deadline*

| | |
|---|---|
| 1: Project selection | Week 3 |
| 2: Pre-study, project planning, and discussion with supervisor | Week 4 |
| 3: High-level modeling design and simulation result (report) | February 11 |
| 4: Gate/transistor level design and simulations result (report) | March 7 |
| 5: Layout, DRC, parasitic extraction, LVS, post-layout simulations, modification, chip evaluations, and delivery of the completed chip | May 17 |
| 6: **DEADLINE**, Final report, and oral presentation | **May 25** |

## *1.3 Parties*

The following parties are involved in this project:

1- Customer: Martin Hansson
2- Project supervisor: Martin Hansson

Tasks:

- Formulates the project requirements
- Provides technical support
- Reviews the project documents.

3- Project leader: One of the members in the design team.

Tasks:

- Responsible for organization of the team and the project planning.
- Divides the design and documentation work in an efficient way

- Organizes the team meetings as well as the meetings between the team and supervisor
- Keeps the supervisor informed about the progress of the project (at least one email or meeting per week)

4- Project design members (including the project leader)

- Are equally responsible for project planning and design.
- Participate actively in all the meetings
- Support the team and the project leader
- Keep the team and project leader informed about the progress of their tasks.

# 2 Project description

## *2.1 System description*

The complete system to be built should include the adder, an on-chip evaluation circuit, and I/O circuitry. Because of the limited amount of pads a bit serial input/output interface must be used to feed input vectors to the adder. This creates the need for serial-to-parallel and parallel-to-serial converters. The total system block level is shown in Figure 1.

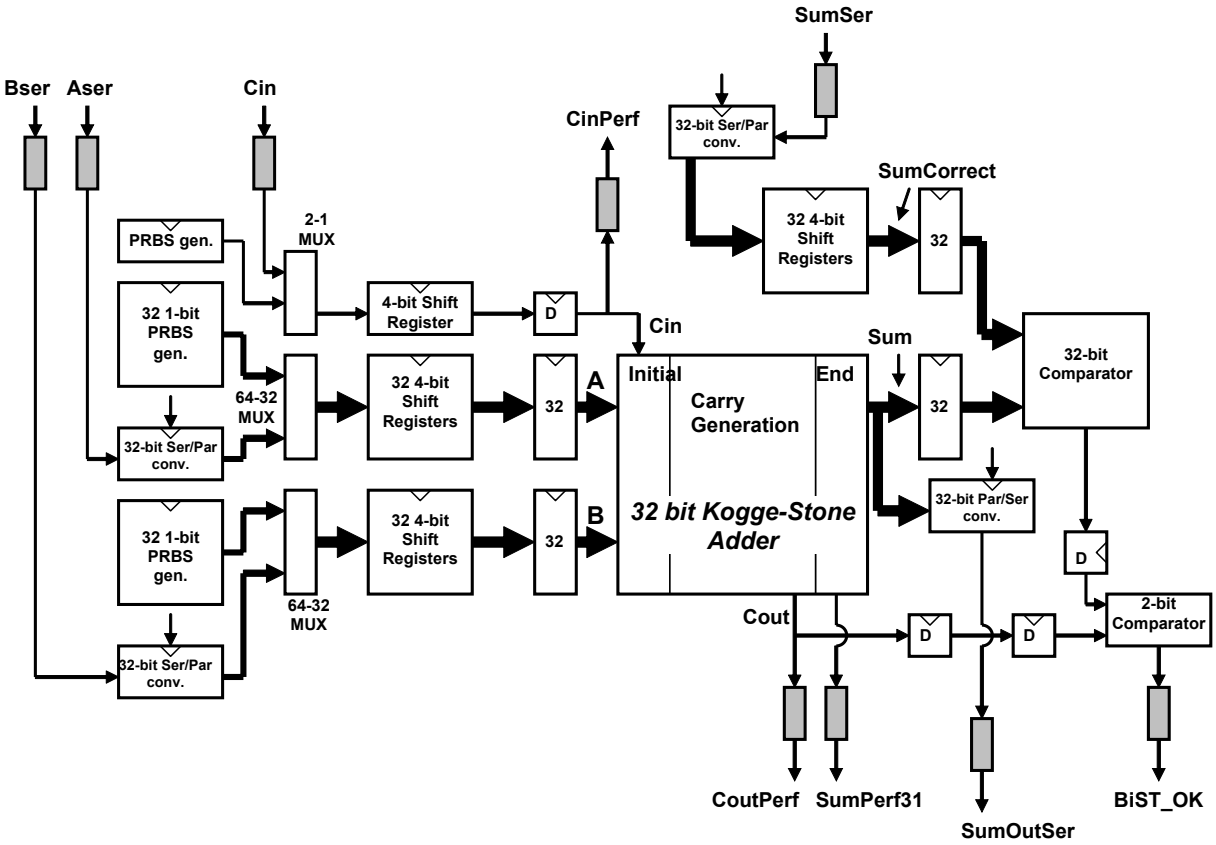


**Figure 1: System Block diagram of Adder and evaluation circuitry.**

The inputs are feed to the circuit in a bit-serial data stream and are converted into 32-bit vectors by the serial to parallel converters. 4 different test vectors for input A, B, and Cin respectively, is feed into the shift registers on-chip. The correct sum vectors are feed into the sum-shift registers. With the four test vectors a full speed on-chip evaluation is possible through the comparator circuitry, which outputs a signal that indicate if the counter evaluated the input data correct or not. Power measurements of the adder are done using PRBS data at the input of the adder. Outputs of the sum vector are possible through a parallel-to-serial

interface. The MSB and the carry output are also feed out of the chip for performance measurements.

### *2.2 Important design metrics*

The adder should be design for a high-performance application, meaning that proper measures must be taken to maximize the performance. However the power consumption should be held at a reasonable level. A dynamic domino implementation of the carry generation stage is a suitable way to go. However, the dynamic domino implementation requires a thorough timing investigation, in order to assure the robustness of the circuit. During the project discussions on suitable design solutions are expected.

# 3 Area, performance requirements

The table below summarizes the adder performance requirements. Each requirement has its number, formulated text, and the given degree of priority. Three degrees of priority are used: high, medium, and low. High is a firm requirement with no possibility of relaxation, while medium requirements can be relaxed somewhat after good motivation.

| **Requirement** | **Requirement text** | **Priority** |
|---|---|---|
| **1** | Operation frequency 400 - 800 MHz | High |
| **2** | Integrate as many system components as possible on-chip | High |
| **3** | Schematic and layout must be verified by simulation | High |
| **4** | On-chip evaluation should be implemented, for full speed testing | High |
| **5** | Simulated chip power consumption < 500mW at max. freq. | Medium |
| **6** | Simulated adder power (normal activity) < 100mW at max. freq. | High |
| **7** | Chip design area ~ 1.2 $mm^2$ (see Figure 2) | Medium |
| **8** | Chip core area < 700μm x 800μm = 0.56$mm^2$ (see Figure 2) | High |
| **9** | Total project pin count < 17 (max 15 active + 2 power supply) | High |
| **10** | Design technology is AMS 4-Metal 0.35 μm CMOS | High |
| **11** | The most important system nodes should have off-chip access pins | Medium |
| **12** | On-chip current densities < 1 mA/μm | High |

- All requirements in the table should be fulfilled in “typical”, “slow”, and “fast” process corners and temperature between 25 and 110 $^oC$

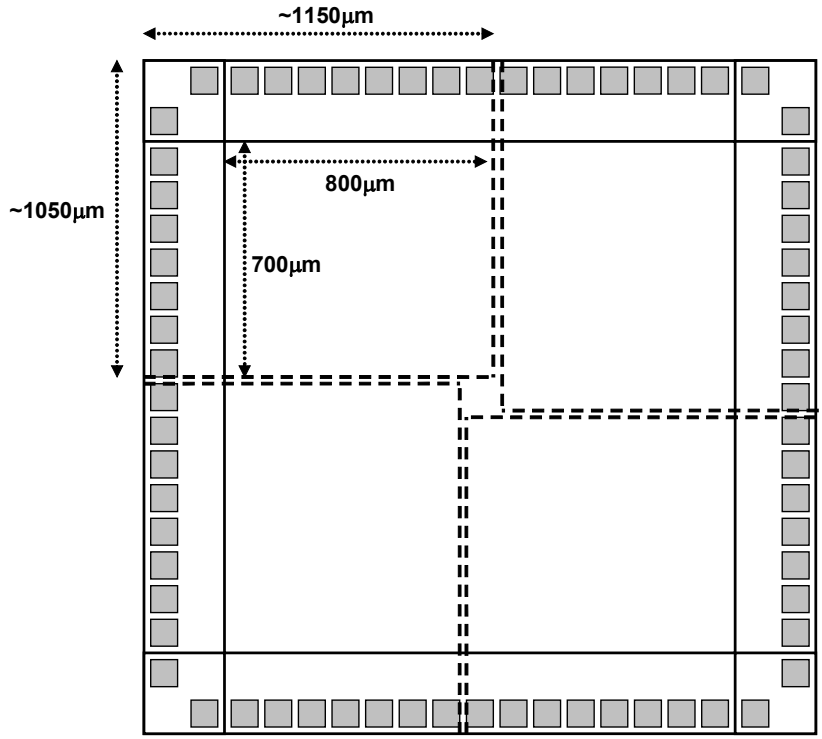


**Figure 2: A 5mm$^2$ chip will be shared by 4 independent projects (4 teams). Each project will utilize a 700x800µm$^2$ area for core layout and 17 pads.**

### *3.1 Available resources*

- Scientific publication database (available from LiU):

♦ IEL – IEEE/IEE Electronic Library, http://www.bibl.liu.se/english/databas/

### *3.2 Tools*

♦ Circuit simulation and layout tools from Cadence®, http://www.cadence.com/

# 4 References

J.M. Rabaey, A. Chandrakasan, and B. Nikolic., "Digital Integrated Circuits", 2nd ed., Prentice Hall, 2003, ISBN 0-13-120764-4.

N. Waste and K. Eshraghian, "Principles of CMOS VLSI Design", Addison-Wesley, 1993.

R.J. Baker, H.W. Li and D.E. Boyce, "CMOS Circuit Design, Layout, and Simulation", IEEE Press, 1998.

S.-M. Kang and Y. Leblebici, "CMOS Digital Integrated Circuits: Analysis and Design", McGraw-Hill, 1999

For more literature references consult with your supervisor.