VLSI design project, TSEK01

Project description and requirement specification

Version 1.0

Project: A Digital Decimation Filter for Oversampled Sigma-Delta Modulators

Project number: 6

Project Group:

Name	Project members	Telephone	E-mail
	Project leader and designer 1(4)		
	Designer 2(4)		
	Designer 3(4)		
	Designer 4(4)		

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1 Background

This document describes the design requirement specification of a digital decimation filter for an oversampled sigma-delta modulator. Many microelectronic systems require an ADC. Instead of using an ADC with a large number of bits, which is tough to design because of matching requirements, an oversampled low resolution ADC together with noise-shaping can be employed. A Sigma-Delta ADC is an example of an oversampled converter commonly used today when the bandwidth of the input signal is less than 1MHz. The output from an oversampled Sigma-Delta ADC contains high frequency noise, which needs to be removed by a digital lowpass filter. A common approach is to in the digital filter also include the necessary decimation down to the target bit rate.

1.1 Project goal

The project goal is to design an integrated circuit (IC) in complementary metal-oxide semiconductor (CMOS) technology. Students, participating in this project as project members and project leaders, should learn the different steps of the IC design flow. That includes the given system architecture analysis, simulation, layout implementation and verification. The project students have an optional choice to manufacture the designed IC circuit on a chip. To test the manufactured chips, another course (TSEK10) is available after the project.

1.2 Milestones and deadline

1: Project selection	Week 3
2: Pre-study, project planning, and discussion with supervisor	Week 4
3: High-level modeling design and simulation result (report)	February 11
4: Gate/transistor level design and simulations result (report)	March 7
5: Layout, DRC, parasitic extraction, LVS, post-layout simulations, modification, chip evaluations, and delivery of the completed chip	May 17
6: **DEADLINE**, Final report, and oral presentation	**May 25**

1.3 Parties

The following parties are involved in this project:

1- Customer: Peter Caputa
2- Project supervisor: Peter Caputa

Tasks:

- Formulates the project requirements
- Provides technical support
- Reviews the project documents.

3- Project leader: One of the members in the design team.

Tasks:

- Responsible for organization of the team and the project planning.
- Divides the design and documentation work in an efficient way
- Organizes the team meetings as well as the meetings between the team and supervisor
- Keeps the supervisor informed about the progress of the project (at least one email or meeting per week)

4- Project design members (including the project leader)

Tasks:

- Are equally responsible for project planning and design.
- Participate actively in all the meetings
- Support the team and the project leader
- Keep the team and project leader informed about the progress of their tasks.

2 Project description

2.1 System description

The microelectronic system you design should be a fully functional digital lowpass decimation filter intended to filter the output signal from a sigma-delta modulator. Hopefully, another group will successfully design a sigma-delta modulator and thus provide you with an appropriate 3-bit input signal. As backup, your design should be able to accept an external 3-bit input signal as well. The target for this design will be to meet the Bluetooth standard. This requires 80dB dynamic range (simply SNR=Signal-to-noise ratio) over a 500kHz bandwidth A 32x oversampled second-order sigma-delta modulator can be designed to meet these requirements.

The digital filter block diagram is shown in Figure1 and consists of two sub-filters. The first filter is a CIC-filter (Cascaded Integrator Comb filter), which takes an input data rate of 32Msps, perfoms a lowpass filtering of it and decimates the data stream by a factor of D1 (e.g D1=16). The CIC-filter consists of an integrator section followed by decimation and finally a comb section. The number of integrator and comb sections in the CIC-filter are the same. The second filter is a standard FIR filter. Just before the filter bank output, we perform a second decimation by a factor of D2 (e.g. D2=2), so that the total decimation D1*D2=32 (e.g. D1*D2=16*2=32).

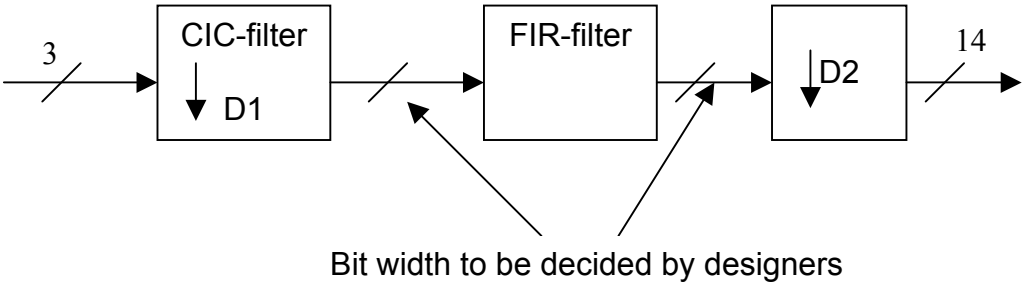

Figure 1: Digital low pass filter block diagram.

The total filter transfer function must have a 3dB bandwidth of 500kHz with a passband ripple smaller than 2dB and stop band attenuation better than 50dB. Figure 2 shows an example of the filter transfer function characteristics.

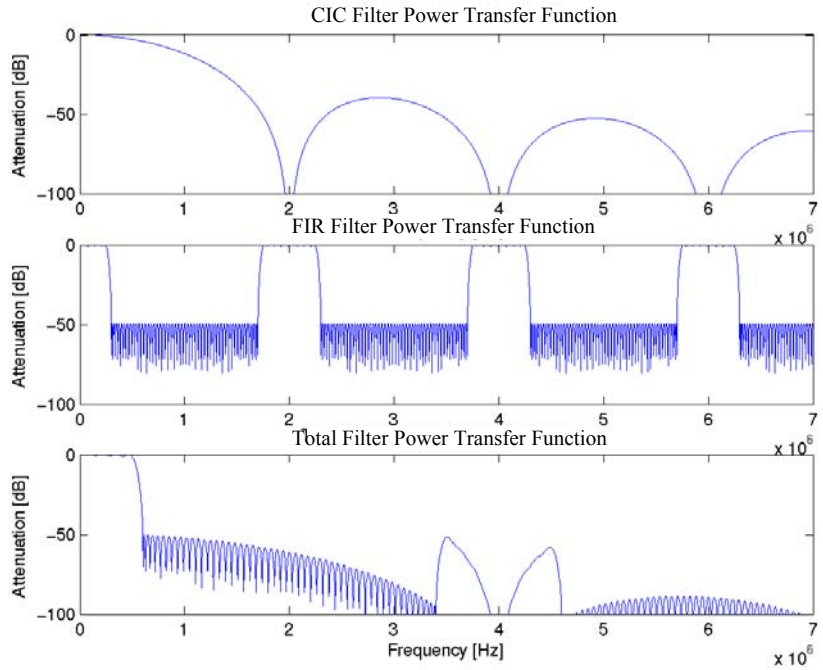

Figure 2: Example of filter transfer function characteristics.

2.2 Important design metrics

The implemented circuit should take an input data stream of 32Msps and decimate it by a factor of 32. This will be translated to requirements on the integrators, adders, and filter coefficient multiplication. Important things to consider are:

- Area
- Internal word length
- Filter Transfer Function Properties

Furthermore, as Bluetooth usually is a battery driven application the power-consumption is of large interest and should be minimized.

3 Area, performance requirements

Table1 below summarizes the circuit performance requirements. Each requirement has its number, formulated text, and the given degree of priority. Three degrees of priority are used: high, medium, and low. High is a firm requirement with no possibility of relaxation, while medium requirements can be relaxed somewhat after good motivation.

Requirement	Requirement text	Priority
1	Accept an input data rate of 32Msps and decimate it by a factor of 32 (i.e. the output data rate must be 1Msps)	High
2	Total 3dB bandwidth 500kHz	High
3	Passband ripple < 2dB	High
4	Total stop band attenuation >50dB	High
5	Integrate as many system components as possible on-chip	High
6	Schematic and layout must be verified by simulation	High
7	Simulated chip power consumption < 25mW at max. freq.	Medium
8	Cooperation with the group designing the sigma-delta modulator	Low
9	Chip design area ~ 1.2 mm^2 (see Figure3)	Medium
10	Chip core area < 700μm x 800μm = 0.56mm^2 (see Figure3)	High
11	Total project pin count < 17 (max 15 active + 2 power supply)	High
12	Design technology is AMS 4-Metal 0.35 μm CMOS	High
13	The most important system nodes should have off-chip access pins	Medium
14	On-chip current densities < 1 mA/μm	High

Table 1. Circuit performance requirements

- All requirements in the table should be fulfilled in "typical", "slow", and "fast" process corners and temperature between 25 and 110 ^oC

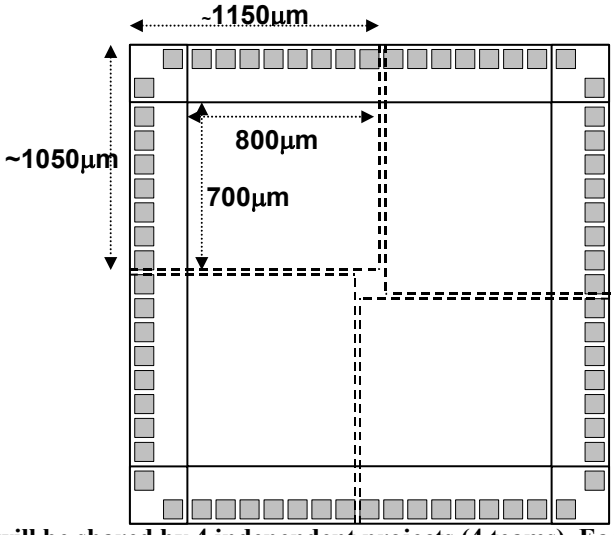

Figure 3: A 5mm^2 chip will be shared by 4 independent projects (4 teams). Each project will utilize a 700x800μm^2 area for core layout and 17 pads.

3.1 Available resources

- Scientific publication database (available from LiU):

♦ IEL – IEEE/IEE Electronic Library, http://www.bibl.liu.se/english/databas/

3.2 Tools

♦ Circuit simulation and layout tools from Cadence®, http://www.cadence.com/

4 References

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