VLSI design project, TSEK01

Project description and requirement specification

Version 1.0

Project: High-Speed 8-bit Pipeline Current-Steering D/A Converter

Project number: 4

Project Group:

Name	Project members	Telephone	E-mail
	Project leader and designer 1(4)		
	Designer 2(4)		
	Designer 3(4)		
	Designer 4(4)		

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1 Background

This document describes the design requirement specification of high-speed 8-bit pipeline current-steering D/A converter. There are different ways to implement current-steering D/A converters. Three common architectures of these kind of D/A converters are: the binary weighted architecture, the unary decoded architecture and segmented architecture (In order to study about these architectures refer to the first reference). The last architecture is proposed in this project. The concept of this architecture is to use a current-matrix for four MSB bits and weighted current sources for four LSB bits, which need less precision.

1.1 Project goal

The project goal is to design an integrated circuit (IC) in complementary metal-oxide semiconductor (CMOS) technology. Students, participating in this project as project members and project leaders, should learn the different steps of the IC design flow. That includes the given system architecture analysis, simulation, layout implementation and verification. The project students have an optional choice to manufacture the designed IC circuit on a chip. To test the manufactured chips, another course (TSEK10) is available after the project.

1.2 Milestones and deadline

1: Project selection	Week 3
2: Pre-study, project planning, and discussion with supervisor	Week 4
3: High-level modeling design and simulation result (report)	February 11
4: Gate/transistor level design and simulations result (report)	March 7
5: Layout, DRC, parasitic extraction, LVS, post-layout simulations, modification, chip evaluations, and delivery of the completed chip	May 17
6: **DEADLINE**, Final report, and oral presentation	**May 25**

1.3 Parties

The following parties are involved in this project:

1- Customer: Behzad Mesgarzadeh
2- Project supervisor: Behzad Mesgarzadeh

Tasks:

- Formulates the project requirements
- Provides technical support
- Reviews the project documents.

3- Project leader: One of the members in the design team.

Tasks:

- Responsible for organization of the team and the project planning.
- Divides the design and documentation work in an efficient way
- Organizes the team meetings as well as the meetings between the team and supervisor

- Keeps the supervisor informed about the progress of the project (at least one email or meeting per week)

4- Project design members (including the project leader)

- Are equally responsible for project planning and design.
- Participate actively in all the meetings
- Support the team and the project leader
- Keep the team and project leader informed about the progress of their tasks.

2 Project description

2.1 System description

The complete system consists of digital processing part and analog circuits, which mainly are current sources. As mentioned earlier a segmented architecture is proposed. In such architecture, circuit is divided into two sub-DACs. For this project four MSB bits will be implemented in Unary architecture and four LSB bits should be implemented in binary weighted architecture. It means we will have a 15-cell current matrix plus four weighted current sources, each of which scaled by the factor of 2. In digital process part a dual path structure is used. Pipelining is another technique to increase throughput of circuit. In digital processing part logics will be broken in a proper way to decrease the length of critical path. For LSB bits which there is no need to special digital processing logics, just simple pipeline stages will be designed.

To get more detailed description of projects students can contact with supervisor.

2.2 Important design metrics

The D/A converter should be design for a high-performance application, meaning that proper measures must be taken to maximize the performance. The most important issue is the speed and throughput of the circuit. However the power consumption should be held at a reasonable level. During the project discussions on suitable design solutions are expected.

3 Area, performance requirements

The table below summarizes the DAC performance requirements. Each requirement has its number, formulated text, and the given degree of priority. Three degrees of priority are used: high, medium, and low. High is a firm requirement with no possibility of relaxation, while medium requirements can be relaxed somewhat after good motivation.

Requirement	Requirement text	Priority
1	Operation frequency > 1.5 GHz (Data rate > 1.5 GS/s)	High
2	Integrate as many system components as possible on-chip	High
3	Schematic and layout must be verified by simulation	High
4	On-chip evaluation should be implemented, for full speed testing	High
5	Simulated chip power consumption < 400mW at max. freq.	Medium
6	Differential output swing for 50-Ohm output >3V	High
7	Chip design area ~ 1.2 mm^2 (see Figure 1)	Medium
8	Chip core area < 700μm x 800μm = 0.56mm^2 (see Figure 1)	High
9	Total project pin count < 17 (max 15 active + 2 power supply)	High
10	Design technology is AMS 4-Metal 0.35 μm CMOS	High
11	The most important system nodes should have off-chip access pins	Medium
12	On-chip current densities < 1 mA/μm	High

- All requirements in the table should be fulfilled in “typical”, “slow”, and “fast” process corners and temperature between 25 and 110 ^oC

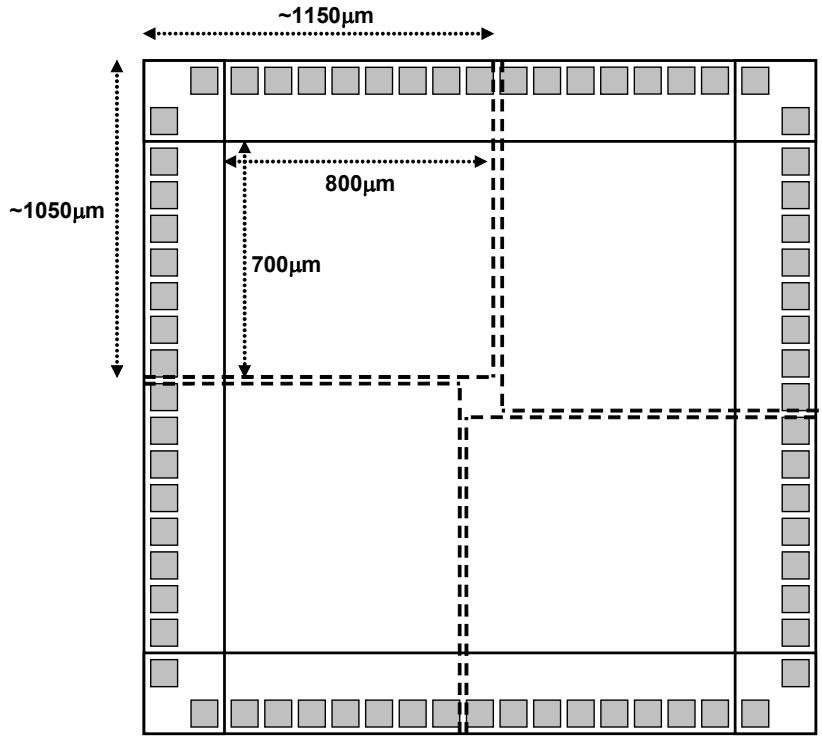

Figure 1: A 5mm^2 chip will be shared by 4 independent projects (4 teams). Each project will utilize a 700x800µm^2 area for core layout and 17 pads.

3.1 Available resources

- Scientific publication database (available from LiU):

♦ IEL – IEEE/IEE Electronic Library, http://www.bibl.liu.se/english/databas/

3.2 Tools

♦ Circuit simulation and layout tools from Cadence®, http://www.cadence.com/

4 References

A.V. Bosch, M. A. F. Borremans, M. S. J. Steyaert and W. Sansen, "A 10-bit 1-Gsample/s Nyquist Current-Steering CMOS D/A Converter", IEEE J. Solid-State Circuits. Vol. 36, No. 3, March 2001.

N. Waste and K. Eshraghian, "Principles of CMOS VLSI Design", Addison-Wesley, 1993.

D.A. Johns and K. Martin, "Analog Integrated Circuit Design", John Wiley & Sons, 1997.

R.J. Baker, H.W. Li and D.E. Boyce, "CMOS Circuit Design, Layout, and Simulation", IEEE Press, 1998.

S.-M. Kang and Y. Leblebici, "CMOS Digital Integrated Circuits: Analysis and Design", McGraw-Hill, 1999

For more literature references consult with your supervisor.